

## DESIGNING AN OCTAVE-BANDWIDTH DOHERTY AMPLIFIER USING A NOVEL POWER COMBINATION METHOD

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**Abstract**—In this paper, an octave bandwidth Doherty power amplifier (DPA) using a novel combiner is presented. The fundamental bandwidth limitation of the load modulation concept of a conventional Doherty structure is solved based on the proposed combination method. For verification, an octave bandwidth asymmetric Doherty architecture is implemented by using gallium-nitride (GaN) HEMT Cree CGH40010 and CGH40025 devices in the carrier and peaking amplifiers, respectively. The carrier and peaking amplifiers are designed to achieve optimal operation with  $25\ \Omega$  load and source impedances. The reduced load and source impedances simplify the matching circuits for broadband operation. Key building blocks, including the proposed combiner, carrier and peaking amplifiers as well as the  $50/25\ \Omega$  input power divider, are outlined. The measurement results represent higher than 37% and 52% drain efficiencies in 6 dB load modulation region across the frequency range from 0.85 to 1.85 GHz and 0.90 to 1.60 GHz, respectively. The implemented Doherty amplifier represents acceptable linearity across the whole operation frequency range. In two-tone signal characterization, the implemented DPA performs with a drain efficiency of 55% and an inter-modulation distortion (IMD) of  $-30\ \text{dBc}$  at an average output power of 41.2 dBm at the center operation frequency of 1.35 GHz. In order to observe wideband signal characterization, a single carrier wideband code-division multiple access (W-CDMA) signal with a peak-to-average power ratio (PAPR) of 6.5 dB is applied and a drain efficiency of 51% with an adjacent-channel leakage ratio (ACLR) of  $-31\ \text{dBc}$  is achieved at an average output power of 38.4 dBm.

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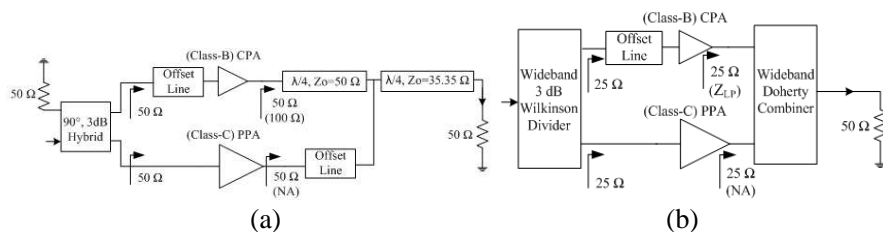
## 1. INTRODUCTION

In modern communication era, wireless communication systems require radio transmitters to operate over a wide frequency range providing multiband multimode operation. The modern communication standards cover a video bandwidth as high as 100 MHz and a peak-to-average power ratio (PAPR) up to 12 dB due to high data rates used in the spectrally efficient digital modulation schemes [1]. In addition, many electronic warfare systems, such as jammers and electronic attack systems also require multimode and multiband operation when the transmission of older communication standards is needed for backward compatibility.

The conventional power amplifiers (PAs) exhibit poor efficiency performance in back-off power levels [2]. The Doherty power amplifier (DPA) is a strong candidate for multimode multiband operation due to its low hardware complexity, wide aggregated instantaneous bandwidth and tunable efficiency characteristic for different power ranges [3–5]. In order to improve the efficiency, various kinds of DPA architecture, such as bias adapted DPA, asymmetrical DPA and multi-stage DPA, have been proposed [6–10]. There have been Doherty amplifiers reported with enhanced back-off efficiency and improved linearity by the utilization of the inter-modulation cancellation and digital pre-distortion techniques [11,12]. However, most of these studies on Doherty PAs have addressed the narrowband operation. Hence, they are not suitable for the multimode/multiband operation requirements of the modern communication systems.

The conventional Doherty PA offers enhanced efficiency characteristic in a fractional bandwidth; smaller than 10% [13,14]. The fundamental components of the conventional DPA are carrier power amplifier (CPA), peaking power amplifier (PPA) and quarter wavelength transmission line. The use of the 90° transmission line in front of the CPA should have two folds and it has a great influence on the bandwidth extension problem. Firstly, this line is used to saturate the CPA below the rated power level by providing load transformation action in low power region. Secondly, it performs the load modulation action of the CPA by PPA in high power region. Unlike ideal devices, the capacitive output impedance of the active device in the real world causes power leakage and degradation in efficiency performance [15].

Recently, there have been several investigations to enhance the efficiency performance of the DPA over a wide frequency range [16–22]. Most of the efforts are concentrated on widening the bandwidth of the quarter-wavelength impedance inverter. The conventional DPA shown in Fig. 1(a) is composed of class-B CPA, class-C PPA, 90° transmission



**Figure 1.** Doherty power amplifier (DPA) structures. (a) Conventional DPA. (b) Proposed DPA.

lines and extra offset lines. A simple offset-line is utilized to satisfy the quasi-open impedance condition at the output of the PPA in low power region.

In this paper, the DPA structure is modified for broadband operation as shown in Fig. 1(b). The output combiner structure that is composed of quarter-wavelength impedance inverter and impedance transformer in the conventional DPA is replaced by a new combiner structure. The proposed combiner is designed by considering the boundary operation conditions of the conventional combiner for proper load modulation. The boundary operation conditions of the conventional DPA combiner are defined at the transition point where the CPA reaches saturation and at the maximum power point where both amplifiers distribute their rated powers.

The other key point in this work is to design the CPA and PPA for 25 Ω terminal impedances. The reduced load and source impedances facilitate the achievements of the optimum power and efficiency performances, especially in a broadband application. Any additional component in the output matching network of the PPA that introduces positive phase dispersion narrows the maximum achievable bandwidth of the DPA [21]. Hence the reduced load impedance extends the bandwidth of the DPA by simplifying the output matching network of the PPA.

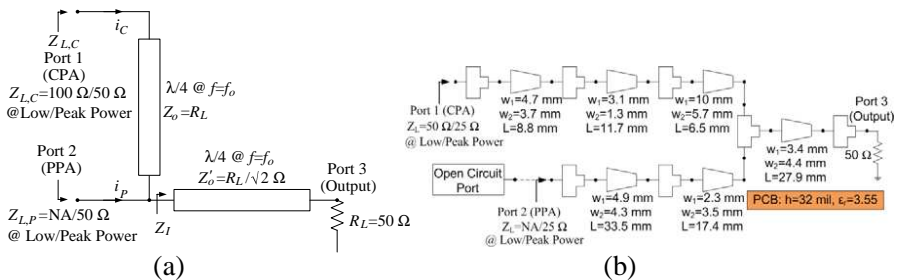
This paper is organized as follows. In Part 2, the proposed combiner structure for an ideal case is introduced and it is implemented in a frequency band ranging from 1 to 2 GHz for the conceptual verification of an octave-bandwidth operation. The design details of the fundamental wideband blocks including the carrier and peaking amplifiers as well as the 50/25 Ω input power divider are outlined in Part 3. In Part 4, the proposed combiner is modified for practical case by taking the off-state output impedance of the PPA into consideration. The conceptual implementation of wideband operation is verified experimentally in an asymmetric-DPA configuration. Finally, the conclusions are drawn in Part 5.

## 2. WIDEBAND DOHERTY COMBINER

The fundamental band limitation of the conventional Doherty combiner originates from the quarter-wavelength transmission line at the output of the CPA. The quarter-wavelength transformer has a narrow-band operation. It is known that the reduction of the transformation ratio enhances its bandwidth, however; the non-optimum transformation ratio degrades the efficiency performance of the DPA. Hence, the bandwidth enhancement by using the reduced transformation ratio is limited well below the octave-bandwidth levels.

By the transformer action of the  $90^\circ$  transmission line, the CPA reaches to saturation at the transition point (TP), which is well below the peak output power of DPA. In conventional scheme, the TP has been set at 6 dB power back-off (PBO) level, which is related to half of the peak output voltage. The PPA is inactive in the low power region up to the TP. The CPA that is matched to  $50\ \Omega$  load impedance for maximum power and efficiency performances operates into the load impedance of  $100\ \Omega$  due to the impedance transformation of the quarter-wavelength line. Doubled load impedance provides the CPA with saturating at the half of its rating power with the maximum efficiency. The CPA that is the only active portion of the DPA in the low power region performs with higher efficiency performance up to TP after which the PPA starts to operate. Referring to Fig. 2(a), the frequency dependent load impedance of the CPA in the low power region,  $Z_{L,C}$ , can be expressed as in (1) by the aid of (2) and (3) where  $f/f_0$  is the frequency normalized with the center frequency of operation:

$$Z_{L,C} = Z_o \frac{Z_I + jZ_o \tan(\theta)}{Z_o + jZ_I \tan(\theta)} \quad (1)$$



**Figure 2.** Doherty combiner structures. (a) Conventional combiner. (b) Proposed wideband combiner for 1–2 GHz.

$$Z_I = Z'_o \frac{R_L + jZ'_o \tan(\theta)}{Z'_o + jR_L \tan(\theta)} \quad (2)$$

$$\theta = \beta \ell = \frac{\pi f}{2 f_o} \quad (3)$$

The delivered fundamental output power and consumed line power by the CPA at the TP can be written as in (4) and (5), respectively, where  $i_{C,f}$  represents the fundamental output current of the CPA at the TP:

$$P_L = \frac{1}{2} (i_{C,f})^2 \text{Re} \{Z_{L,C}\} \quad (4)$$

$$P_{DC} = \left( \frac{2}{\pi} i_{C,f} \right) V_{DC} \quad (5)$$

Then, the overall efficiency of the DPA at this point can be derived as in (7) by the aid of (6):

$$R_L = \frac{V_{DC}}{2i_{C,f}} \quad (6)$$

$$\eta_{TP} = \frac{P_L}{P_{DC}} = \frac{\pi \text{Re} \{Z_{L,C}\}}{8 R_L} \quad (7)$$

In (6),  $2i_{C,f}$  represents the fundamental output current of the CPA and  $R_L$  represents the optimum load impedance of the CPA at the maximum power level. Thus, as (7) concludes, efficiency at the TP depends on the  $\text{Re}\{Z_{L,C}\}$ . As investigated in [19], the frequency dependent  $\text{Re}\{Z_{L,C}\}$  can be given as in (8) for the conventional structure:

$$\text{Re} \{Z_{L,C}\} = \begin{cases} 2R_L, & f = f_o \\ < 2R_L, & f \neq f_o \end{cases} \quad (8)$$

For an octave bandwidth operation, where the normalized frequency is in the range of (9), the smallest  $\text{Re}\{Z_{L,C}\}$  and the related efficiency at the band edges are found as given in (10) and (11):

$$\frac{f}{f_o} = [0.67 \quad 1.34] \quad (9)$$

$$\text{Re} \{Z_{L,C}\} = 0.85R_L \quad (10)$$

$$\eta = 33.5\% \quad (11)$$

33.5% efficiency is lower than what the conventional class-B amplifier offers at 6 dB PBO, i.e., 39.2%. Hence, the quarter wavelength transformer is not a good solution to achieve higher efficiency in an octave bandwidth operation.

In the high power region, PPA modulates the load of the CPA through the quarter wavelength line. By the impedance inverting action of the quarter-wavelength line, the PPA decreases the load impedance seen by the CPA, as the driving level increases beyond the TP. However, the quarter-wavelength transformer has a narrow-band operation and the non-optimum transformation ratio degrades the efficiency performances of the DPA in the high power region.

Both the CPA and PPA operate into  $50\ \Omega$  common load impedance by presenting their optimum performances and delivering equal powers to the output at the maximum power point. At the maximum power point, the only limitation originates from the outer transformer and the maximum efficiency can be realized if the condition in (12) is satisfied [13]:

$$Z_I = \frac{R_L}{2} \quad (12)$$

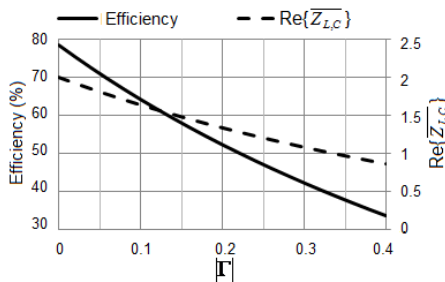
In this work, the output portion of the Doherty structure, including the band limited quarter wave-length line, is interpreted as a special combining network. The operation of this combiner is characterized at the TP and maximum power point of the ideal Doherty operation. At the TP where the PPA (port 2) has open circuit impedance, the combiner represents high return loss and low insertion loss when port-1 and port-3 are terminated with  $2R_L$  and  $R_L$ , respectively. Hence, the achievable efficiency at the TP can be depicted from the reflection coefficient,  $\Gamma$ , at port-1. In the low power region,  $\Gamma$  at port-1 can be written as given in (13) where  $\overline{Z_{L,C}}$  represents the normalized load impedance seen by the CPA with respect to the low power optimum load impedance,  $2R_L$ :

$$\Gamma = \frac{\overline{Z_{L,C}} - 2}{\overline{Z_{L,C}} + 2} \quad (13)$$

$$\overline{Z_{L,C}} = \frac{Z_{L,C}}{R_L} \quad (14)$$

In an octave bandwidth, controlling both the magnitude and phase of  $\Gamma$  is not practical. However, the worst case efficiency related to the possible smallest  $\text{Re}\{Z_{L,C}\}$  can be expressed in terms of the magnitude of  $\Gamma$  by using (7). This relation is plotted in Fig. 3 and it concludes that the worst case efficiency up to  $|\Gamma| = 0.33$  is higher than the efficiency of class-B amplifier (39.2%) driven at 3 dB back-off power. Hence, obtaining better reflection coefficient (or  $S_{11}$ ) at TP in the wide frequency band is the necessary and the sufficient condition.

The ideal combiner distributes equal power from port 1 and port 2 to the output with minimum insertion losses ( $S'_{31}$  and  $S'_{32}$ )



**Figure 3.** For a given  $\Gamma$ , smallest real part of the load impedance and associated worst case efficiency.

at the maximum power point. Hence, the required conditions at the maximum power point can be stated as in (15)–(17):

$$S'_{31} = \frac{1}{\sqrt{2}} \angle \phi_{31} \tag{15}$$

$$S'_{32} = \frac{1}{\sqrt{2}} \angle \phi_{32} \tag{16}$$

$$\phi_{31} - \phi_{32} = 0 \tag{17}$$

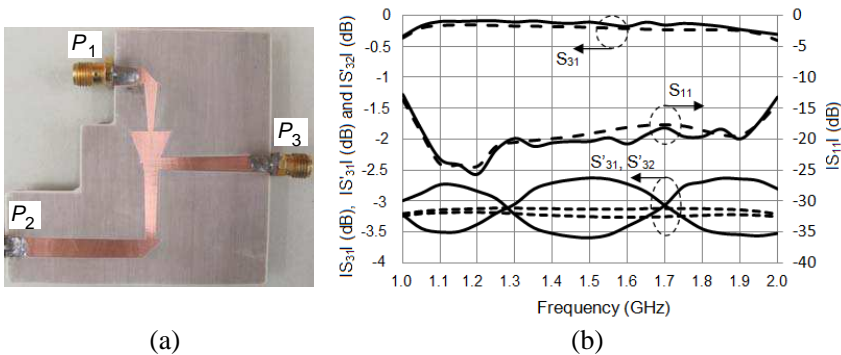
If the combiner network is lossless and reciprocal, both the CPA and PPA can operate into the ideal load impedance of  $R_L$  without any reflection.

If these boundary operation conditions at the TP and maximum power point are satisfied in a wide bandwidth, the broadband DPA design problem is simplified to the design of broadband sub-amplifiers and broadband input power divider. In this study, a novel Doherty combiner structure satisfying the boundary conditions is proposed. The condition in (17) is not attempted in the combiner design phase because it can be satisfied using simple offset line prior to the amplifiers in the DPA structure. The CPA and PPA were designed to operate into  $25 \Omega$  load impedance at the maximum power as discussed in Part 3. The proposed combiner is designed using the short-length taper lines. The taper lines are strong candidates for the applications of broadband matching and impedance transformation [23]. The optimized combiner for an octave-bandwidth application ranging from 1 to 2 GHz is shown in Fig. 2(b).

The simulated and measured characteristics of the conceptually verified wideband Doherty combiner and its photograph are given in Fig. 4. In this design, the ideal operation condition of DPA in which the output port of the PPA (port 2) presents exact open circuit condition in low power region was assumed.

In low power region up to TP, the CPA (port 1) was intended to operate for  $50\ \Omega$  load impedance with minimum insertion loss between port 1 and output port (port 3). The return loss and insertion loss behaviors of the designed combiner are shown in Fig. 4(b) as  $S_{11}$  and  $S_{31}$ , respectively. Lower than 0.4 dB insertion loss was maintained through the targeted frequency range. It shows the efficient power transfer from the CPA to the output of the DPA in low power region. Similarly, an acceptable return loss of higher than 14 dB was achieved. This indicates that the structure offers the worst case efficiency of higher than 52% across an octave bandwidth. At the maximum power point, both the CPA and PPA, which were designed to operate into  $25\ \Omega$  load impedances for their rating powers, were intended to deliver powers to the output of the DPA with minimum losses. The combiner insertion losses from the CPA port ( $S'_{31}$ ) and PPA port ( $S'_{32}$ ) are shown in Fig. 4(b). Acceptable loss performances at the maximum power point where both the CPA and PPA operate into  $25\ \Omega$  load impedances were measured with  $\pm 0.5$  dB amplitude imbalance. Wideband 50/25  $\Omega$  tapered line transformer has been used in the measurement phase of  $25\ \Omega$  ports by network analyzer.

In this way, the wideband operation of the Doherty combiner is verified. However, in this verification ideal operation of the DPA was assumed. In practical Doherty operation, the output impedance of the inactive PPA is highly capacitive and it limits the achievable



**Figure 4.** Ideal wideband Doherty combiner structure and its simulated (dashed lines) and measured (solid lines) performances. (a) Photograph. (b) Low power behavior — insertion loss ( $S_{31}$ ), return loss ( $S_{11}$ ) when port 2 is open circuited, port 1 is matched to  $50\ \Omega$  and high power behavior — combiner insertion losses ( $S'_{31}$  and  $S'_{32}$ ) when port 1 and port 2 are  $25\ \Omega$ .

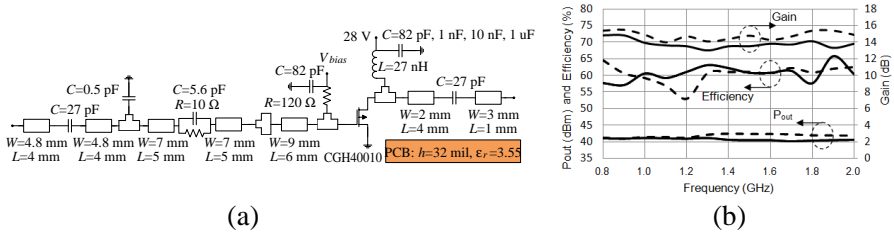


bandwidth as well. This limitation was also imported to the combiner design. The proposed combiner was improved by taking the non-open circuit condition of the inactive PPA output impedance into consideration as further explained in Part 4.

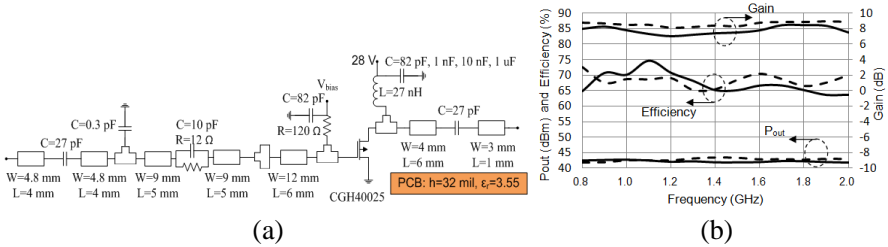
### 3. DESIGNING WIDEBAND CARRIER/PEAKING AMPLIFIERS AND POWER DIVIDER

The proposed Doherty combiner whose broadband operation capability has been verified in Part 2 simplifies the broadband DPA design problem into the design of broadband sub-amplifiers and broadband input power divider. The DPA was aimed to operate in the octave-bandwidth ranging from 0.9 to 1.8 GHz. Appropriate transistor technology selection is a key requirement in achieving a broadband power amplifier operation. The gallium nitride (GaN) transistors that have low parasitic reactance and efficient operation are strong candidates in designing a broadband amplifier [24]. In this work, the usage of GaN HEMT transistors, CGH40010 and CGH40025 from Cree Inc. (Durham, NC), were chosen in the design of CPA and PPA sections, respectively. The asymmetric DPA configuration requires different sized class-AB/C biased devices in the CPA and PPA sections in order to supply the full voltage swing and peak power at the output of the class-C biased PPA. The Doherty structure provides the designers with the flexibility of designing the sub-amplifiers for different terminal impedances. The combiner and divider should also be modified with respect to designed impedances of the CPA and PPA. Using the reduced load and source impedances instead of  $50\ \Omega$  enhances the power and efficiency performances of the broadband PAs. Moreover, the reduced load impedance extends the bandwidth of the DPA by simplifying the output matching network of the PPA. This is due to the fact that the additional component in the output matching network of the PPA introduces positive phase dispersion and narrows the maximum achievable bandwidth of the DPA [21]. Hence, the CPA and PPA devices were designed to operate into  $25\ \Omega$  load and source impedances similar to the proposed wideband combiner outlined in Part 2.

The class-AB biased CPA whose schematic and performance are given in Fig. 5 was designed to satisfy optimum power-efficiency performance over the frequency range of 0.9–1.8 GHz. The CPA was designed using 10 W Cree CGH40010 GaN HEMT transistor. The quiescent current of 30 mA was used in both the simulation and measurement phases. The parallel resistor-capacitor used in the input matching network enhanced the stability and gain flatness



**Figure 5.** Class-AB carrier power amplifier operating on  $25 \Omega$  load/source impedances and its simulated (dashed lines) and measured (solid lines) performances. (a) Circuit schematic. (b) Large signal gain, output power and efficiency characteristics.



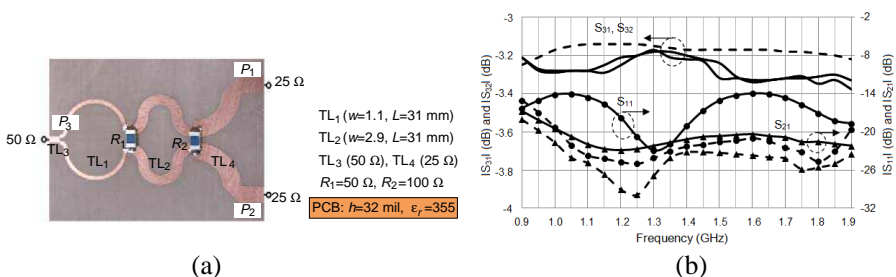
**Figure 6.** Class-C peaking power amplifier operating on  $25 \Omega$  load/source impedances and its simulated (dashed lines) and measured (solid lines) performances. (a) Circuit schematic. (b) Large signal gain, output power and efficiency characteristics.

over the operation frequencies. The load pull analysis and large signal simulations of the designed amplifier were hold on Agilent-ADS simulation tool. The empirical performances possess high conformity with the simulation performances. The implemented CPA performs with an output power of higher than 40 dBm, a drain efficiency of higher than 57% and a gain of higher than 13 dB over the targeted bandwidth of 0.9–1.8 GHz.

Similar to the CPA, the PPA design was initialized by the simulation on ADS. A 25 W Cree CGH40025 GaN HEMT transistor was utilized in design of the PPA. The gate bias voltage of  $-4.9$  V for the peaking device whose pinch-off voltage is  $-3.1$  V was used. The schematic of the designed class-C amplifier, its simulation and empirical performances over the targeted frequency band are shown in Fig. 6. The implemented PPA achieved an output power of higher than 42 dBm, a drain efficiency of higher than 64% and a gain of higher than 7 dB over the targeted frequency band. The simplified output matching

network due to the use of reduced load impedance,  $25 \Omega$ , enhances the maximum achievable bandwidth of the resultant DPA.

The last building block of the DPA structure is the wideband power divider. Since both the CPA and PPA sections were designed with  $25 \Omega$  source impedances, the input power divider was also designed to operate from  $50 \Omega$  input impedance to  $25 \Omega$  output impedances. A two-section Wilkinson divider with modified port impedances was utilized to accomplish this task. The fabricated divider and its measured performance are given in Fig. 7. The measurement results show that the divider has an insertion loss of lower than 0.4 dB, a return loss of higher than 14 dB and an isolation of higher than 17 dB over the targeted frequency band of 0.9–1.8 GHz.



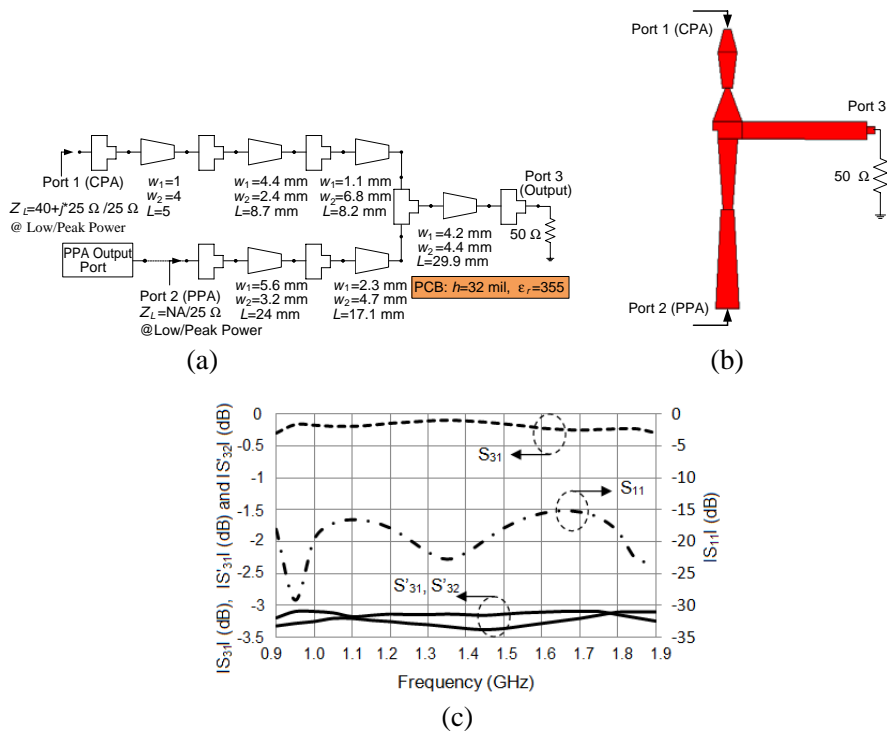
**Figure 7.** 50 Ω/25 Ω power splitter and its simulated (dashed lines) and measured (solid lines) performances. (a) Photograph. (b) Insertion loss ( $S_{31}$ ,  $S_{32}$ ), return loss ( $S_{11}$ ) and isolation ( $S_{21}$ ) characteristics.

#### 4. IMPLEMENTATION OF WIDEBAND ASYMMETRIC DOHERTY POWER AMPLIFIER

The wideband Doherty combiner was designed and fabricated for an ideal Doherty structure in Part 2. The output impedance of the inactive PPA was modeled as open circuit in that verification. However, the inactive PPA represents capacitive output impedance in the low power region of Doherty operation. In order to achieve quasi-open impedance from the PPA, the offset line is used in conventional Doherty applications. In this study, the quasi-open circuit requirement is also satisfied by the proposed combiner. The measured output impedance of the off-state PPA was modeled as one-port network and it is used in the optimization of the Doherty combiner. The maximum power load impedances of the CPA and PPA ports were defined as  $Z_{L,MP} = 25 \Omega$  similar to the ideal wideband combiner of

Part 2. In ideal Doherty operation, the low power load impedance of  $Z_{L,LP} = 2 \cdot Z_{L,MP}$  is defined to be optimum for the active device intrinsically. However, the optimum load impedance of the CPA deviates from this value due to the output matching network. The optimum load impedance of  $Z_{L,LP} = 40 + j \cdot 25 \Omega$  has been decided upon the wideband simulated efficiency performance of the CPA in the low power region [25].

The schematic and layout of the optimized wideband Doherty combiner for the targeted frequency band of 0.9–1.8 GHz is given in Figs. 8(a) and 8(b). The simulated performance of the modified combiner is given in Fig. 8(c). In the low power region where the CPA operates into  $Z_{L,LP} = 40 + j \cdot 25 \Omega$  and the PPA is in off-state, the

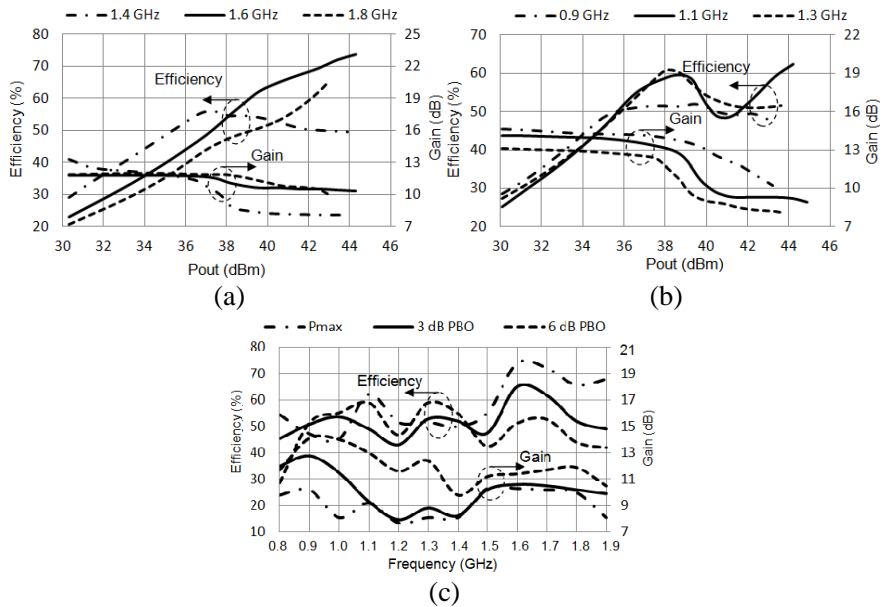


**Figure 8.** Wideband Doherty combiner for non-ideal Doherty structure. (a) Optimized circuit schematic in 0.9–1.8 GHz. (b) Simulated layout. (c) Low power behavior-insertion loss ( $S_{31}$ ), return loss ( $S_{11}$ ) when port 2 is loaded with off-state PPA, port 1 is matched to  $40 + j \cdot 25 \Omega$  and high power behavior-combiner insertion losses ( $S'_{31}$  and  $S'_{32}$ ) when port 1 and port 2 is  $25 \Omega$  loaded.

combiner has an insertion loss ( $S_{31}$ ) lower than 0.3 dB and a return loss ( $S_{11}$ ) higher than 15 dB. Combination losses ( $S'_{31}$  and  $S'_{32}$ ) lower than 0.3 dB with an amplitude imbalance of  $\pm 0.2$  dB have been achieved.

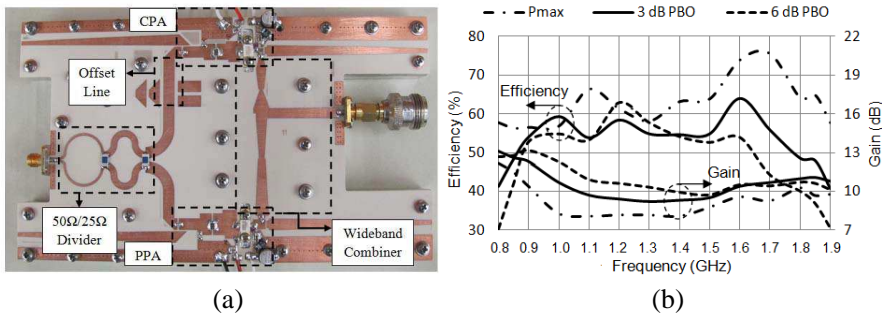
The modified wideband combiner, wideband power divider, CPA and PPA has been assembled to form an asymmetric DPA in the targeted frequency band of 0.9–1.8 GHz. The offset line of 21 mm prior to the CPA was found to be optimum in order to satisfy the in-phase power combination at the output of the DPA. The simulation results of the wideband DPA show promising results in the whole frequency band. The simulated drain efficiency and gain characteristics with 200 MHz frequency steps are given in Figs. 9(a) and (b). The drain efficiency and gain performances at different PBO cases; 0-dB, 3-dB and 6-dB, are given in Fig. 9(c). In the simulations, a drain efficiency of higher than 43% and a gain of higher than 8 dB in 6 dB PBO region have been achieved in the frequency range from 0.85 to 1.85 GHz.

The fabricated prototype of the proposed amplifier is shown in Fig. 10(a); post-tuning on the simulated structure is not required.



**Figure 9.** Simulated drain efficiency and gain performances of the wideband Doherty power amplifier. (a) Operating frequencies of 1.4, 1.6 and 1.8 GHz. (b) Operating frequencies of 0.9, 1.1 and 1.3 GHz. (c) Power backed-off (PBO) characteristics over frequency.

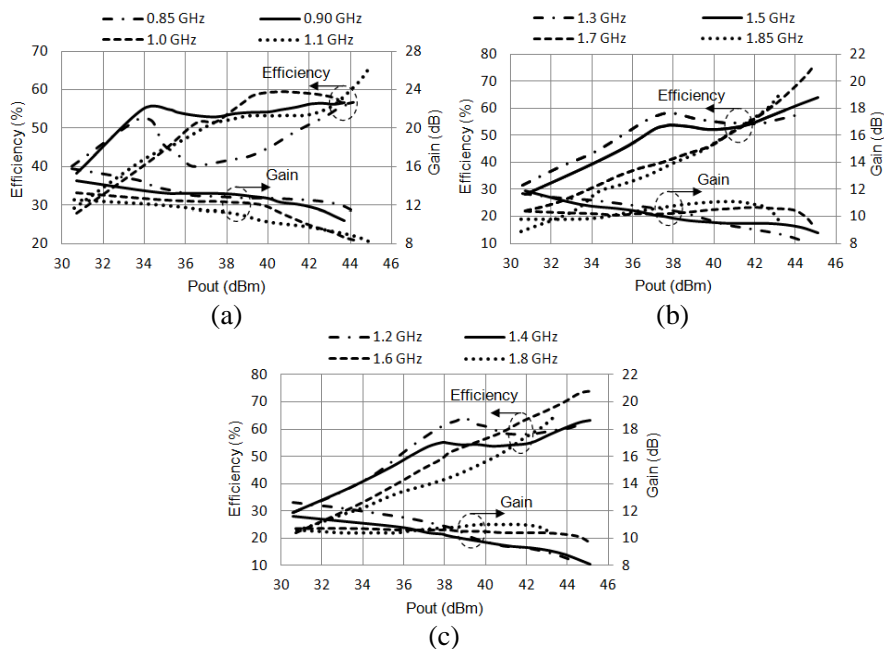
The operating points of the class-AB carrier and class-C peaking devices have been set to  $I_{DS,CPA} = 30\text{ mA}$  and  $V_{GS,PPA} = -4.9\text{ V}$ , respectively. The drain efficiency and gain performances of the fabricated amplifier for different PBO cases are summarized in Fig. 10(b). The measurements were taken in the frequency range from 0.8 to 1.9 GHz with a step of 50 MHz. The power dependent drain efficiency and gain characteristics of the amplifier for different operating frequencies between 0.85 GHz and 1.85 GHz are given in Fig. 11. The proposed wideband DPA delivers an output power of higher than 43.2 dBm in the frequency band ranging from 0.85 to 1.85 GHz. In 6 dB PBO region, it maintains higher than 37% and 52% drain efficiencies across the frequency ranges from 0.85 to 1.85 GHz and 0.9 to 1.6 GHz, respectively. The gain of the proposed wideband amplifier is higher than 8 dB in 6 dB PBO region at all operating frequencies.



**Figure 10.** Fabricated wideband Doherty power amplifier and its performance summary. (a) Photograph. (b) Drain efficiency and gain characteristics for maximum, 3 dB power back-off (PBO) and 6 dB PBO power levels.

The linearity properties of the fabricated wideband DPA were characterized by applying the two-tone signal and wideband code-division multiple access (W-CDMA) signal. The third-order and fifth-order inter-modulation distortions ( $IMD_3$  and  $IMD_5$ ) were measured by applying two-tone signals with 1 MHz frequency spacing. The  $IMD_3$  and  $IMD_5$  performances shown in Fig. 12(a) are measured at 3 dB PBO, 40–41 dBm, in the frequency band of 0.8–1.9 GHz with a step of 50 MHz. In the center frequency of 1.35 GHz, the fabricated amplifier maintains  $-30\text{ dBc } IMD_3$  and  $-34\text{ dBc } IMD_5$  with a drain efficiency of 55% at the output PAPR of 2.8 dB.

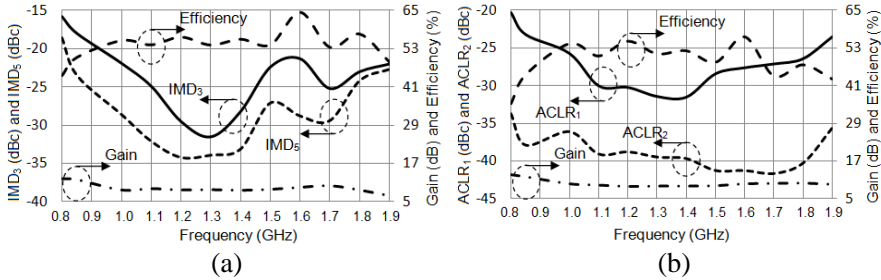
Linearity performance of this amplifier is considered to be acceptable for such a wideband amplifier. W-CDMA signal with



**Figure 11.** Measured drain efficiency and gain performances of the fabricated wideband Doherty power amplifier. (a) Operating frequencies of 0.85, 0.9, 1.0 and 1.1 GHz. (b) Operating frequencies of 1.3, 1.5, 1.7 and 1.85 GHz. (c) Operating frequencies of 1.2, 1.4, 1.6 and 1.8 GHz.

PAPR of 6.5 dB was applied to observe the adjacent-channel leakage ratio (ACLR) of the amplifier. The  $ACLR_1$  (with 5 MHz offset) and  $ACLR_2$  (with 10 MHz offset) were measured at 6 dB PBO, 37–38 dBm. The measurement results are given in Fig. 12(b). The fabricated amplifier achieves an  $ACLR_1$  of  $-31$  dBc and an  $ACLR_2$  of  $-39$  dBc at center frequency operation of 1.35 GHz. The related drain efficiency was noted as 51%. The ACLR values measured in such a wideband application is again considered to be acceptable. In order to satisfy the spectral emission mask requirements of the communication standards, there have been many reported promising works with using digital pre-distortion methods [12].

Table 1 summarizes the performance of the fabricated wideband DPA and it compares the performance of the wideband DPA of this study with those present in the literature. The modified DPA of [22] is out of this comparison due to the required external system used to configure the input signals of the CPA and PPA. The widest band



**Figure 12.** Measured nonlinearity performances of the wideband Doherty power amplifier. (a)  $\text{IMD}_3$ ,  $\text{IMD}_5$ , efficiency and gain at 40–41 dBm (3-dB PBO) 2-tone average output power. (b)  $\text{ACLR}_1$  (5 MHz offset),  $\text{ACLR}_2$  (10 MHz offset), efficiency and gain at 37–38 dBm (6-dB PBO) average output power.

**Table 1.** Comparison of broadband Doherty amplifiers in the literature.

Publication Year	Frequency Range (GHz)	BW (%)	Minimum DE (%) in 6 dB PBO Region	Minimum 6 dB PBO $P_{out}$ (dBm)	Technology	Reference
2010*	1.7–2.3	30	~35	~36	LDMOS	[17]
2010	1.5–2.14	35.2	33	36.1	GaN	[18]
2011	1.7–2.6	41.9	~36	~36.2	GaN-Asymmetric	[19]
2012	2.2–2.96	29.5	~37	~34.2	GaN	[21]
2012	0.7–1	35.3	~52	-43.2	GaN	[13]
2013*	1.5–2.4	46.2	~49	36	GaN	[22]
2013	0.85–1.85 (0.90–1.60)	74.1 (56)	37 (52)	37.2 (37.7)	GaN-Asymmetric	This work

\* Proposed DPA requires individually controlled and configured input signals for the carrier and peaking devices.

DPA in the literature has 41.9% bandwidth (BW) with minimum drain efficiency (DE) of 36% in 6 dB PBO region whereas the fractional BW of 74.1% with DE of higher than 37% has been achieved in this study. Similarly, the most efficient, wideband DPA in the literature has a minimum DE of 52% in the fractional BW of 35.3% whereas the DPA implemented in this study has a DE of higher than 52% in the BW of 56%. This enhancement in the BW is possible because unlike the previous studies that focused on quarter-wave length inverter



optimization or matching network optimization, the whole output section of the DPA is interpreted as a special combiner network and the broadband combiner structure is proposed and used to solve the bandwidth limitation problem in this study. Moreover, the reduced load impedance of  $25\ \Omega$  instead of conventional  $50\ \Omega$  enhances the fractional BW by reducing the phase dispersion at the output of the PPA in low power region.

## 5. CONCLUSION

A new Doherty amplifier structure with an octave bandwidth operation capability is presented based on the proposed novel combination method. This novel combiner solves the fundamental bandwidth limitation problem of a conventional Doherty structure. It uses the boundary operation conditions of the conventional Doherty combiner at the transition and peak power points. It achieves the required load transformation function of the carrier amplifier in the load modulation region. Moreover, the proposed combiner removes the requirement of an extra offset line in front of the peaking amplifier. The proposed combiner simplifies the bandwidth limitation problem of the Doherty amplifier into the wideband design of the carrier amplifier, peaking amplifier and the input power divider. The conceptual implementation of the proposed combiner has been verified by achieving an octave bandwidth operation ranging from 1 to 2 GHz.

For the verification of an octave bandwidth Doherty amplifier, a carrier and a peaking amplifier with  $25\ \Omega$  terminal impedances and a wideband input divider from  $50\ \Omega$  to  $25\ \Omega$  terminal impedances have been designed optimally in the frequency band ranging from 0.9 to 1.8 GHz. After the optimization of the proposed output combiner in 0.9–1.8 GHz frequency band, an asymmetric Doherty amplifier has been designed and implemented. The implemented asymmetric Doherty amplifier structure presented higher than 52% and 37% drain efficiencies through 6 dB PBO region in the operation frequency bands of 0.9–1.6 GHz and 0.85–1.85 GHz, respectively. The implemented DPA also possesses acceptable linearity performance for such a wideband amplifier. In two-tone signal characterization, the amplifier represents an  $\text{IMD}_3$  of  $-30\ \text{dBc}$  at a drain efficiency of 55% at the center operation frequency. In a single-carrier W-CDMA operation mode with a PAPR of 6.5 dB, a drain efficiency of 51% has been achieved with an ACLR of  $-31\ \text{dBc}$ . To the best of authors' knowledge, this work represents the most wideband Doherty amplifier published in the literature. Acceptable wideband nonlinearity characteristics can be further improved applying digital pre-distortion techniques.

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