

Analytical Optimization of High Performance and High Quality Factor MEMS Spiral Inductor

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Abstract—In this paper, design and simulation of optimized MEMS spiral inductor are presented. The effects of design parameters on characteristics of inductor have been considered. The suspended spiral inductor was designed on silicon substrate using MEMS technology to reduce the metal and substrate losses of inductor. The results show that the quality factor of the inductor is 27 at 5.23 GHz and that the maximum Q -factor is 42 at 26.56 GHz. The dimension of the inductor is $185 \times 200 \mu\text{m}^2$, which occupies less area on chip than other works. In this work, the high quality factor inductor with small size is obtained.

1. INTRODUCTION

In many on-chip RF components, inductors play an important role and are essential elements. The quality factor is a very important parameter in the design of spiral inductor which can be a key element for high performance RF circuits such as voltage controlled oscillator (VCO) and low-noise amplifier (LNA). As silicon processing technologies advances with huge improvements are made to the transistor's speed and cut-off frequency, RF circuits operating at higher frequencies will benefit from small-size, high Q -factor inductors [4]. Standard silicon IC process cannot provide inductor Q factors higher than 12, which is not sufficient. The reasons for these low Q factors come from thin metal layers (ohmic loss) and high substrate coupling (eddy current loss) in standard silicon processes [12]. The substrate and metal losses in standard silicon process lead to reducing the self-resonant frequency and quality factor of conventional CMOS inductor, respectively. The CMOS inductor problems limit the device performance and furthermore the specifications of RF circuits. MEMS technology provides the best solution to fabricate small, low loss, high quality factor, and CMOS compatible devices. Several works used MEMS technology to enhance the quality factor of inductor. For instance, Tseng et al. [8] employed post-CMOS process to fabricate inductor. The quality factor of CMOS and CMOS-MEMS inductors were 8 and 13 at 5.8 GHz, respectively. The maximum Q -factor and inductance of the CMOS-MEMS inductor were 15 and 1.88 nH at 8.5 GHz, respectively. Dai et al. [5] manufactured a suspended CMOS-MEMS inductor using post-process. The maximum Q -factor of inductor was 15 at 11 GHz. Fang et al. [6] fabricated a high performance MEMS planar spiral inductors. Two types of spiral inductor with different inner diameters were fabricated. The maximum quality factor of the spiral inductor — type A is 15.8 at 1.4 GHz, and type B is 19.7 at 4.1 GHz in which type B had a lower inner diameter than type A. Lee et al. [3] fabricated MEMS spiral inductors and characterized the properties of inductors according to the substrates, size of gap between the inductor metal lines, and the width of the inductor. The quality factor of inductor fabricated on silicon substrate with an oxide insulation layer was over 20 at 1 GHz, and the maximum quality factor of inductor fabricated on silicon substrate with a nitride insulation layer was 15 at 1 GHz. In addition, the simulated values of this parameter on the nitride insulation layer and oxide insulation layer were 12.5 and 21.5 at 1 GHz, respectively. To fully exploit the cost-effective

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silicon technologies, area-efficient inductors with optimized performance at the application frequency are required [4].

This paper proposes an optimum design of MEMS spiral inductor with high quality factor and small size with good performance at high frequency.

2. DESIGN AND MODELING OF THE MEMS SPIRAL INDUCTOR

To characterize a spiral inductor, three parameters are usually employed as figure-of-merits, i.e., Q -factor, inductance, and Self-Resonant Frequency (SRF). These parameters determine the performance of a spiral inductor [9]. Figure 1 shows the schematics of the proposed spiral inductor. The design parameters are the width of the line (W), space between turns (S), number of turns (n), inductor shapes, metal thicknesses (t), outer diameter (D_{out}), and inner diameter (D_{in}) which determines the value of inductance and quality factor of inductor.

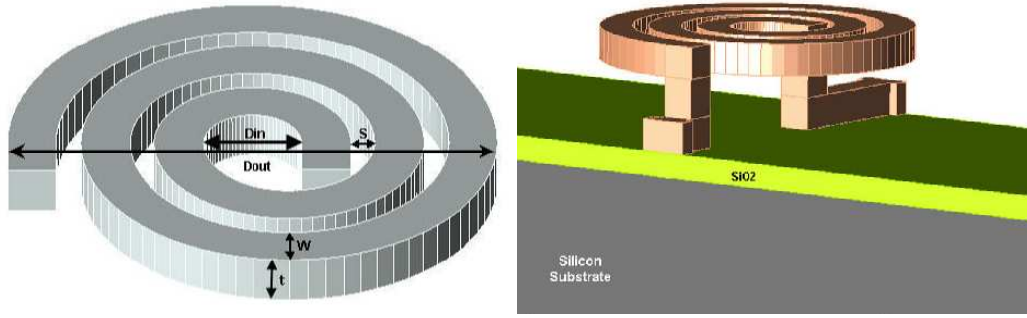


Figure 1. Schematics of the 2.5 turn spiral inductor.

Modeling inductors on the silicon substrate requires a compact physical model. Figure 2 shows that the simple lumped model of inductor consists of nine elements. The series inductance and series resistance of inductor are expressed by L_s and R_s , respectively. The distance between inductor turns creates capacitance represented by series capacitance and modeled by C_s . The capacitance between the spiral inductor and substrate is modeled by C_{ox} . The resistance and capacitance of the silicon substrate are represented by R_{si} and C_{si} . The substrate parasitic components presented in Figure 2 by R_{si} , C_{si} , and C_{ox} can be modeled by two equivalent parameters (R_p and C_p) as illustrated in Figure 3.

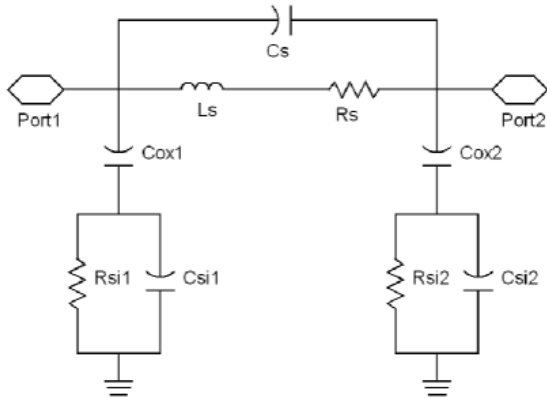


Figure 2. The lumped model of inductor.

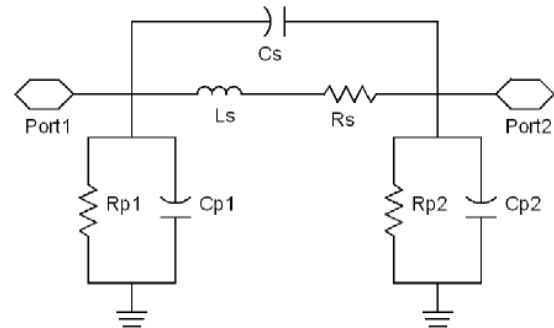


Figure 3. The equivalent model of inductor.

The substrate capacitance C_{si} is determined by:

$$C_{si} = \frac{WlC_o}{2} \quad (1)$$

where W is the metal width, l the total length of the inductor, and C_o the substrate capacitance per unit area depending on the physical properties of the substrate called fitting parameter and typically between 10^{-2} and 10^{-3} fF/ μm^2 . The substrate resistance R_{si} can be given as:

$$R_{si} = \frac{2}{WlG_o} \quad (2)$$

where G_o is the substrate conductance per unit area depending on the physical properties of the substrate called fitting parameter and typically around 10^{-7} S/ μm^2 . The inductor-substrate oxide capacitance C_{ox} can be expressed as:

$$C_{ox} = Wl \left(\frac{\varepsilon_{ox}}{2t_{ox}} \right) \quad (3)$$

where $\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/m is the oxide permittivity and t_{ox} the distance between the spiral inductor and the substrate. The shunt capacitance C_p which is shown in an equivalent inductor model is given by:

$$C_p = C_{ox} \left(\frac{1 + \omega^2 (C_{si} + C_{ox}) C_{si} R_{si}^2}{1 + \omega^2 (C_{si} + C_{ox})^2 R_{si}^2} \right) \quad (4)$$

The shunt resistance R_p which is shown in an equivalent inductor model is given by:

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{si}} + \left(R_{si} \left(\frac{(C_{si} + C_{ox})^2}{C_{ox}^2} \right) \right) \quad (5)$$

The series capacitance C_s , created due to the distance between the spiral turns, is determined by:

$$C_s = nW^2 \left(\frac{\varepsilon_{ox}}{t_{ox,M1-M2}} \right) \quad (6)$$

where n is the turn numbers and $t_{ox,M1-M2}$ the distance between the turns. Finite conductivity of metal layer occurs when the thickness of the inductor metal layer is less than the effective thickness. This is one of the metal loss mechanisms modeled by series resistance R_s :

$$R_s = \frac{\rho l}{W\delta \left[1 - e^{-\frac{l}{\delta}} \right]} \quad (7)$$

where ρ is the resistivity of metal, t the metal thickness in micron meter, and δ the skin effect depth given by:

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}} \quad (\mu\text{m}) \quad (8)$$

where f is the frequency in GHz and μ the magnetic permeability. An accurate expression for inductance L_s can be given by:

$$L_s = \frac{\mu_0 n^2 D_{avg} c_1}{2} \left(\ln \left(\frac{c_2}{\rho} \right) + c_3 \rho + c_4 \rho^2 \right) \quad (9)$$

where μ_0 is the magnetic permeability of free space equal to $4\pi \times 10^{-7}$ H/m, and ρ is the fill ratio and can be expressed by:

$$\rho = \frac{D_{out} - D_{in}}{D_{out} + D_{in}} \quad (10)$$

And D_{avg} is the average diameter and can be given by:

$$D_{avg} = \frac{D_{in} + D_{out}}{2} \quad (11)$$

And c_1 , c_2 , c_3 , and c_4 are layout depending factors that shown in Table 1 [10].

Table 1. Coefficients of layout depending factors for circular inductor.

Layout	c_1	c_2	c_3	c_4
circle	1	2.46	0	0.2

The quality factor, Q , of the inductor can be expressed as:

$$\begin{aligned}
 Q &= 2\pi \times \frac{[\text{peak magnetic energy} - \text{peak electric energy}]}{\text{energy loss in one oscillation cycle}} \\
 &= \frac{\omega L_s}{R_s} \cdot \frac{1}{1 + \frac{R_s}{R_p} \left[\left(\frac{\omega L_s}{R_s} \right)^2 + 1 \right]} \cdot \left[1 - \frac{R_s^2 (C_s + C_p)}{L_s} - \omega^2 L_s (C_s + C_p) \right] \quad (12)
 \end{aligned}$$

where the first term is the conventional equation and intrinsic quality factor of the overall inductor which represents the magnetic energy stored along with the ohmic loss. The second term represents the substrate loss. The final term represents the self-resonance due to the parasitic capacitance losses. It should be noted that the quality factor in an inductor depends on the inductance of inductor, material properties, and selective central frequency.

As the frequency increases, R_s increases mainly due to both skin and proximity effects [13]. The metal line width and metal thickness are important parameters to increase the quality factor of inductor. According to Equation (7), by increasing the width and thickness of metal line the resistive loss is decreased, and quality factor can be increased. The sharp points in the path of current increase the crowding of current as well as at the edges of inductor which causes the increase in the resistance of the line. The circular shape inductor has less resistive loss than the other shapes due to not having sharp points which can lead to high quality factor. Silicon substrate has been used to design the inductor. The substrate losses and substrate coupling can be reduced using suspended inductor on substrate. At a certain frequency, resonance will occur due to the parasitic effects of the substrate and distribution characteristic of metal tracks. After the SRF point, the inductor has a negative reactance value, thus behaves as a capacitor. Usually, the inductors are required to operate at frequencies far from its SRF. When self-resonance happens, the inductive reactance and parasitic capacitive reactance become equal. This means that the imaginary part of the one-port input impedance is equal to zero [9]. As seen from Equation (6), the parasitic capacitance due to inter-winding capacitance can be reduced by choosing a suitable distance between the spiral turns which lead to increase the self-resonant frequency. The natural conductivity of silicon substrate creates a capacitance between inductor and substrate, which is called substrate capacitance. According to Equation (3), by increasing the distance between inductor and substrate, the substrate capacitance is decreased. Furthermore, the substrate capacitance which creates parasitic capacitance can be reduced by depositing a thick silicon oxide as an insulation layer, and this layer can also isolate the inductor from substrate and reduce the losses.

At low frequencies, loss is mainly due to the series ohmic metal loss, thus wider track width, thicker and higher conductivity metal should be used to get a larger $Q_{\max}$. While at high frequencies, Q -factor will be dominated by substrate loss. Therefore, narrower track width or smaller outer-dimension will be better for minimizing the occupied chip area, thus minimizing substrate loss [9]. At high frequency penetration of magnetic field and current into conductor decreases, and the current flowing in the outer area of conductor which this phenomenon is called skin effect. When the frequency is very high, and thus the skin depth becomes very shallow, the currents are almost restricted in a very thin shell of the metal [11].

3. OPTIMIZATION OF THE SPIRAL INDUCTOR

In this section, the analytical optimization of the spiral inductor using equations is performed, and the effect of design parameters on inductance, quality factor, and SRF are expressed. It should be noted that optimization is based on changing one parameter, while the other parameters are constants. Also the thickness of the inductor is 20 μm . Figure 4 shows the effect of the inductor line width on

quality factor. The area of magnetic flux is increased by increasing the line width of inductor. At low frequency, the line resistance is decreased which leads to increasing the quality factor, thus the inductor with thicker line width has higher quality factor. But at high frequency, according to Equation (3), the parasitic capacitance between the spiral inductor and the substrate is increased which leads to reducing the quality factor and SRF.

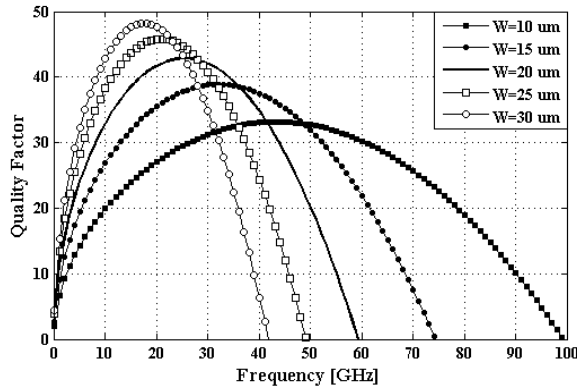


Figure 4. Q -factor of inductor with different line width ($D_{in} = 40 \mu\text{m}$, $S = 10 \mu\text{m}$, $n = 2.5$).

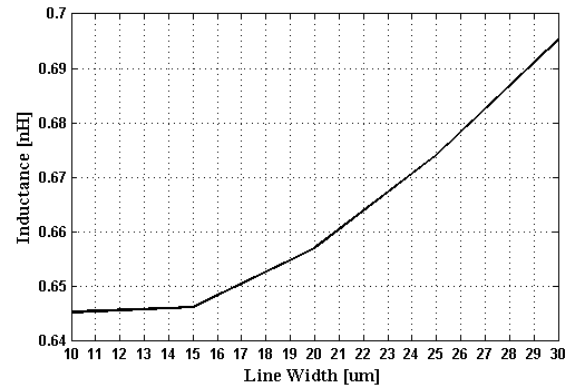


Figure 5. The inductance of inductor with different line width ($D_{in} = 40 \mu\text{m}$, $S = 10 \mu\text{m}$, $n = 2.5$).

Figure 5 shows the effect of inductor line width on the inductance. It can be seen that by increasing the line width, the inductance is increased. Large conductor width designs are found to yield good performance for inductors with small inductance values [4]. Figure 6 illustrates the quality factor as a function of frequency with different space between the turns. As seen from Figure 6, at high frequency by increasing the distance between turns, the parasitic capacitance between spiral inductor and substrate is increased and the quality factor decreased.

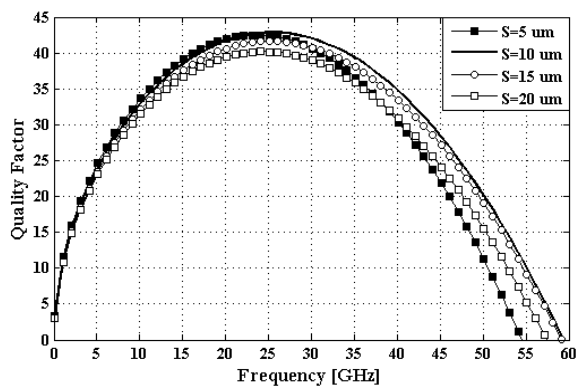


Figure 6. The Q -factor of inductor with different space between turns ($D_{in} = 40 \mu\text{m}$, $W = 20 \mu\text{m}$, $n = 2.5$).

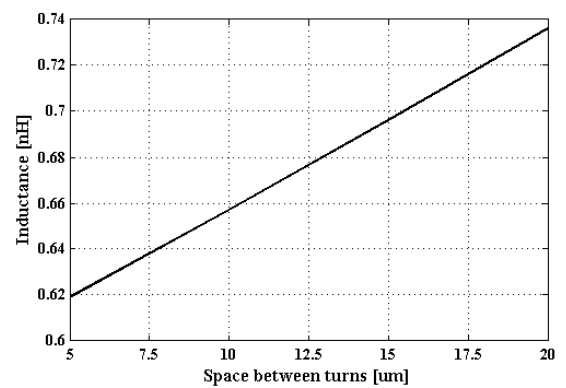


Figure 7. The inductance of inductor with different space between turns ($D_{in} = 40 \mu\text{m}$, $W = 20 \mu\text{m}$, $n = 2.5$).

The total inductance of a loop is then equal to the sum of the partial self-inductances of each straight element plus all the partial mutual inductances between the elements [2]. As shown in Figure 7, by increasing the space between turns, the inductance increases due to more mutual inductive coupling between conductors.

Figure 8 indicates the effect of turns number on the quality factor. The length of the line is increased by increasing the number of turns and according to Equation (3) the parasitic capacitance between the spiral inductor and the substrate is increased which leads to reducing the quality factor. According to

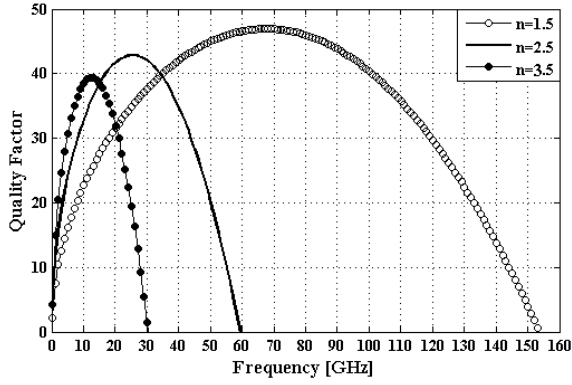


Figure 8. The Q -factor of inductor with different turn numbers ($D_{in} = 40 \mu\text{m}$, $W = 20 \mu\text{m}$, $S = 10 \mu\text{m}$).

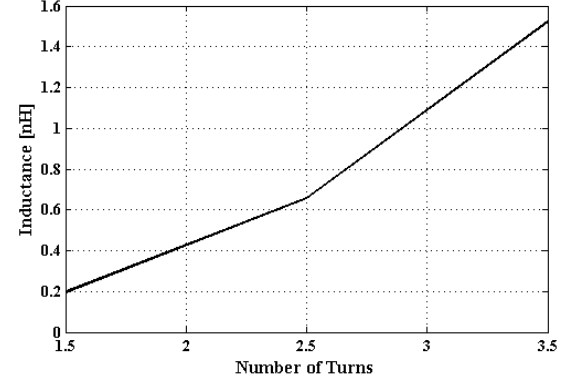


Figure 9. The inductance with different turn numbers ($D_{in} = 40 \mu\text{m}$, $W = 20 \mu\text{m}$, $S = 10 \mu\text{m}$).

Equation (9), by increasing the number of turns the inductance of the inductor is increased, which is demonstrated in Figure 9.

Figure 10 shows the results of the quality factor as a function of the frequency with different inductor inner diameters. The parasitic capacitance between the spiral inductor and the substrate is increased by increasing the inner diameter of inductor, which leads to decreasing the quality factor.

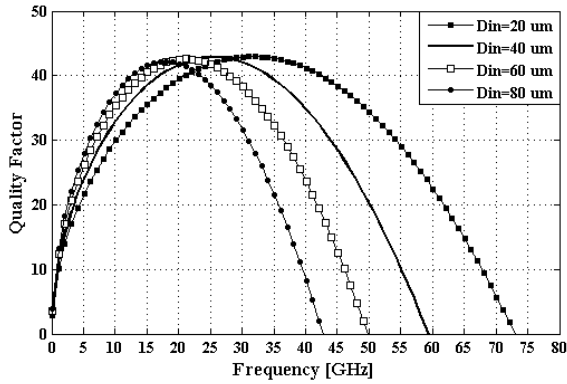


Figure 10. The Q -factor with different inner diameters ($W = 20 \mu\text{m}$, $S = 10 \mu\text{m}$, $n = 2.5$).

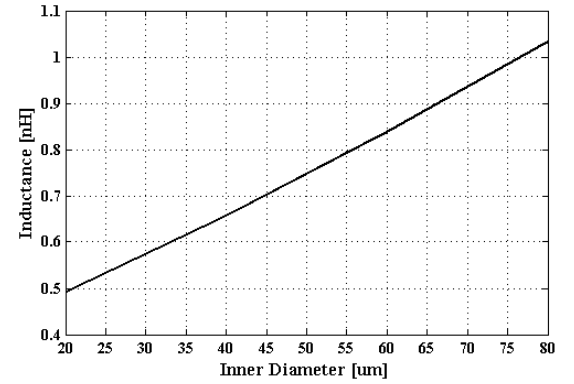


Figure 11. The inductance with different inner diameters ($W = 20 \mu\text{m}$, $S = 10 \mu\text{m}$, $n = 2.5$).

According to Equation (9), by increasing the inner diameter the length of the inductor increases, and more magnetic flux can be passing into the inductor which causes the increase of the inductance. Figure 11 shows the effect of the inductor inner diameter on inductance.

According to the above results, the optimized parameters of the inductor are shown in Table 2.

Table 2. Geometrical parameters of inductor.

shape	D_{out}	D_{in}	W	S	n
circular	200 μm	40 μm	20 μm	10 μm	2.5

Figure 12 shows the quality factor of the optimized inductor as a function of frequency.

From the above results, it can be concluded that the quality factor, inductance, and SRF are dependent on the line width, distance between turns, turn numbers, and inner diameter. Many variables

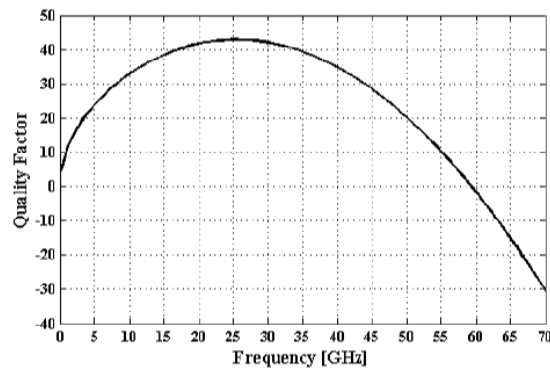


Figure 12. The Q -factor of the optimized inductor ($D_{in} = 40 \mu\text{m}$, $W = 20 \mu\text{m}$, $S = 10 \mu\text{m}$, $n = 2.5$).

Table 3. General trends on Q -factor, inductance, and SRF of spiral inductor based on effects of design parameters.

Design Parameters		Quality Factor (peak Q)	Inductance	SRF
line Width	Increase ($\uparrow$)	Increase	Increase	Decrease
Distance Between Turns	Increase ($\uparrow$)	Slight Decrease	Increase	Insignificant Difference
Turn Numbers	Increase ($\uparrow$)	Decrease	Large Increase	Large Decrease
Inner Diameter	Increase ($\uparrow$)	Decrease	Increase	Decrease

may be optimized in the design of the spiral inductor. Table 3 shows the trends on the quality factor, inductance, and SRF of the spiral inductor based on the effect of design parameters such as line width, distance between turns, turn numbers, and inner diameter.

In this work, the MEMS inductor is suspended around $25 \mu\text{m}$ above the topmost layer. The thickness of inductor is $20 \mu\text{m}$, and $15 \mu\text{m}$ thick insulation layer is deposited on substrate. The maximum quality factor is 42.85 at 25.2 GHz. Using Equation (12), the quality factor of the inductor is about 24.33 at 5.23 GHz, and also using Equation (9) the inductance is about 0.65 nH. The series resistance of the inductor is about 0.87Ω at 5.23 GHz. The other calculated parameters of the inductor have been summarized in Table 4.

Table 4. Calculated parameters of the inductor.

C_{si}	R_{si}	C_{ox}	C_s
94.24 fF	1061.03 Ω	8.12 fF	3.45 fF

4. RESULTS AND DISCUSSION

In this work, the ADS software has been used to design and simulate the MEMS inductor. Figure 13 illustrates the simulated quality factor of the inductor. The maximum quality factor of the spiral inductor is 42.84 at 26.56 GHz. Figure 14 shows the simulated inductance of the inductor. The inductance of the inductor is about 0.61 nH at 5.23 GHz, which is very close to calculated result. Also, the SRF of the inductor is about 65.5 GHz. As can be seen from Figure 14, the inductance value is a constant from 0 to 50 GHz.

Figure 15 shows the analytical and simulated results of quality factor versus frequency for optimized inductor. The calculated quality factor is 24.33 at 5.23 GHz. At the same frequency, the simulated quality factor is 27.31.

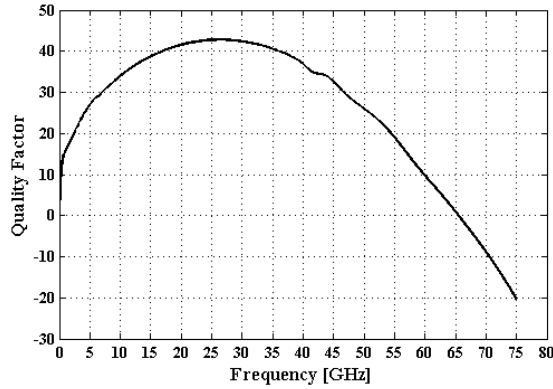


Figure 13. The quality factor of the spiral inductor.

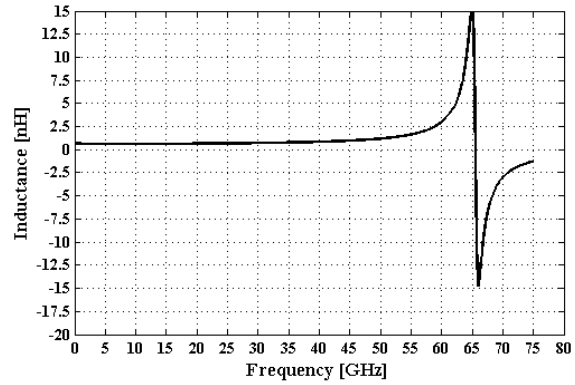


Figure 14. The inductance of the spiral inductor.

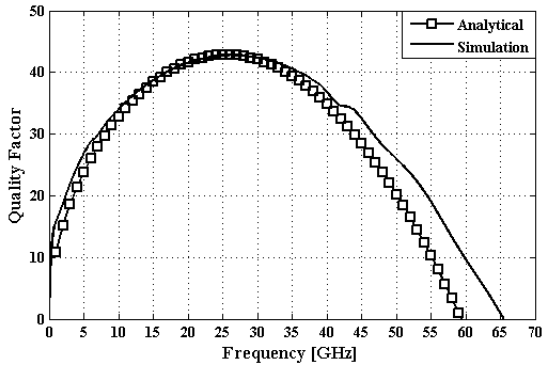


Figure 15. The quality factor versus frequency for optimized inductor.

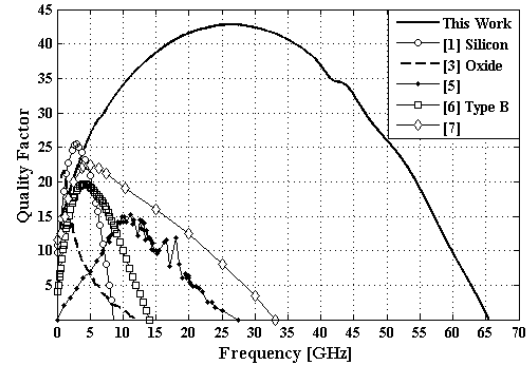


Figure 16. Comparison of quality factor for different Inductors.

Figure 16 shows the quality factor of some previous works and our work. It can be seen that in this work the MEMS spiral inductor has higher quality factor than other works.

Table 5 shows the comparison between previous works and our design. It can be seen that in this work the area of the inductor has been reduced and the quality factor increased. The quality factor of the inductor at 5.23 GHz is 27.3, and the maximum Q -factor is 42.8 at 26.56 GHz. The dimension of the inductor is $185 \times 200 \mu\text{m}^2$ which occupies less area than the other works. The self resonant frequency

Table 5. Comparison of different inductors.

works	Results of	shape	Freq (GHz)	Q	L (nH)	Size (μm^2)	SRF (GHz)
[1] SI-GaAs	measurement	rectangle	5.4	29.5	15	470×470	11.4
[1] silicon	measurement	rectangle	5.4	19.4	12.5	470×470	8.6
[3] nitride	simulation	rectangle	1	12.5	2.4	315×315	13
[3] oxide	simulation	rectangle	1	21.5	2.6	315×315	14
[5]	measurement	circular	11	15	1.4	216×228	27.5
[6] type A	measurement	rectangle	1.4	15.8	4.61	1900×1920	9
[6] type B	measurement	rectangle	4.1	19.7	1.4	980×1000	14
[7]	simulation	circular	2.4	22	1.5	500×500	33
[13]	simulation	rectangle	2.5	8.5	6	265×265	6
This work	simulation	circular	5.23	27.31	0.61	185×200	65.47

of the inductor is 65.5 GHz, which is much more than the other works. Also, the new MEMS spiral inductor is based on silicon substrate which is compatible with CMOS process and can be integrated with CMOS elements.

5. CONCLUSION

In this paper, the design parameters of inductor such as line width, distance between the turns, turn numbers, inductor shape, metal thickness, and inner diameter are optimized, and the effect of them on quality factor, inductance, and SRF of inductor are considered. In addition, the equivalent circuit of inductor and accurate model of circuit elements are expressed. The calculated quality factor is 24.33 at 5.23 GHz, and the inductance is 0.65 nH. The maximum quality factor is 42.85 at 25.2 GHz. The layout of the inductor is designed and simulated using ADS software. The quality factor and inductance of the inductor are 27.31 and 0.61 nH at 5.23 GHz, respectively. The maximum quality factor is 42.84 at 26.56 GHz. The dimension of the inductor is $185 \times 200 \mu\text{m}^2$ which occupies less area than the other works.

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