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A Tradeoff Design of Broadband Power Amplifier in Doherty Configuration Utilizing a Novel Coupled-Line Coupler

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Abstract—A broadband power amplifier designed and implemented in Doherty configuration is illustrated in this paper. Both input and output networks adopt the broadband matching topology. Additionally a compensation network, consisting of a series transmission line shunted with a capacitance, is set behind the peak amplifier to avoid in-band power leakage in the low-power section while at the cost of peak output power in partial band. A novel coupler is designed as an uneven power-divided splitter and experimentally validated for a broadband power amplifier module. A tradeoff of bandwidth, efficiency and output power is fulfilled through parameters select and postproduction tuning. According to the measured results, the proposed broadband Doherty power amplifier achieves an average saturated output power of 42 dBm, an average gain of 10.6 dB, an average peak and 6 dB back-off efficiency of 48.4% and 32.8%, respectively, and a fractional bandwidth of 51.4%, from 1.3 GHz to 2.2 GHz. The adjacent channel power ratio is better than −40 dBc when the amplifier is driven with 10-MHz QPSK signal, thus exhibiting a high linearity performance.

1. INTRODUCTION

Along with the rapid evolution of modern communication system, the standard of modulated signal such as long-term evolution (LTE) signal requires an aggregate bandwidth of up to 100 MHz for a larger channel capacity. The advanced software defined radio (SDR) technology also put strong emphasis on the power amplifier's bandwidth. Moreover, the broadband amplifier can significantly reduce the hardware research & develop costs due to the compatibility for the old and new wireless standards. Therefore the design of broadband amplifiers is necessary and promising.

Another fact that cannot be ignored is that modern wireless communication system highly emphasizes on the high efficiency performance of the microwave power amplifiers (PAs) over a wide range of the output back-off power level due to the modern modulated signals with high PAPR (peak-to-average power ratio) around 5–12 dB. Under this condition, Doherty power amplifiers (DPA) [1], characterized by the significant improvement on back-off efficiency, have been widely designed and implemented. To further expand the performance in efficiency and linearity, numerous efforts have been made to combine DPA with digital pre-distortion [2], adaptive bias [3], adaptive load modulation [4], switch structure [5], to name as a few. However, the performance of bandwidth is still unsatisfied and limited ($< 10\%$).

In past literatures, many designs and implementations of dual-band Doherty architecture [6–8] and broadband Doherty amplifier [9–17] have been reported. It is worth mentioning that dual-band technologies have the limitation of a high frequency-ratio, while in practical situation, taking China Mobile for instance, the frequency-ratio of 2G standard (GSM1800) and 3G standard (TD-SCDMA) is only about 1.11. As a consequence, we concern on the design of a broadband amplifier. Various

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technologies and structures are proposed to broaden bandwidth of Doherty PA. For instance, a wideband DPA with a simplified structure is reported with a fractional bandwidth of 35% in [9]. In [17], a new matching strategy is proposed, that is, the two PAs are not matched to 50 Ω, thus to eliminate the quarter-wave transmission lines. Finally the Doherty power amplifier with 40% bandwidth is reported. A comprehensive method, real frequency technique, for broadband Doherty PA designing is proposed in [16] and a calculated fractional bandwidth of 29.5% is achieved. A novel output combining network — four sections of quarter-wave transmission lines, is adopted in [14]. A 14% of fractional bandwidth is achieved using this structure. Authors in [15] explored an evolution of the network in [14], thus achieving a Doherty PA with a 36% fractional bandwidth. A novel output compensator network is exploited in wideband DPA design in [12], where a fractional bandwidth of 18.2% is achieved, at a center frequency of 3.3 GHz. Digital technologies are applied to the DPA in [13], where a fractional bandwidth of 22.6% is achieved. However the digital technologies significantly add the complexity of the circuits. A modified Doherty configuration, which solves the problem of inherently narrow-band characteristic in traditional Doherty configuration, is presented in [10], where a fractional bandwidth of 35.3% is achieved. However, the ACPR without DPD is only −23.15 dBc at an average output power of 39.14 dBm when driven with a 20-MHz LTE signal at 740 MHz. In addition, the external technology increases the design complexity and the implementation cost.

In this paper, we present the design of a broadband power amplifier in Doherty configuration, over a 900 MHz bandwidth, from 1.3 GHz to 2.2 GHz (51.4% fractional bandwidth), which covers the mainstream communication standards such as TD-SCDMA, CDMA 2000, WCDMA, GSM1800 and parts of LTE. Furthermore, the design achieves a simple configuration and an excellent linearity performance. The measured ACPR is better than −40 dBc when the amplifier is driven with 10-MHz QPSK signal, without external linearity enhancement technology.

2. THE PROPOSED CIRCUIT AND DESIGN APPROACH

The circuit configuration of the proposed broadband Doherty power amplifier (DPA) is shown in Figure 1(a). Two 10-W commercial transistors in GaN technology are used as the carrier power amplifier and the peak one. The bias and stability networks of the two PAs are correspondingly identical. The matching networks are carefully regulated when they are bias at Class AB and Class C, respectively. A novel coupled-line coupler in [18] is synthesized as an uneven power-dividing splitter. Its basic configuration is shown in Figure 1(b). A compensation network is proposed in this paper and set at the output-end of the peak PA, as shown in Figure 1(a). This compensation network consists of series transmission lines and a shunt capacitance (C_0). The combined branch includes two traditional quarter-wave impedance inverters with different characteristic impedance (R_1, R_2). In the following sub-sections, the detailed design approach is discussed.

2.1. Matching Networks

The carrier power amplifier (CPA) and peak power amplifier (PPA) both employ a 10-W commercial packaged device on GaN technology from Cree Inc. As a consequence, the corresponding bias and stability networks of CPA and PPA could be identical, which significantly reduced the complexity of design. After comparing different topologies for broadband matching networks, we decided to use microstrip lines shunted with capacitances as the matching network because this topology allowed optimized harmonic loads at different frequency via computer-aided tool. It means that we can make a tradeoff between efficiency and linearity for a broadband performance. Taking center frequency (1.75 GHz) for example, the impedances at 2nd harmonic and 3rd harmonic frequency are 1.75 Ω and 429.8 Ω, respectively, which rectified the waveforms of voltage and current, thus improving the efficiency by reducing the internal power dissipation. Conversely, at other frequency points, the harmonic impedances are optimized for better linearity. In a word, with this matching methodology, we have a space to balance the overall performance when considering the overall broadband performance as a priority.

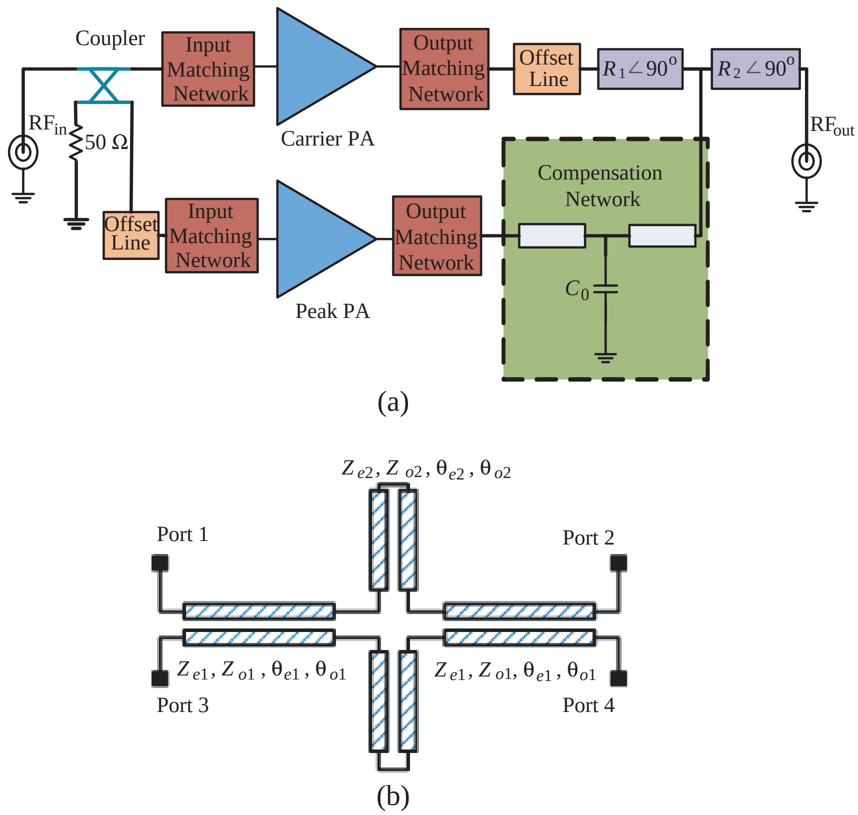

Figure 1. The circuit configuration of (a) the proposed broadband Doherty PA, (b) the novel coupler proposed in [18].

2.2. Quarter-Wave Impedance Inverters and the Proposed Compensation Network

The typical quarter-wave impedance inverter lines (IIL) at the output combined branch is applied to reduce the design complexity. The feasibility of the quarter-wave IIL in broadband application has been experimentally validated in [9]. It is worth mentioning that the narrowband characteristic of the quarter-wave IIL can lead to an imperfect load modulation, which would deteriorate the overall performance, especially the ideal efficiency improvement at 6 dB back-off power at off-center frequency points.

As shown in Figure 1(a), a compensation network, consisting of series transmission lines and a shunt capacitance (C_0), is set at the PPA output-end. The principle of this methodology is based on that in [19], where the microstrip line equals to a virtual open stub in low-power region. In this work, a shunt capacitance is added on the virtual open stub. The value and position of the capacitance, the configuration of the microstrip lines can be carefully optimized to guarantee the high load impedance of the PPA at the low-power region in a broad band. As a consequence, the limited bandwidth brought by the traditional offset line is compensated, while simultaneously the PPA saturated output power is inevitably reduced. However, the broadband performance (measured fractional bandwidth of 51.4%) is guaranteed and realized in such a simple way.

2.3. Broadband Coupler

In this work, a novel symmetrical coupler maintaining tight-coupling performance of 3-dB given in [18], is redesigned to achieve an uneven coupling characteristic. The basic configuration of the coupler is illustrated in Figure 1(b). The proposed coupler obtains a high directivity, a high isolation, a frequency-dependent power-divided ratio and a nearly constant phase difference over a wide bandwidth, all of which benefit this power-amplifier design.

This novel coupler can improve the input matching, optimizing the single amplifier broadband performance regardless of the input matching network. Besides, it achieves a broadband uneven power-divided characteristic which is an advantage in Doherty power-amplifier design. We adopted the strategy that more power is transmitted to the PPA in order to compensate the degradation of the drain current and the soft turn-on effect, which has been theoretically analysis and experimentally confirmed in [20, 21]. Typically, the input power is uneven divided and transmitted to carrier and peak power amplifier at a ratio of 1/2 at the center frequency. Furthermore, the relatively constant phase difference (about 98°) enables a simple phase-compensated offset line and a potential linearity performance. The feasibility of the proposed coupler in [18] as an uneven power-dividing splitter in broadband applications is experimentally validated in this work.

In design and implementation, we set the value and position of C_0, width and length of the microstrip lines in compensation network, configuration of offset lines and gate bias of PPA ($V_{p,G}$) as "tuning knobs". The specifications of the DPA performance are interdependent, so we need to make a tradeoff for broadband performance. With the Agilent ADS optimizing tool, we obtain the values of the variations. The experimental results are illustrated in the next section.

3. EXPERIMENTAL RESULTS

The photo of the proposed Doherty power amplifier circuit is illustrated in Figure 2, where each section mentioned above is marked. In this work, the proposed Doherty power amplifier is implemented on the substrate of Rogers 4350B, the ε_r of which is 3.48. The size of the circuit plane is 13 cm × 7.5 cm. The carrier and peak PAs both adopt the 10 W commercial transistor (CGH40010) in GaN technology from Cree Inc.. The matching networks are similar, consisting of series microstrip lines with shunted Murata capacitances. In this coupled-line coupler shown in Figure 1(b), the port 1 is an input termination; the port 2 and port 3 are connected to the CPA and PPA, respectively; the port 4 is an isolation termination that connects to a 50 Ω grounded resistor. The compensation network includes a shunt capacitance and series transmission lines. The value and position of the capacitance has been manually regulated according to the tradeoff design. The following measured results validate the broadband performance of the proposed Doherty power amplifier.

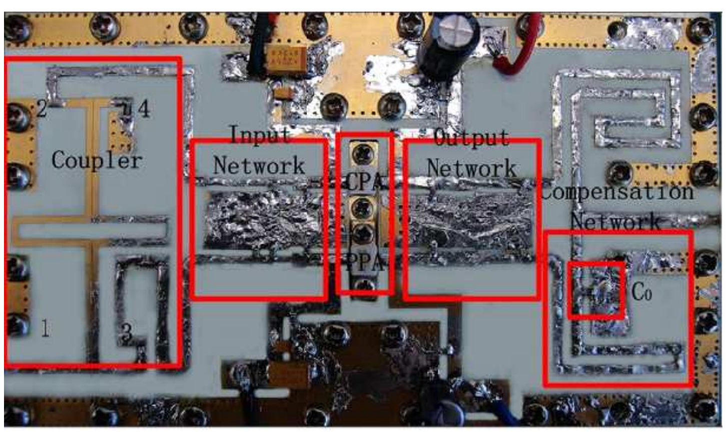

Figure 2. Configuration of the practical wide-band Doherty power amplifier circuit.

3.1. Small-Signal Measurement

In this sub-section, S-parameters of the PAs and coupler are presented. The feasibilities of the matching networks, coupler, and the compensation network are experimentally validated, respectively.

First of all, the small-signal characteristics of a single PA in this circuit plane are presented in order to verify the feasibility of the matching networks. The measurement reveals that the S-parameters of PAs (CPA and PPA) are highly similar when both biased at class-AB operations. For simplification,

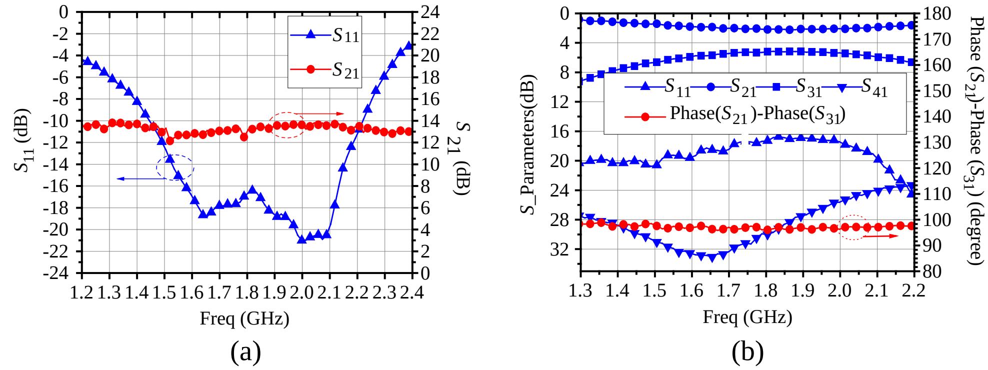

Figure 3. Measured small-signal S-parameters of (a) single power amplifier (CPA or PPA) biased at class-AB condition, (b) microstrip coupled-line coupler.

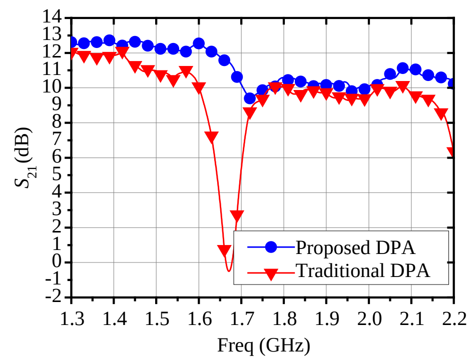

Figure 4. The measured S_{21} of the proposed DPA and the traditional DPA (without compensation network).

we present the S-parameters of CPA in Figure 3(a). The frequency bandwidth, in which S_{11} is under -10 dB, is about 800 MHz, from 1.4 GHz to 2.2 GHz. The S_{21} in desired band is from 12.1 dB to 13.8 dB (a flatness of less than 2-dB).

Then in Figure 3(b), the S-parameters of the practical coupler circuit are illustrated to validate its ability to support broadband performance. Obviously, it achieves a high isolation and a good input return loss coefficient — that is, the S_{11} and S_{41} are both under -16 dB. From the measured results of both S_{21} and S_{31} we can infer an uneven power-dividing characteristic of the coupler. The power-dividing ratio frequency-dependently varies from 1/6.3 to 1/2.

Finally the S_{21} curves of the proposed DPA and the traditional DPA without compensation network are presented in Figure 4. This comparison is used to verify the feasibility of the proposed compensation network. The S_{21} curve of the DPA without compensation network has a noticeable "gap" between 1.6 GHz and 1.7 GHz, revealing a narrowband performance. On the other hand, the proposed DPA achieves a higher gain over the broadband and significantly eliminates the "gap". It is proved that the compensation network significantly contributes to the broadband performance.

3.2. Large-Signal Measurement

In this sub-section, the measured peak output power and efficiency are presented. The testing wave is CW at every hundred megahertz frequency from 1.3 GHz to 2.2 GHz.

In Table 1, the peak output power of the proposed DPA and the traditional DPA (without the compensation network) is illustrated. The calculated average power of the DPA without compensation network is 41.5 dBm, and the peak output powerless than 41 dBm locates from 1.3 GHz to 1.7 GHz, which can be regarded as a fail operation. So the calculated fractional bandwidth of the traditional

Table 1. Measured peak output power of the proposed DPA and the traditional DPA (without compensation network).

Frequency (MHz)	Peak output power (traditional DPA) (dBm)	Peak output power (proposed DPA) (dBm)
1300	40	41.3
1400	39	42
1500	40	42.2
1600	40.8	42.1
1700	N/A	42.4
1800	44	42.1
1900	43.8	42
2000	43.7	42
2100	41.2	41.9
2200	41	42
Average power	41.5	42

DPA is only about 20%. Conversely, the proposed DPA achieves an average peak output power of 42 dBm. More than 41 dBm peak output power is achieved at every measured frequency point while no one reaches 43 dBm. Obviously, the peak output power is sacrificed in order to pursue a broadband performance. The calculated fractional bandwidth of the proposed DPA is about 51.4% which as to our best acknowledge, realizes the widest fractional bandwidth.

Figure 5 illustrates the gain vs. output power at the selected frequency points. A calculated average gain of 10.2 dB is observed when the saturation effects do not occur.

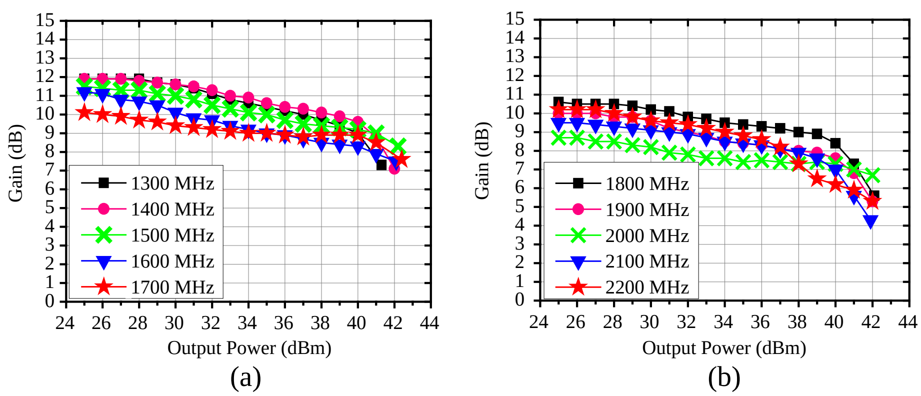

Figure 5. Measured gain vs. output power at (a) 1300 MHz–1700 MHz, (b) 1800 MHz–2200 MHz.

The drain efficiency vs. output power at the selected frequency points is presented in Figure 6. The DPA obtains an average peak and 6 dB back-off efficiency of 48.4% and 32.8%, respectively, when calculated among the selected frequency points. The output back-off (OBO) varies due to the imperfect load modulation. However, the feasibility of the proposed DPA in broadband application can be firmly validated.

3.3. Linearity Measurement

In this sub-section, the linearity performance of the proposed DPA is presented in Figure 7. The ACPR is better than −40 dBc at the average output power of 37 dBm, when driven with the 10 MHz QPSK signal, of which the center frequency is 1.95 GHz, and the peak-to-average power ratio is 5 dB, without

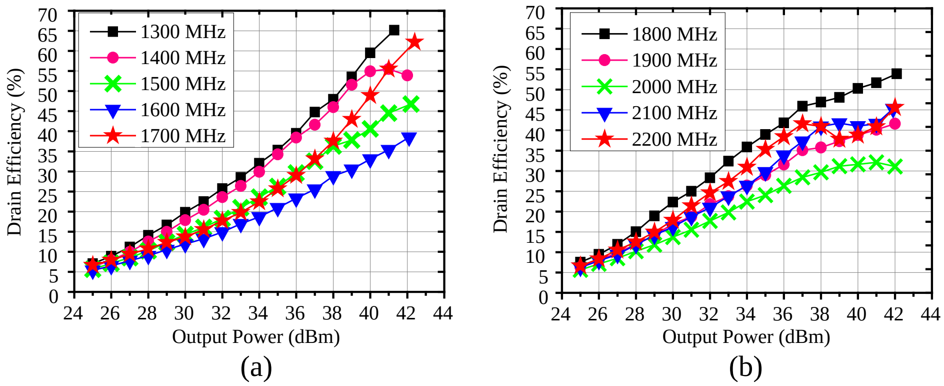

Figure 6. Measured efficiency vs. output power at (a) 1300 MHz–1700 MHz, (b) 1800 MHz–2200 MHz.

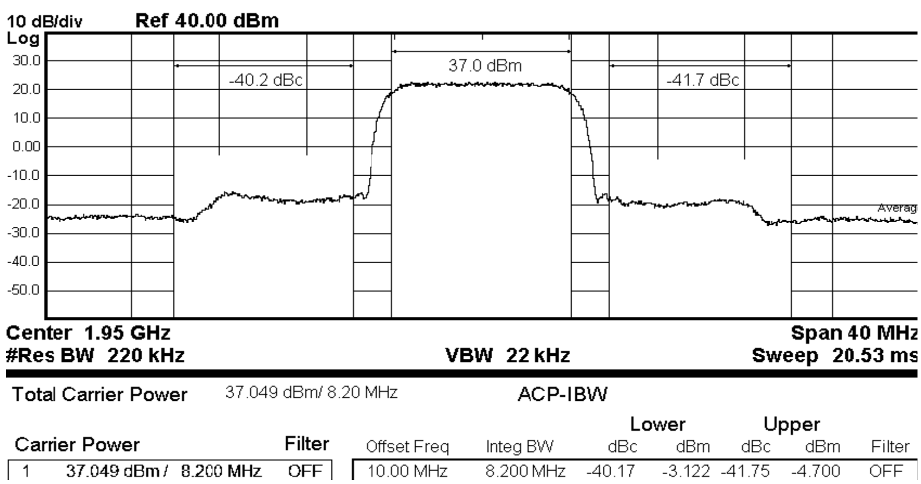

Figure 7. The measured spectra of the proposed DPA at an average output power of 37 dBm.

Table 2. Comparison with the state-of-the-art broadband Doherty power amplifier.

	Fractional BW (%)	f_0 (GHz)	Peak Power/BOL (dBm)	η_{avg} @ OPBO (%)	ACPR (dBc)/Signal
[9]	35	1.82	43 (6-dB)	38	−36/WCDMA @ 2.14 GHz
[10]	35.3	0.85	49.9 (6-dB)	60.6	−29.57/WCDMA @ 880 MHz
[11]	22	7.65	35 (9-dB)	38	−50/256-QAM @ 7.5 GHz
[12]	18.2	3.3	43 (6-dB)	47	N/A
[13]	22.6	2.21	44 (6-dB)	44.2	−27/LTE @ 2.22 GHz
[15]	36	2.01	41 (6-dB)	47	−30/LTE @ 2 GHz
[17]	40	1.0	40.2–42.9 (6-dB)	(PAE) 30.3–40.1	N/A
This work	51.4	1.75	42 (6-dB)	32.8	Better than −40/QPSK @ 1.95 GHz

∗OPBO: Output Power in Back-Off
∗BOL: Back-Off Level

external linearity enhancement methods. Additionally, the ACPR is better than −30 dBc when the center frequency approximately ranges from 1.75 GHz to 2.14 GHz. In other working frequency regions, the ACPR deteriorates and further linearity enhancement technologies need to be synthesized, such as digital pre-distortion. In a word, the proposed DPA is experimentally validated to achieve a good linearity performance in a relatively wide bandwidth.

3.4. Bandwidth Comparison

In Table 2, the proposed Doherty power amplifier and the state-of-the-art broadband Doherty power amplifiers are compared. To author's best acknowledge, the DPA in this work has **the widest fractional bandwidth**. The proposed Doherty power amplifier achieves an average saturated output power of 42 dBm, an average gain of 10.6 dB, an average peak and 6-dB back-off efficiency of 48.4% and 32.8%, respectively, and a fractional bandwidth of 51.4%, from 1.3 GHz to 2.2 GHz. It is demonstrated that the Doherty power amplifier performs well in a broad bandwidth.

4. CONCLUSIONS

A tradeoff design of broadband Doherty power amplifier on GaN technology is presented in this paper. A novel coupled-line coupler is optimized and synthesized in the circuit as an uneven input power splitter. The feasibility of the coupler in broadband application is experimentally confirmed. The broadband matching networks consist of series microstrip lines and shunted capacitances. In order to avoid power leakage when the Doherty power amplifier is operating in low-power region, a compensation network is proposed and set at the output-end of the peak power amplifier. The value of the capacitances, length and width of the microstrip lines, gate biased voltage can be set as "tuning knobs" that confirmed with the ADS tools. A tradeoff among the certain specifications of the Doherty power amplifier, like peak output power, efficiency, bandwidth and linearity performance, is achieved through optimizing the "tuning knobs". Although the narrowband characteristic of the traditional impedance inverter lines can deteriorate the overall power-amplifier performance in broadband application, the wide-band applications of the traditional impedance inverter lines after adding the proposed compensation network has been experimentally validated in this paper. It can be expected that this proposed new wide-band Doherty power amplifier with high-performance can be widely used in practical wireless communication systems.

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