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Implementation of a PLDRO with a Fractional Multiple Frequency of Reference

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Abstract—A PLDRO (Phase Locked Dielectric Resonator Oscillator) with the output frequency of a fractional multiple of reference is proposed and implemented. The key element in the proposed PLDRO is an image rejection mixer placed between a VCDRO (Voltage Controlled Dielectric Resonator Oscillator) and SPD (Sampling Phase Detector). The image rejection mixer shifts the coupled signal from the VCDRO before the signal feeds the SPD. Therefore, the output frequency of the PLDRO can be realized such that it is not harmonically related with its reference frequency. The frequency divider and multiplier generate the IF frequency for the mixer from the reference frequency. The general PLL (Phase Locked Loop) design parameters such as the damping coefficient and the natural frequency are derived for the proposed topology of the PLDRO. A 7.25 GHz PLDRO with a 100 MHz reference, intended for use as a local oscillator for a ka band Block-up Converter (BUC), is designed and measured. A BJT (Bipolar Junction Transistor) is used as an active component of the VCDRO and a modified two micro-strip line coupled DR model is presented and used for frequency tuning range estimation. The measured phase noise at 10 kHz/100 kHz offset is 101 dBc/Hz and 115 dBc/Hz, respectively. The fabricated PLDRO size is 100 mm by 105 mm by 23 mm including a 100 MHz reference crystal oscillator.

1. INTRODUCTION

In microwave communication systems such as satellite ground terminals, the phase noise of the local oscillator is required to be increasingly lower as the demand for large data transmission such as video signal rises. In order to accommodate this demand, higher frequency bands such as the ka band are currently receiving more attention, as lower frequency bands are nearly saturated. The PLDRO is the most widely used for a local oscillator for such high frequency bands due to its superior phase noise characteristics compared with the PLL IC based approach. Millimeter wave SiGe based integer-N PLL IC phase noise performance has recently improved substantially [1–3], but fractional PLL with the same technology still shows inadequate performance compared with its integer counterpart, i.e., about 90 dB in-band phase noise and less than 70 dB spurious [4, 5].

This paper presents a PLDRO structure that has output frequency that is not an integer multiple of the reference frequency, and verifies the structure by analyses and experiments. With this structure, theoretically arbitrary output frequency can be realized from the same reference such as a 100 MHz crystal oscillator. The conventional PLDRO uses a reference crystal oscillator and a SPD, which compares the harmonic frequency of the reference and the feedback signal from VCDRO to generate an error signal for the loop filter [6]. As a variation, the fundamental VCDRO is replaced with a push-push VCDRO [7, 8], and the SPD is replaced with a mixer [8]. However, the aforementioned PLDROs have the same limit: the output frequency must be an integer multiple of the reference frequency, typically 100 MHz. Accordingly, if output frequency that is not an integer multiple of the 100 MHz reference is required, a special frequency crystal oscillator is needed. However, special frequency crystal oscillators

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other than the standard frequency such as 100 MHz must be specially-order-made, as they are not available on the market. Furthermore, the special oscillators are usually inferior to the standard ones in terms of performance, cost, and delivery.

We overcome this drawback of the conventional PLDRO by proposing a PLDRO structure where the output frequency of the PLDRO can be a fractional multiple of the reference (100 MHz) so that technically arbitrary output frequency can be generated from a 100 MHz reference. This paper analyzes the proposed PLL structure and derives the design equation for it. To verify the PLDRO, we designed and fabricated a 7.25 GHz PLDRO using a bipolar transistor, which is intended for use as the local oscillator of a ka band satellite ground terminal block up converter after multiplying it by 4 to realize 29 GHz.

2. PLDRO STRUCTURE

The proposed concept of this PLDRO is to shift the input frequency of the SPD from the output frequency of the VCDRO by a fraction of the reference frequency using an image rejection mixer so that non-reference multiple output frequency can be achieved in the PLDRO. Fig. 1 illustrates the block diagram of the proposed PLDRO structure. The coupled VCDRO output signal acts as an LO for the image rejection mixer, and the fractional frequency of the reference (100 MHz), generated by the consecutive frequency divider and multiplier, acts as an IF for it, resulting in a frequency shift from the VCDRO output by a fractional frequency of the reference. The shifted frequency is further divided by a prescaler to reduce the SPD input frequency, thereby making the SPD matching circuit less sensitive to the external impedance and input power level. While the output frequency of the conventional PLDRO is an integer multiple of the reference frequency, the output frequency of the proposed PLDRO can be not only an integer but also a fractional multiple of the reference frequency. From Fig. 1, the output frequency can be extracted as

$$f_{dro} = \left(P \cdot L \pm \frac{M}{N} \right) f_{ref} \tag{1}$$

where P is the dividing factor of the prescaler, L the multiplying factor of SPD, N the reference divider, and M the reference multiplier. As for the '$\pm$' sign in front of the fractional part $\frac{M}{N}$, '+' denotes a frequency down shift (LSB) and '$-$' indicates a frequency up shift (USB) at the image rejection mixer. By choosing proper values of P, L, M, N, and the sign of the fractional part, we can implement an arbitrary frequency output with the same reference input, such as the most commonly used 100 MHz crystal oscillator. $F(s)$ in Fig. 1 represents the transfer function of the commonly used second order type II loop filter, which is an integrator with phase lead circuit.

$$F(s) = \frac{1 + s\tau_2}{s\tau_1}, \qquad \tau_1 = R_1 C, \quad \tau_2 = R_2 C \tag{2}$$

This is physically realized with an operational amplifier, as shown in Fig. 2.

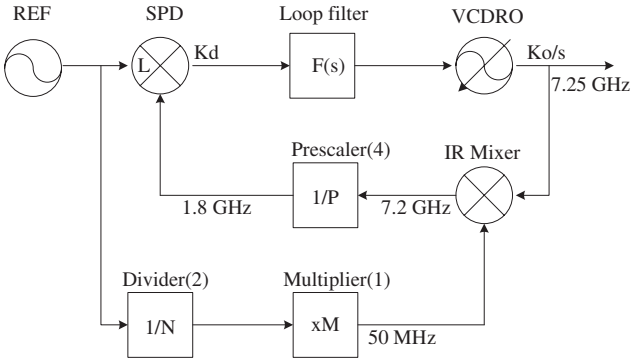


Figure 1. The proposed PLDRO block diagram.

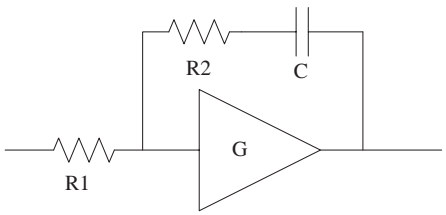


Figure 2. Active loop filter for type II second order PLL, an integrator with a phase lead circuit.

By applying Mason's rule to the block diagram, the closed loop transfer function of the proposed PLDRO can be expressed as in (3), where K_d is SPD's phase detector gain in V/rad, and K_0 is the VCDRO gain in Hz/V. After mathematical manipulation, the final form of the closed loop transfer function is obtained.

$$H(s) = \frac{LK_dF(s)K_0/s \pm \frac{M}{NP}K_dF(s)K_0/s}{1 + K_dF(s)K_0/Ps} \tag{3}$$

$$H(s) = \left(PL \pm \frac{M}{N}\right)\frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4}$$

$$\omega_n = \sqrt{\frac{K_dK_o}{\tau_1 P}}, \quad \zeta = \frac{\tau_2\omega_n}{2} \tag{5}$$

Hence, by choosing the damping coefficient and optimum 3 dB bandwidth, ζ and $\omega_{3\,\mathrm{dB}}$, in (6), we can determine the loop filter parameters, such as τ_1 and τ_2, from (5).

$$\omega_n = \frac{\omega_{3\,\mathrm{dB}}}{\sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2+1)^2 + 1}}} \tag{6}$$

3. PLDRO IMPLEMENTATION

We implemented a 7.25 GHz PLDRO according to the proposed PLDRO structure, which is intended to be used as a local oscillator for a ka-band block up converter by multiplying it by 4 so that its output frequency will be 29 GHz. In this case, to realize 7.25 GHz output frequency from the 100 MHz reference, we choose $P = 4$, $M = 1$, $N = 2$, $L = 18$, and LSB, respectively. The coupled 100 MHz reference is divided by 2 ($N = 2$) to become 50 MHz and low pass filtered ($M = 1$) without a multiplier. The coupled 7.25 GHz VCDRO output is lower shifted (LSB, +) by 50 MHz to become 7.2 GHz, and the successive prescaler divides 7.2 GHz by 4 ($P = 4$), realizing 1.8 GHz ($L = 18$) as the SPD input. We chose a damping coefficient $\zeta = 1$ for good loop stability, and optimize the 3 dB bandwidth for optimal phase noise. Fig. 3 shows the 7.25 GHz voltage controlled DRO schematic. We used a silicon RF npn transistor, which has better close to carrier phase noise than that of the FET, as an active component. The emitter stub TL1 makes the transistor unstable, and the output matching circuit TL2 and TL3 are adjusted for the transistor to have sufficient positive input reflection to a DR (Dielectric Resonator) at the frequency of 7.25 GHz. The DR is placed where the phase of the input reflection coefficient of the active component is zero at 7.25 GHz.

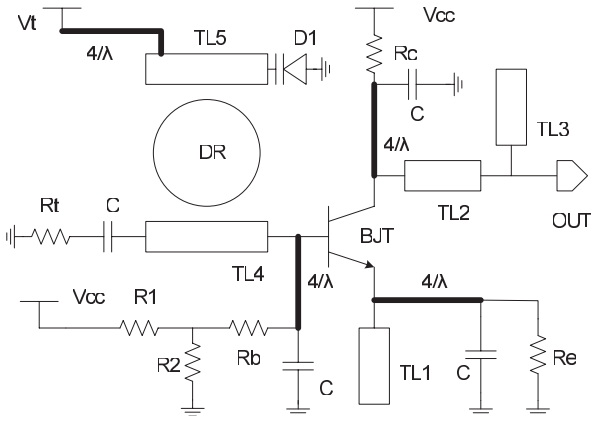
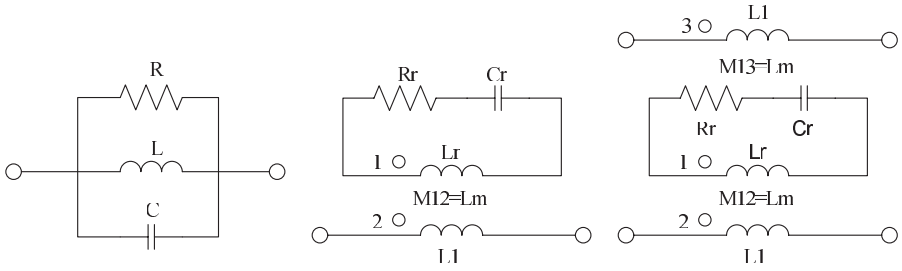


Figure 3. Voltage controlled DRO schematic.

The dielectric resonator coupled with two micro-strip lines, TL4 and TL5, is modeled to estimate the VCDRO frequency range. The resonance frequency is changed by the coupled reactance of the varactor diode, which is changed by the tuning voltage change (Vt). We first extracted the simple



(a) DR model (b) one MS coupled DR model (c) two MS coupled DR model

Figure 4. Two Micro-strip coupled DR model.

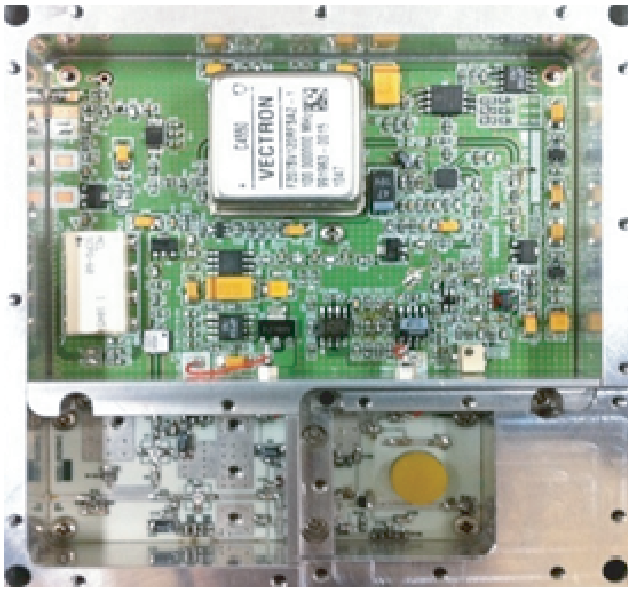


Figure 5. The implemented 7.25 GHz PLDRO ($100 \times 105 \times 23\,\text{mm}^3$).

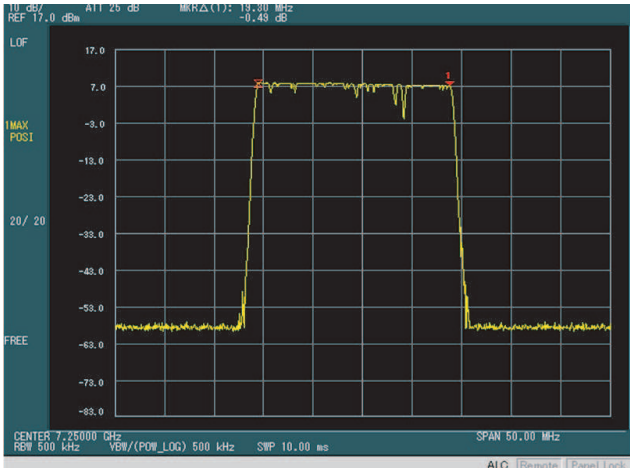


Figure 6. The VCO tuning range (19 MHz).

resonator model (a) in Fig. 4 for the single micro-strip coupled DR using the program supported by the DR manufacturer, and changed it into (b) [9]. Finally, we modified (b) into (c). Because the two coupling gaps from TL4 and TL5 are the same, and we used the same mutual inductance Lm and L1 values for both sides. Using the modified model, the length of TL5 is adjusted to achieve adequate tuning bandwidth, such as more than 10 MHz. The total design was verified in a non-linear simulator and physically implemented. The implemented PLDRO has a size of $100 \times 105 \times 23\,\text{mm}^3$ as shown in Fig. 5. The DRO circuits are implemented on the RO4003 20 mil substrate. The 100 MHz reference oscillator, sub-harmonic mixer with coupler, dividers, and loop filter are placed separately on a 4-layered FR4.

4. PLDRO MEASUREMENT

With the initial length of the TL5 in Fig. 3 using the two micro-strip coupled DR model in Fig. 4 and the final adjustment during the measurement, the VCDRO has the frequency tuning range about 19 MHz shown in Fig. 6, which is wide enough for PLL implementation. The power variation between the lowest and highest frequencies is about 0.5 dB.

Figure 7 shows the implemented PLDRO phase noise measurement at 7.25 GHz. The measured phase noise is 101 dBc/Hz and 115 dBc/Hz at 10 kHz and 100 kHz, respectively. From Table 1, they are expected to have at least 8 dB better phase noise than that defined in the Intelsat earth station

Table 1. Phase noise comparison between measured 7.25 GHz, estimated 29 GHz, and IESS-308. Phase noise at 29 GHz is calculated as the phase noise at 7.25 GHz plus $(20 \log 4 + 1)$.

Offset freq.	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz
7.25 GHz (measured)	53 dBc	81 dBc	104 dBc	101 dBc	115 dBc
29 GHz (estimated)	40 dBc	68 dBc	91 dBc	88 dBc	102 dBc
IESS-308	30 dBc	60 dBc	70 dBc	80 dBc	90 dBc

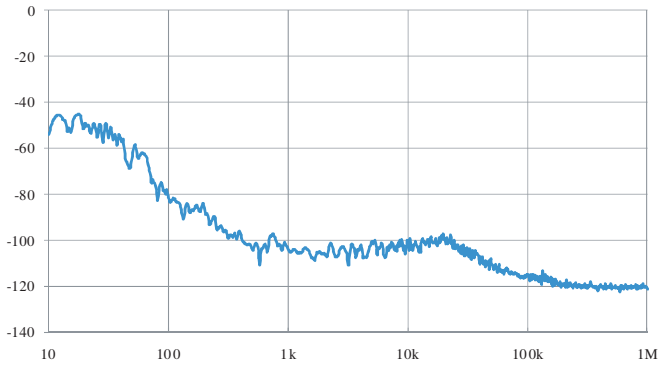


Figure 7. Implemented 7.25 GHz PLDRO phase noise plot.

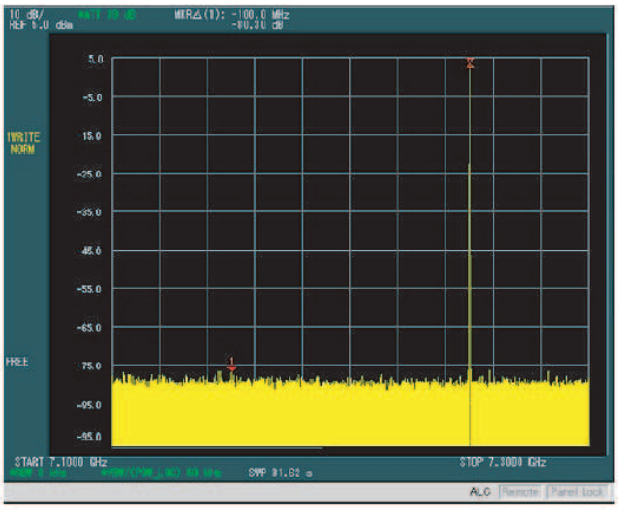


Figure 8. Implemented 7.25 GHz PLDRO output spurious level (80 dBc).

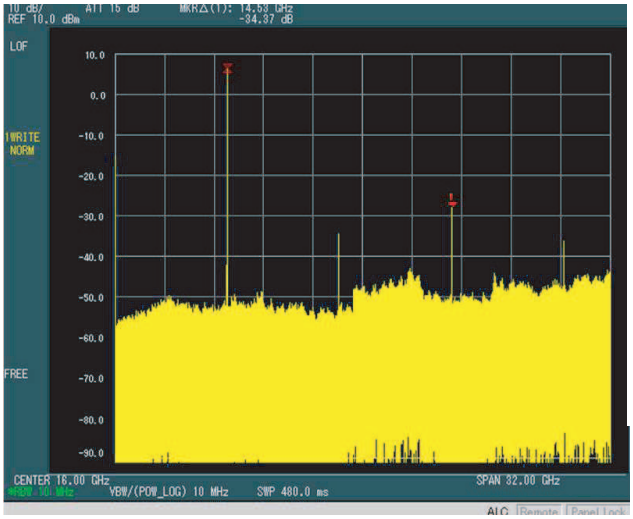


Figure 9. The harmonics of the PLDRO (Third harmonic: 34 dBc).

standards, IESS-308 [10], even after being multiplied by 4 to realize 29 GHz for ka-band BUC application. Table 1 compares the measured phase noise of 7.25 GHz, the estimated phase noise of 29 GHz after multiplication, and the phase noise defined in IESS-308. The additional current consumption from the LO Amp and the frequency divider is about 56 mA.

The spurious level 100 MHz away from the output frequency in Fig. 8 is caused by the coupling between 100 MHz in the FR-4 board and active parts in the RO4003 board such as the buffer amplifier and oscillator. The resulting level is about 80 dBc.

In Fig. 9, the third-order harmonic power, which is the largest among all the harmonics, is below 34 dBc from the fundamental. The second and fourth harmonics are below 40 dBc.

5. CONCLUSION

This paper proposes a PLDRO configuration that has an output frequency of the fractional multiple of the reference input frequency. We shifted the phase detector input frequency by a fractional multiple of the reference using an image rejection mixer. As a result, the local oscillator does not need to be bound to the reference frequency, and the reference frequency does not need to be specially made according to the required local oscillator frequency, in contrast with the conventional PLDRO. The measurement results show that this PLDRO offers a sufficient phase noise margin (at least 8 dB) for ka-band ground terminal block up converter application. This PLDRO concept will lend much greater flexibility to future mm-wave communication system design where a PLDRO is to be used.

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