Ultra-Wideband Four-Way In-Phase Multilayer Power Divider with High Isolation

Long Xiao^{*}, Hao Peng, and Tao Yang

Abstract—A novel ultra-wideband four-way in-phase multilayer power divider based on the microstripto-slotline transition is proposed in this paper as a complemental slotline power divider with high isolation. Due to the introduction of three lumped isolation resistors, the isolations between output ports in the new structure have been improved. The design expressions have been derived by making use of odd-mode and even-mode method. Both simulated and measured results have proved that the proposed power divider has good impedance matching at all ports, high isolations between output ports, excellent amplitude and phase balance, as well as flat group delay over the wide frequency range from 3.8 GHz to 11 GHz.

1. INTRODUCTION

Since the ultra-wideband (UWB) spectrum was determined in 2002, a large number of devices and components have been designed [1–11]. UWB power divider, which is an indispensable passive components, plays an important role in the microwave and RF systems. To obtain an 180° out-of-phase signal division in a wide frequency range, an UWB power divider based on a T-junction consisting of a microstrip line and slotline was proposed in [4]. In [1], a compact non-complanar power divider based on microstrip-to slotline transition was designed, which introduced two circular stubs as implemental circuit that connect to the ends of output arms to decrease the ripple in the passband. In [6], a tapered transition and a fan-shaped slot were exploited to take the place of a circular slot so that the performances of the improved power divider were better than one designed in [1, 4].

The power dividers proposed in [1-7] have low insertion losses and good return losses. However, the isolations between output ports were not satisfying. Thus, some new power dividers with high isolations based on slotline were proposed [8–11]. In [10], a slot has been processed on the ground plane which separated the ground into two parts, and a resistor bridging over the slot has been introduced to improve the isolations between output ports. Different from the power divider in [10], a via hold located on the substrate has been drilled to contain an isolation resistor that connected to the output branches in [8]. In order to expand the application of UWB power divider, a four-way out-of-phase slotline power divider was proposed in [9].

In this paper, a novel UWB four-way in-phase multilayer power divider based on microstrip-toslotline transition is proposed, which introduces three resistors to increase the isolations between output ports. Both the simulated and measured results have proved that the new four-way power divider with high isolation has good impedance matching, excellent amplitude and phase balance as well as high isolations between output ports.

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^{*} Corresponding author: Long Xiao (XL740512@126.com).

The authors are with the School of Electronic Engineering, University of Electronic Science and Technology of China, Chengdu, Sichuan 611731, China.

2. CIRCUIT DESIGN

The configuration of the proposed four-way power divider with high isolation presented in this paper is shown in Figure 1, which consists of three layers (top layer, middle layer and bottom layer). All the output ports (port 2–port 5) as well as input port (port 1) are located in the top layer. The slot is etched in the middle layer, namely ground plane. And two branches of the first-order power divider are located in the bottom layer.

This new power divider employs microstrip-to-slotline transition to realize the goal of distributing power equally. Three resistors are employed to improve the isolations between output ports. Moreover, three radial stubs are placed at the ends of microstrip lines, and six circular stubs are placed at the ends of slotlines. No matter the radial stubs or the circular stubs, all of them act as compensating circuits. Their equivalent lengths are a quarter of λ_m and λ_{s1} (or λ_{s2}). λ_m and λ_{s1} (or λ_{s2}) stand for the guided

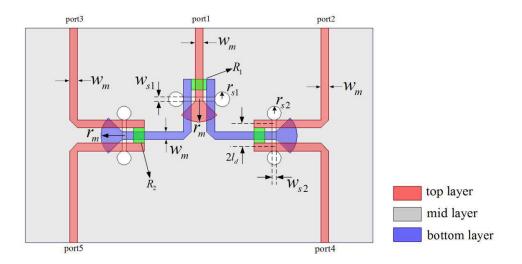


Figure 1. Configuration of the proposed UWB four-way in-phase multiplayer power divider with high isolation.

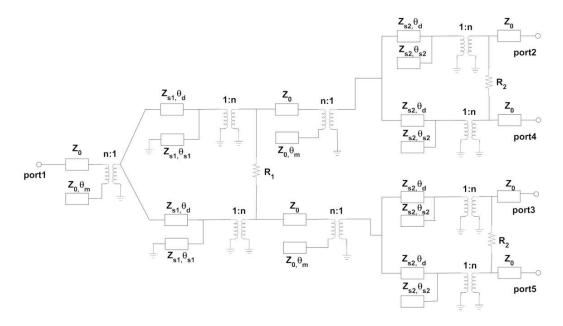


Figure 2. Equivalent circuit of the proposed UWB four-way in-phase multiplayer power divider with high isolation.

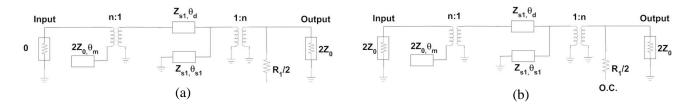


Figure 3. The first order power dividing. (a) Odd-mode circuit model. (b) Even-mode circuit model.

wavelength of microstrip line and guided wavelength of slotline at the center frequency, respectively.

Because of the symmetrical structure, the power divider proposed in this paper can employ oddmode and even-mode analysis method. Its equivalent circuit is shown in Figure 2, where θ_m , θ_{s1} , θ_{s2} and θ_d represent the equivalent electrical length $\lambda_m/4$, $\lambda_{s1}/4$, $\lambda_{s2}/4$ and l_d , respectively. Figure 3 shows the equivalent circuits of the first-order power divider (including port 1). Figure 3(a) exhibits the odd-mode equivalent circuit. In order to obtain good impedance matching and excellent isolations between output ports locating on both sides of the input port (port 1) like port 2 and port 3, the following expression must be satisfied.

$$\frac{1}{R_{1}} = \frac{n^{4}Z_{s1}^{2}\tan\theta_{s1}\tan\theta_{d} - j2n^{2}Z_{s1}Z_{0}\tan\theta_{d} - j2n^{2}Z_{s1}Z_{0}\tan\theta_{s1}}{4n^{2}Z_{s1}Z_{0}\tan\theta_{s1}(n^{2}Z_{s1}\tan\theta_{d} - 2Z_{0}\cot\theta_{m})} + \frac{-j4Z_{0}^{2}\tan\theta_{s1}\tan\theta_{d}\cot\theta_{m} - 2n^{2}Z_{s1}Z_{0}\tan\theta_{s1}\cot\theta_{m} + j4Z_{0}^{2}\cot\theta_{m}}{4n^{2}Z_{s1}Z_{0}\tan\theta_{s1}(n^{2}Z_{s1}\tan\theta_{d} - 2Z_{0}\cot\theta_{m})}$$
(1)

Because $\theta_m = 90^\circ$, $\theta_{s1} = 90^\circ$, and the value of θ_d is small, namely $\cot \theta_m = 0$ and $\tan \theta_{s1} \gg \tan \theta_d$, equivalent (1) can be simplified as:

$$\frac{1}{R_1} \approx \frac{n^2 Z_{s1} \tan \theta_d - j2Z_0}{4n^2 Z_{s1} Z_0 \tan \theta_d}$$

Considering that resistor is a real number, the value of R_1 is selected as:

$$R_1 \approx 4Z_0 \tag{2}$$

Here, the transformer turn ratio n stands for the coupling coefficient between slotline and microstrip line, which can be derived according to [12] as following:

$$n = \frac{J_0(k_{es}W_m/2)J_0(k_{em}W_s/2)}{k_{es}^2 + k_{em}^2} \cdot \left(\frac{k_{es}^2k_1}{k_1\cos k_1h + k_2\sin k_1h} + \frac{k_{em}^2k_2\varepsilon_r}{k_2\varepsilon_r\cos k_1h - k_1\sin k_1h}\right)$$
(3)

where $J_0(\cdot)$ is the zeroth-order Bessel function and

$$k_{1} = \sqrt{\left|k_{0}^{2}\varepsilon_{r} - k_{es}^{2} - k_{em}^{2}\right|} = k_{0}\sqrt{\left|\varepsilon_{r} - \varepsilon_{res} - \varepsilon_{rem}\right|};$$

$$k_{2} = k_{0}\sqrt{\left|\varepsilon_{res} + \varepsilon_{rem} - 1\right|};$$

$$k_{es} = k_{0}\sqrt{\varepsilon_{res}}; \quad k_{em} = k_{0}\sqrt{\varepsilon_{rem}};$$

 ε_{rem} and ε_{res} , which are confined according to [12], represent the effective dielectric constants of microstrip line and slotline, respectively.

Figure 3(b) exhibits the even-mode equivalent circuit of the first-order power divider. In order to obtain good even-mode impedance matching, the characteristic impedance of slotline Z_{s1} must satisfy the following expression.

$$2Z_0 = \frac{n^2 Z_{s1} \left(j n^2 Z_{s1} \tan \theta_{s1} \tan \theta_d + 2Z_0 \tan \theta_{s1} + 2Z_0 \tan \theta_d \right)}{j 2Z_0 \tan \theta_{s1} \tan \theta_d + n^2 Z_{s1} \tan \theta_{s1} - j 2Z_0} \tag{4}$$

Since θ_{s1} approximates 90°, and θ_d is a small value, namely $\tan \theta_{s1} \gg \tan \theta_d$, the above equivalent can be simplified as:

$$2Z_0 \approx \frac{n^2 Z_{s1} \left(j n^2 Z_{s1} \tan \theta_d + 2Z_0 \right)}{j 2Z_0 \tan \theta_d + n^2 Z_{s1}}$$

Figure 4. The second order power dividing. (a) Odd-mode circuit model. (b) Even-mode circuit model.

Namely,

$$Z_{s1} \approx \frac{2Z_0}{n^2} \tag{5}$$

The odd-mode equivalent circuit of the second-order power divider is exhibited in Figure 4(a). Similar to the analysis of the first-order power divider, the resistor R_2 must be confined by the following equation.

$$\frac{1}{R_2} = \frac{n^4 Z_{s2}^2 \tan \theta_{s2} \tan \theta_d - j n^2 Z_{s2} Z_0 \tan \theta_d - j n^2 Z_{s2} Z_0 \tan \theta_{s2}}{2n^2 Z_{s2} Z_0 \tan \theta_{s2} (n^2 Z_{s2} \tan \theta_d - 2Z_0 \cot \theta_m)} + \frac{-j 2 Z_0^2 \tan \theta_{s2} \tan \theta_d \cot \theta_m - 2n^2 Z_{s2} Z_0 \tan \theta_{s2} \cot \theta_m + j 2 Z_0^2 \cot \theta_m}{2n^2 Z_{s2} Z_0 \tan \theta_{s2} (n^2 Z_{s2} \tan \theta_d - 2Z_0 \cot \theta_m)}$$
(6)

Because $\theta_m = 90^\circ$, $\theta_{s2} = 90^\circ$, and the value of θ_d is small, namely $\cot \theta_m = 0$ and $\tan \theta_{s2} \gg \tan \theta_d$, equivalent (6) can be simplified as:

$$\frac{1}{R_2} \approx \frac{n^2 Z_{s2} \tan \theta_d - j Z_0}{2n^2 Z_{s2} Z_0 \tan \theta_d}$$

Considering that resistor is a real number, the value of R_2 is selected as:

$$R_2 \approx 2Z_0 \tag{7}$$

Through the analysis of Figure 4(b), expression (8) about Z_{s2} can be derived.

$$Z_0 \approx \frac{n^2 Z_{s2} \left(j n^2 Z_{s2} \tan \theta_d + Z_0 \right) \tan \theta_{s2}}{n^2 Z_{s2} \tan \theta_d + j 2 Z_0 \tan \theta_d \tan \theta_{s2} + n^2 Z_{s2} \tan \theta_{s2} - j 2 Z_0}$$
(8)

Since $\theta_{s2} = 90^{\circ}$ and θ_d is a small value, namely $\tan \theta_{s2} \gg \tan \theta_d$, the above equivalent can be simplified as:

$$Z_0 \approx \frac{n^2 Z_{s2} (j n^2 Z_{s2} \tan \theta_d + Z_0)}{j 2 Z_0 \tan \theta_d + n^2 Z_{s2}}$$

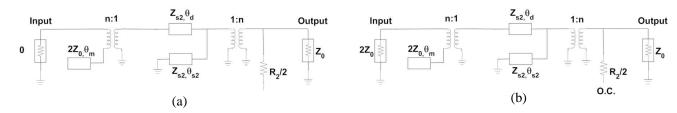
Then,

$$Z_{s2} \approx \frac{\sqrt{2Z_0}}{n^2} \tag{9}$$

Equations (2) and (7) provide a simple guideline to determine the values of isolation resistors R_1 and R_2 so that high isolations between output ports can be obtained. In addition, the dimensions of the four-way in-phase multilayer power divider can also be confined by the above expressions.

3. EXPERIMENTAL RESULTS

The presented UWB four-way in-phase multilayer power divider with high isolation is designed and fabricated on a Rogers 4003C substrate with dielectric constant of 3.38, thickness of 0.508 mm, and loss tangent of 0.0023. The characteristic impedance of microstrip line is 50 Ω . Through optimization by EM simulator HFSS, the final dimensions of the presented four-way power divider with high isolation are listed as following: $w_m = 1.14 \text{ mm}, r_m = 3.6 \text{ mm}, r_{s1} = 1.08 \text{ mm}, w_{s1} = 0.6 \text{ mm}, l_d = 1.68 \text{ mm},$



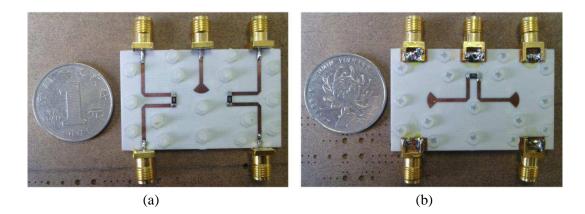


Figure 5. Photograph of the four-way in-phase power divider. (a) Top view. (b) Bottom view.

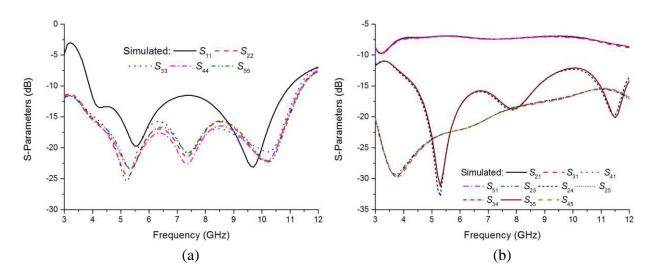


Figure 6. Simulated results. (a) Return loss. (b) Insertion loss.

 $R_1 = 200 \Omega$, $R_2 = 100 \Omega$, $r_{s2} = 1.0 \text{ mm}$, $w_{s2} = 0.6 \text{ mm}$. Figure 5 shows a photograph of the fabricated four-way in-phase multiplayer power divider with high isolation. The whole size of the power divider is $30 \text{ mm} \times 50 \text{ mm}$.

The simulated and measured results of the proposed four-way power divider with high isolation are exhibited in Figure 6, Figure 7 and Figure 8. It is obvious that the measured results show a good agreement with the simulated ones in the wide working frequency range. The simulated and measured 10 dB return loss bandwidths of input port, namely S_{11} , are about 7.2 GHz (from 3.8 GHz to 11 GHz) and 7.5 GHz (from 3.7 GHz to 11.2 GHz), respectively. The measured return losses of outputs ports S_{22} , S_{33} , S_{44} and S_{55} are better than 12 dB in the frequency range from 4 GHz to 11 GHz, while the simulated ones are better than 15 dB in the same frequency band, which are shown in Figure 6(a) and Figure 7(a).

Figure 6(b) and Figure 7(b) exhibit the simulated and measured insertion losses of all the input and output ports and the isolations between output ports. The simulated insertion losses S_{21} , S_{31} , S_{41} and S_{51} are within $7.2 \pm 0.3 \,\mathrm{dB}$ in a wide frequency range from 4 GHz to 10 GHz, while the measured insertion losses are within $7.5 \pm 0.5 \,\mathrm{dB}$. The measured isolations S_{24} and S_{35} are better than 10 dB in the range from 4 GHz to 12 GHz, while the simulated ones are better than 12 dB. In addition, the other simulated and measured isolations S_{23} , S_{25} , S_{34} and S_{45} are better than 15 dB and 14 dB over frequency range 3 GHz-12 GHz, respectively.

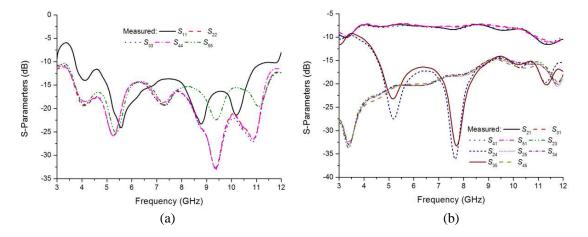


Figure 7. Measured results. (a) Return loss. (b) Insertion loss.

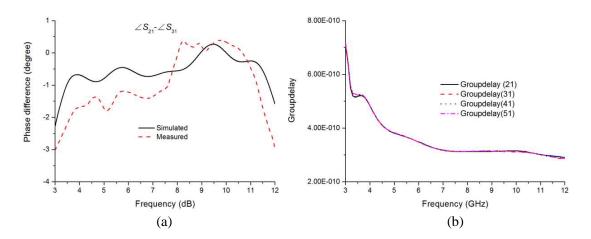


Figure 8. (a) Simulated and measured phase difference. (b) Measured group delay.

Figure 8(a) exhibits the phase difference between output port 2 and port 3, which represents the phase balance of the power divider. The measured result is within $0^{\circ} \pm 1^{\circ}$ from 4 GHz to 11 GHz, which shows good agreement with simulated one. Moreover, it is easy to find that the group delay is very flat as shown in Figure 8(b).

4. CONCLUSION

A new ultra-wideband four-way in-phase multiplayer power divider with high isolation has been proposed. Three isolation resistors have been introduced to increase the isolations between output ports. Equivalent circuits have also been constructed to determine the dimensions of the power divider. The simulated and measured results exhibit a good agreement. The results also indicate that the presented four-way power divider shows good input and output impedance matching, high isolations between output ports, as well as excellent amplitude and phase balance at output ports in a wide frequency range.

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