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A Miniaturized Gysel Power Divider/Combiner Using Planar Artificial Transmission Line

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Abstract—A miniaturized Gysel power divider/combiner (PDC) based on planar artificial transmission line (ATL) is presented in this paper. This planar ATL is composed of microstrip equivalent quasi-lumped elements and their discontinuities, and the ATL is capable of synthesizing microstrip line with various characteristic impedances and electrical lengths. For demonstration, the simulated and experimental results of proposed PDC @ 1 GHz implemented on microstrip are given. Experimental results of the designed PDC agree well with the theoretical predictions. The proposed Gysel PDC circuit not only demonstrates low insertion loss at the fundamental frequency with compact size and high frequency suppression features, but also maintains Gysel PDC's high power-handling advantage. The occupied sizes of the proposed Gysel PDC are merely about 40% of the conventional Gysel PDC.

1. INTRODUCTION

At present, power divider/combiner (PDC) are widely used in microwave communication and radar systems, such as the feeding networks for antenna arrays and the power splitting/combining networks for microwave power amplifier modules [1–6]. There are various PDC, and the Gysel PDC is one of the most popular structures. Figure 1 shows the traditional two-way Gysel PDC. This traditional Gysel PDC is made up of six lines, and the electrical length of each line is 90°. Generally, The impedances of each line are $Z_1 = 70.7\,\Omega$, $Z_2 = 50\,\Omega$, $Z_3 = 35\,\Omega$ (for getting a wider frequency band, usually choose a lower value of Z_3) [3–6].

The main advantages of Gysel PDC are (1) the capability of heat transfer to the ground plane because of external isolation load resistors, (2) monitoring capability for imbalances at the output ports. Consequently, the Gysel structure plays a key role in many high PDC applications. But the major drawbacks of the conventional Gysel PDC are its large size and the presence of spurious response due to the adoption of quarter-wavelength transmission lines [7–11].

Recently, numerous achievements have been published in order to minimize PDC size or to achieve high frequency suppression performance. Meandering of transmission lines can be the most straight forward way for size reduction [12]. Using lumped elements directly to approximate the behavior of a transmission line is a approach for miniaturization [13, 14]. Although the lumped-element PDC has the merit of compact size, it suffers from low-Q factor problem. Some studies overcome this problem by using defected ground structure (DGS) or electromagnetic bandgap (EBG) cells for the size reduction or suppression of harmonic frequency. However, this structure has a relatively limited ability to miniaturize the circuit size. And explicit design formulas are often not available [15–19]. Structures without reactive components by using open-stubs were proposed with even-odd-mode analysis method [20–25]. Recently, planar artificial transmission line (ATL) can be readily fabricated by standard printed circuit broad (PCB) technology. To design a PDC with an even more compact size, the miniaturized Wilkinson PDC and coupler with planar ATL are proposed in [26–30].

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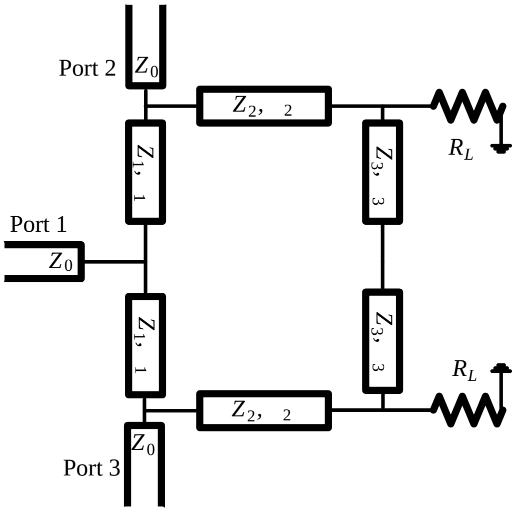


Figure 1. The traditional two-way Gysel PDC.

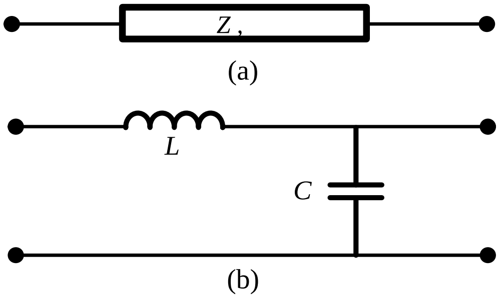


Figure 2. (a) Lossless conventional transmission line. (b) Equivalent lumped circuit of transmission line.

To design a PDC with an even more compact size, in this paper we propose a new miniaturized Gysel PDC on PCB with recently proposed planar ATL. By replacing the conventional connecting lines in the Gysel PDC with ATL, the Gysel PDC have compact sizes and improve high frequency suppression. This paper is organized as following. In Section 2, the design concepts, methodology, propagation characteristics of the ATL are briefly introduced. In Section 3, the proposed miniaturized Gysel PDC is presented along with the simulated and experimental results. This is then followed by conclusion in Section 4.

2. ANALYSIS AND DESIGN OF THE PROPOSED PLANAR ARTIFICIAL TRANSMISSION LINE

2.1. Principle of Planar Artificial Transmission Line

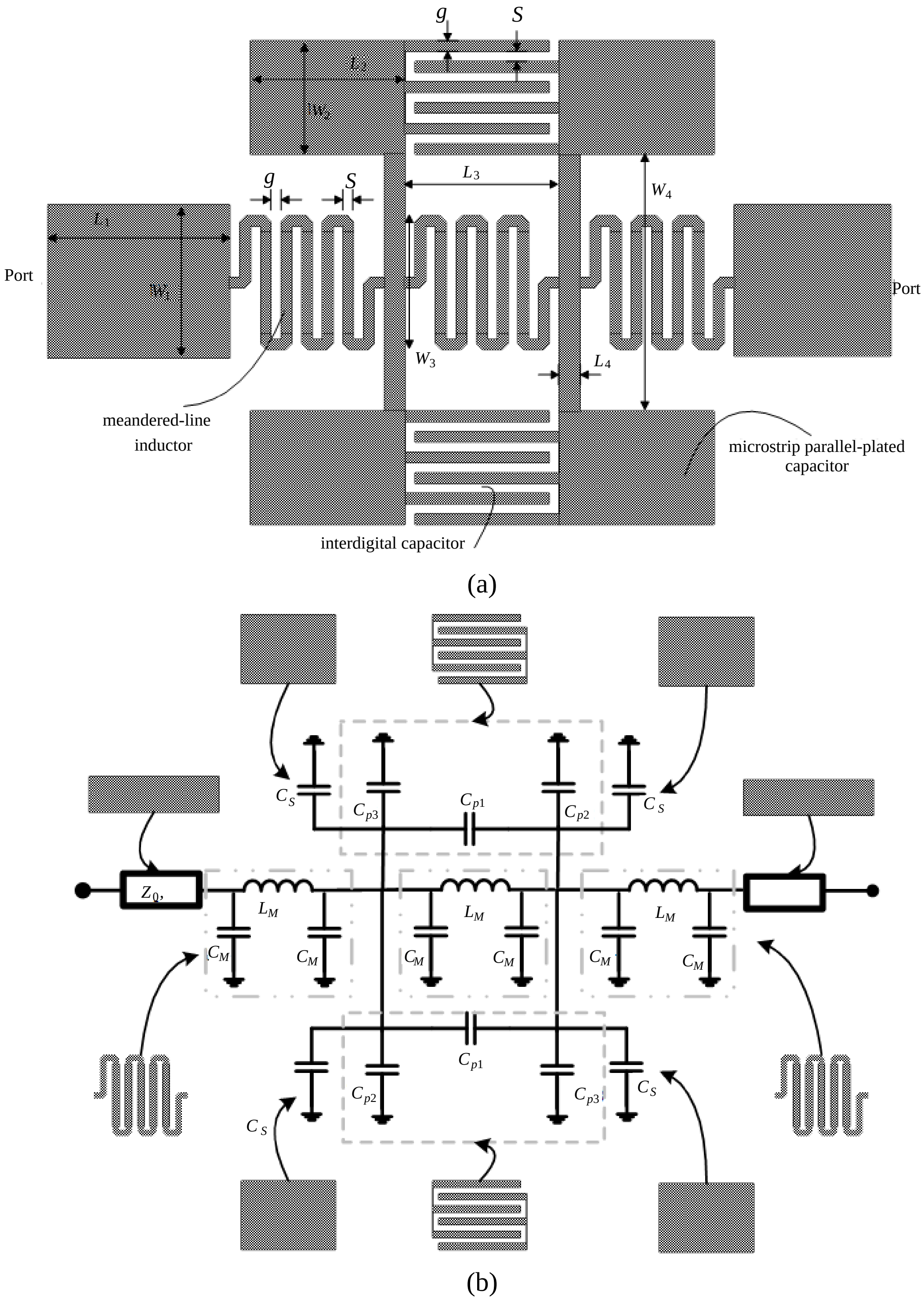
Figure 2 displays the lossless conventional transmission line and its equivalent circuit. Its characteristic impedance Z and guided wave-number β can be given by (1).

$$\begin{aligned} Z &= \sqrt{L/C} \\ \beta &= \omega\sqrt{LC} \end{aligned} \tag{1}$$

where L and C are the equivalent inductor and capacitor for unit length of transmission line, respectively, and ω is the working angle frequency. On the other hand, the circuit layout of a unit cell of the proposed ATL and its corresponding equivalent lumped circuit model are shown in Figures 3(a) and (b), respectively.

The ATL is composed of three cascade stages of meandered-line inductor, two interdigital capacitors, four parallel-plated capacitors and their associated discontinuities [26–30]. In order to make the ATL module simple, in this paper, we assume that the ATL is symmetrical, and some parasitic parameters are equal. The short connecting lines between the meandered-line inductors and parallel-plated capacitors are neglected. Referring to the equivalent lumped circuit model in Figure 3(b), inductors L_M represent meandered-line inductors, while parasitic capacitance L_M can be accounted for by capacitors C_M. The series capacitors C_{P1} is realized by two interdigital capacitors, and both the meandered-line inductor and interdigital capacitors can account for parasitic capacitances C_{P2} and C_{P3}. Shunt capacitors C_S are implemented with microstrip parallel-plated capacitors.

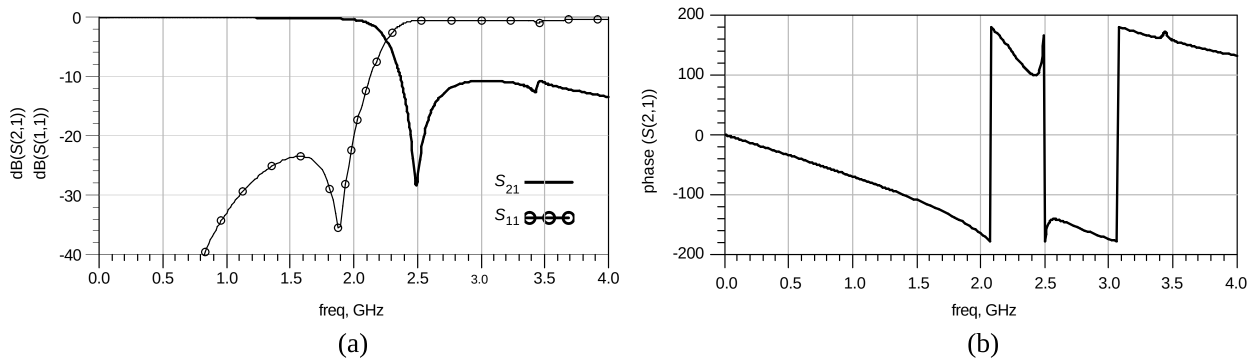
As the analysis in papers [26–29], the ATL effectively shortens guided wavelength, and therefore, significantly reduces the required physical length of a microstrip line with given characteristic impedance and electrical length. It can also be introduced to suppress the high frequency.



(a)

(b)

Figure 3. (a) The circuit layout of ATL. (b) Equivalent lumped circuit model of ATL.



(a)

(b)

Figure 4. The S-parameter of ATL cell with $50\,\Omega$, 70°. (a) Magnitude. (b) Phase delays.

2.2. Design of Planar Artificial Transmission Line

The design of the proposed ATL initially begins with the equivalent circuit model in Figure 3(b). The design concepts and methodologies of ATL have been presented in detail in [27–30]. It is also known that the inductor values of ATL can be easily optimized by tuning the meandered-line, and the capacitance values of ATL can be easily optimized by either tuning the fingers of an interdigital capacitor or adjusting the occupied area of a parallel-plated capacitor [28–30].

In this paper, for simple design, we define the numbers of meandered-line sections $n = 3$, and gap and width of meandered-line and interdigital capacitor $g = s = 0.2\,\text{mm}$. We also define 'm' as the number of interdigital capacitor sections. Following the design rules, an example of ATL with a characteristic impedance of $50\,\Omega$ and electric length of 70° was designed and optimized by the ADS electromagnetic simulation. The simulated S-parameter, phase delays and characteristic impedance of the $50\,\Omega$-70° versus frequencies is shown in Figure 4.

From Figure 4, the ATL shows a similar S-parameter to the original transmission line at around fundamental passband frequency and bandstop filter character at the higher frequency.

3. SIMULATION AND MEASUREMENT

In Section 3, a miniaturized Gysel PDC is designed by utilizing the proposed ATL in Section 2. The design shown in Figure 5 was fabricated on a 1.6 mm FR-4 substrate with dielectric constant 4.3 and 1 GHz center frequency of PDC as an example. The high power handling capacity depends on the

Table 1. The parameters of ATLs in the proposed Gysel PDC.

	Equivalent ATL @ 1 GHz		
	$70.7\,\Omega$-90°	$50\,\Omega$-90°	$35\,\Omega$-90°
n	3	3	3
m	3	5	6
g (mm)	0.2	0.2	0.2
s (mm)	0.2	0.2	0.2
L_1 (mm)	7	8	7
M_1 (mm)	1.6	3.6	5.3
L_2 (mm)	2.2	2.4	2.8
M_2 (mm)	2.2	3.8	4.6
L_3 (mm)	3	3	3
M_3 (mm)	1.6	0.8	0.6
L_4 (mm)	0.4	0.4	0.4
M_4 (mm)	5	3	3

isolation loads R_L. We use resistor for termination in this paper for demonstration, and the resistors can be replaced by external isolation load, which is outside the PCB, for high power handling.

As shown in Figure 5, two 70.7 Ω-90°, two 50 Ω-90° and two 35 Ω-90° ATLs were introduced to replace the conventional quarter wavelength microstrip lines in the Gysel PDC. In order to accommodate the parasitic effects, adjustment of the physical lengths, width and gaps of the lines were applied using an electromagnetic (EM) solver ADS. Table 1 gives the parameters of ATLs in the proposed Gysel PDC.

The measurements were taken by an Agilent performance network analyzer. The simulated and measured S-parameters of the proposed miniaturized Gysel PDC are illustrated in Figure 6, and are found to be in good agreement.

Referring to Figure 6, the measured center frequency of the miniaturized PDC is about 1 GHz. Inside the fundamental band, the divider was found to exhibit an insertion loss less than 3.65 dB and

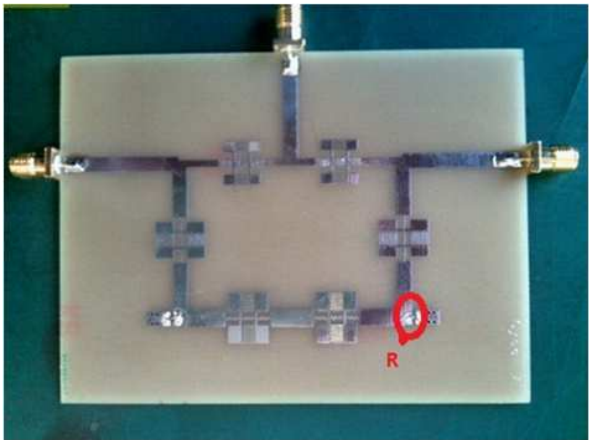
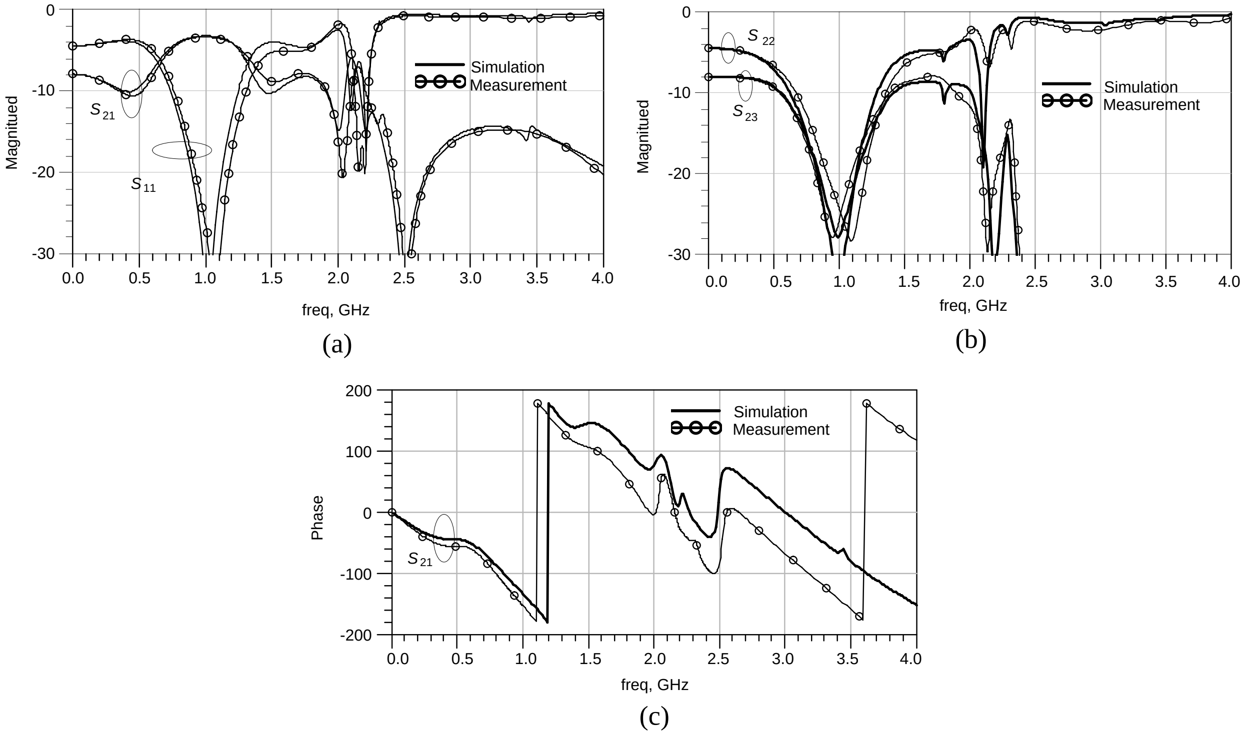


Figure 5. The proposed Gysel PDC with ATLs.

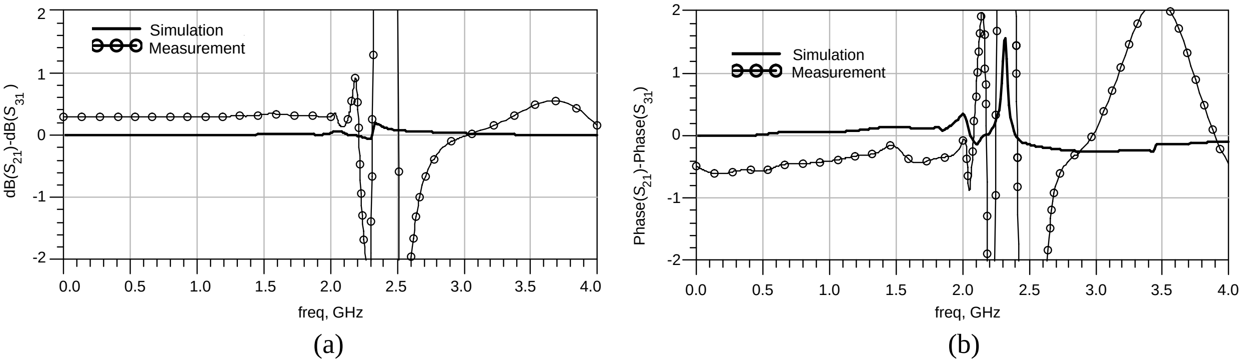


(a)

(b)

(c)

Figure 6. The Simulation and measurement of S-parameter performance of proposed Gysel PDC.



(a) (b)

Figure 7. The Simulation and measurement of the output magnitude and phase difference between port 2 and port 3.

Table 2. Comparisons of the major features of various Gysel PDC.

	Relative area	*Harmonic suppression*	*Fabrication*
Paper [1]	100%	No	Single layer
Paper [5]	not explicit report	Yes	Single layer
Paper [7]	55%	No	Double layer
Paper [31]	57%	Not report	Double layer, Additional lumped elements
This work	40%	Yes	Single layer

minimum return loss (both input and output) and port isolation less than -15 dB, over a fractional bandwidth of about 30%. The output magnitude and phase difference between port 2 and port 3, displaying in Figure 7, was found to be negligibly small at the fundamental band.

By replacing the conventional connecting lines in the Gysel PDC with ATLs, it is observed from the Figure 5 and Figure 6 that the proposed Gysel PDC has been significantly miniaturized with fairly good responses at fundament frequency and high frequency suppression. The dimension of the proposed divider is about $0.30\lambda_g * 0.17\lambda_g$, and the dimension of the conventional Gysel PDC is a little larger than $0.5\lambda_g * 0.25\lambda_g$. Here λ_g is the guided wave length of microstrip line at center frequency of 1 GHz. Accordingly, the circuit area of the proposed design is merely 40% of that of a conventional Gysel PDC. It is believed that the discrepancies between the simulated and measured results were mainly caused by fabrication tolerances, discontinuities and parasitic effect. Table 2 compares the proposed design with several previous designs.

4. CONCLUSION

In this paper, a new miniaturized Gysel PDC is designed, fabricated, and measured. This new PDC is realized by a recently proposed ATL and features a size reduction as high as 40% and very wideband high frequency suppression. Also the proposed circuit maintains Gysel PDC's high power-handling advantage over Wilkinson PDC and flexible layout with simple design process. Experimental results of the designed PDC agree well with the theoretical predictions. The proposed PDC can be applied in a wide variety of circumstances where circuit miniaturization is demanded.

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