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Building Blocks for a 24 GHz Phased-Array Front-End in CMOS Technology for Smart Streetlights

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Abstract—According to a recent European Union report, lighting represents a significant share of electricity costs and the goal of reducing lighting power consumption by 20% demands the coupling of light-emitting diode (LED) lights with smart sensors and communication networks. In this context, this paper proposes the integration of these three elements into a smart streetlight, incorporating a 24 GHz phased-array (Ph-A) front-end (FE). The main building blocks of this Ph-A FE integrated in a low-cost 90 nm complementary metal-oxide-semiconductor (CMOS) technology are fully characterized. The selected FE's architecture allows the implementation of transceivers as well as Doppler radar sensors functionalities. More specifically, the Ph-A technology is applied to a Doppler radar sensor in order to realize multi-lane road scanning and pedestrian detection. That way, the smart streetlight can become eco-friendly by turning on the LEDs only when necessary as well as to measure traffic parameters such as vehicle speed, type and direction. Intercommunication between the smart streetlights is based on a time-sharing mechanism that uses the same FE reconfigured as transceiver. Thanks to this functionality, the recorded traffic information can be relayed through adjacent streetlights to a control center, and control commands and warnings can be spread through the network. The system requirements are derived assuming a simplified model of the operating scenario with a typical inter-light distance of 50 m and line-of-sight between lights. The radar range is around 60 m, which allows for continuous coverage from one streetlight to the adjacent one. Meanwhile, a communication range of 140 m is derived as a fundamental requirement for reliable communication between streetlight sensors because it allows bypassing of one node in case of failure. For the developed building blocks — a low-noise amplifier, a variable-gain amplifier, a voltage-controlled oscillator and a vector modulation phase shifter — the design methodology is presented together with measurement results. The system power, consumption, noise figure and gain are estimated by means of a system analysis based on the measured data from the implemented blocks and the state of the art performances for the missing parts. It is shown that the requirements can be fulfilled with a total power consumption of around 375 mW in Doppler radar sensor mode and around 190 mW in transceiver mode. To the authors' knowledge, this kind of integration is new and overcomes some limitations of the currently used solutions based on infrared sensors and low-throughput communications.

1. INTRODUCTION

In line with European Union legislation to phase out incandescent light bulbs in streetlights by the end of 2016 [1], some important researches have been done in the past few years to develop light-emitting diode (LED) light sources with additional smart functionalities. Most of the research in this area focuses on wireless networking between lamps by using a standard protocol such as ZigBee [2]. Currently, there are few reliable movement sensors on the market. Indeed actual passive infrared sensors are not able to cover the whole illumination area of a streetlight and are very sensitive to environmental influences

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like rain or snow. Different field tests have shown that there are some reliability problems with infrared sensors in the range of about 10 m [3]. Only a few developments have targeted the integration of wireless sensors to add sensing features to the LED lamps [4]. Moreover, the high density of streetlights would be an ideal platform for an intelligent sensor network to monitor the road network and the environment.

To upgrade the huge number of streetlights, an extremely low-cost solution is required. Complementary metal-oxide-semiconductor (CMOS) technology enables a low-cost implementation of complex systems on the same chip (system on chip, SoC). Furthermore, integration of the sensor and the LED streetlight can profit from the ceramic substrate used to dissipate the heat produced by LEDs. The high relative permittivity and the low losses of the ceramic substrate allow the implementation of miniaturized and high-performance printed circuits at mm-wave [5]. For example, a very compact radar antenna array is reported in [6], where a 36 GHz four-patch antenna array is smaller than 1 cm^2.

The industrial, scientific, and medical (ISM) band at 24 GHz is accepted worldwide for short-range communication and for radio determination [7, 8]. Since a wide band, i.e., 250 MHz, is available, a simple binary phase-shift keying (BPSK) modulation carrying some Mbps enables the allocation of more than 10 channels. Considering the duty cycle between the radar and transceiver modes (e.g., 10%), the net data rate could easily exceed the ZigBee's throughput (100 kbps) already proposed for streetlight networking.

The development of a 24 GHz integrated circuit (IC) radar front-end (FE) started in 2003 with silicon germanium (SiGe) technology [9] by M/A-COM Technology Solutions. It continues today, especially for automotive radar, as well as in many silicon foundries, e.g., STMicroelectronics, Philips and Motorola [10–12]. In the last five years, some implementations of the main building blocks and complete FEs have also been developed in CMOS technology by university groups [13]. Phased-array (Ph-A) technology was developed during World War II, and it continues to be used mainly in military radars. Recently, increasing attention has been focused on the research of the Ph-A technology for civil applications, such as automotive radars in CMOS technology [14]. However, chipsets are still hardly available on the open market for general purpose applications. To the best of our knowledge, there is only the BGT24MTR11 by Infineon Technologies [15], which works at 24 GHz and is based on SiGe monolithic microwave integrated circuit. Moreover, this product does not use the Ph-A technology.

In this paper, a novel approach of the 24 GHz CMOS IC FE, which is based on our previous work [16–18], is proposed. This FE uses the Ph-A technology for the Doppler radar sensor and integrates an extra transceiver communication channel that can be used in a time-sharing mechanism.

2. SYSTEM DESCRIPTION AND ANALYSIS

2.1. System Description

One advantage of working at 24 GHz is the quite high Doppler shift, about 44 Hz per km/h, which allows the detection of a slow moving target with only few hundreds of milliseconds of measurement time. It entails that the FE does not need to work continuously as a radar.

The estimation of Doppler frequency can rely on different techniques depending on the desired accuracy. For movement detection, a low false alarm probability is the main requirement. For this purpose, a simple calculation of the average of the Doppler frequency on few signal cycles (e.g., 10) is typically enough and allows a short system reaction time. For example, this principle was used in [19], showing an accuracy better than 10% for the vehicle length estimation. This performance can be equivalently seen as the capability of the system to successfully recognize more than 90% of the Doppler signal cycles. Therefore, considering that the average of just 10 cycles of the Doppler signal is used, a worst-case calculation for the reaction time can be made for a vehicle running at a maximum speed of 250 km/h (70 m/s). In this case the Doppler frequency is 11 kHz and the observation time necessary to do the average is almost 900 µs, which corresponds to only 6.5 cm of vehicle displacement during this time lapse. Meanwhile, for the lowest speed case of 1 km/h, the Doppler signal will have a period of 22.5 ms, and with 10 averages to obtain an accurate measure, the minimum observation time will be around 225 ms, which also corresponds to 6.5 cm of vehicle displacement. If we further assume a measurement rate of four times per second, which is still acceptable for the reaction time of the system because in the worst case (i.e., 250 km/h speed) the vehicle displacement is below 17 m which is well below the antenna footprint, we will still have 100 ms per second of free time that can be used for the

communication. By using a direct-conversion receiver and a direct-modulation transmitter, it is thus conceivable that a single FE may fulfill the radar and communication functionalities in time-sharing, by implementing a communication duty cycle of around 10%, i.e., using a data rate 10 times faster than the required throughput.

Figure 1 shows the streetlight application scenario and the functionalities implemented by the Ph-A FE. Typical parameters of the streetlight deployment are 7.6 meters in height and 50 meters in inter-distance [20]. By pointing the main antenna beam towards the sidewalk, the Doppler radar sensor can detect the presence of pedestrians and turn on the streetlights only when people are detected. Similarly, by pointing the antenna towards one of the road lanes, it is possible to detect the presence of cars and measure their speeds and lengths, as well as recognize their moving directions. When the FE works as transceiver, communication between streetlights is enabled, thus building up the hardware for a wireless sensor network (WSN). The streetlight files can be organized in a hierarchical network that enables each node to communicate with a control center. This is a powerful feature that allows the collection of a lot of information, such as the presence of faults, and real-time road traffic conditions. Moreover, profiting from the 250 MHz bandwidth, a frequency division technique can be used, for example, adjacent FEs could use different carrier frequencies, i.e., f_1 to f_n, in order to improve the robustness against radar and transceiver interferences. In the event of fault of one or more transceiver, the control center can locate the fault and change the frequency plan to bypass the out-of-order ones.

From the description given above, it is clear that the antenna system is a key element of the Ph-A FE. Indeed, in radar mode, a beam-steering antenna with a relatively narrow beam is needed. A further advantage of working at 24 GHz is the antenna dimension, because the in-air wavelength is only 12.5 mm. For inter-communication, a fixed antenna with limited directivity is preferable in order to allow links with multiple FEs. To fulfill the different requirements, two types of antennas are supposed to be used.

The radar antenna array is assumed to be a patch array antenna type; indeed it could be directly printed on the ceramic substrate usually used as LEDs carrier for heat dissipation. In this case the beam is pointed towards the ground. However, as shown in Figure 2, it should be tilted by about 76° in order to point towards the vehicle incoming direction as well as at the halfway point between two streetlights. This tilt is achievable by embedding fixed delay lines in the patches feeding transmission lines.

For inter-communication, a fixed antenna with limited directivity is preferable in order to allow links with multiple FEs. Therefore the inter-communication link exploits two dedicated antennas for

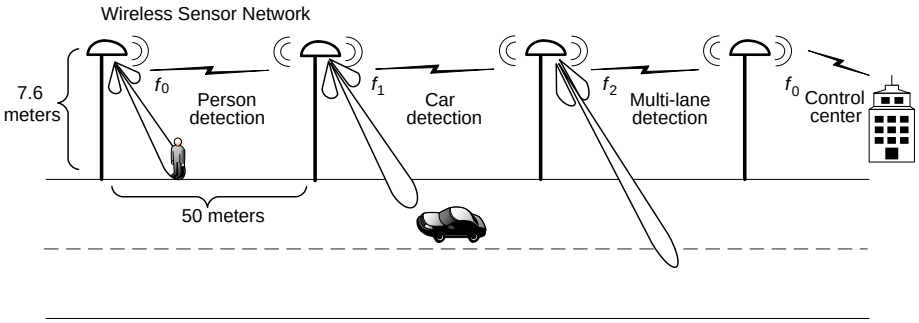

Figure 1. Sketch of the proposed scenario and the functionalities implemented by the Ph-A FE.

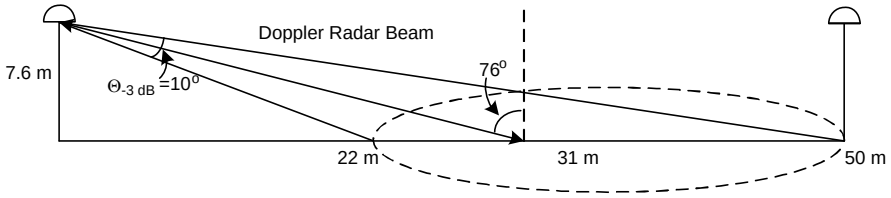

Figure 2. Geometrical setup of the proposed scenario.

transmitter (TX) and receiver (RX), less directive than the radar case, pointing towards the adjacent streetlight. The wireless link between the streetlights can be nearly treated as a line-of-sight point-to-point communication.

2.2. Additional Antenna Considerations

A complete analysis with electromagnetic models is beyond the scope of this paper. However, there are several examples of antenna design at 24 GHz for radar applications. In this paper, we refer to [19], where two antenna arrays of 10×4 patches each one were used as TX and RX antennas. Such an antenna array can be viewed as the combination of four sub-arrays where each one consists of 10 elements in-line. Thus, the four linear sub-arrays can be paired with the four channels of a Ph-A FE, in which case the beam steering can occur along the same direction of the shorter side of the antenna. The corresponding 3 dB beamwidth can be calculated by the simple model equation presented in [21]: for a linear array, the half-power beamwidth is approximated by $\Theta = \frac{101.8^\circ}{N}$, where N is the number of elements. Thus, in our case, a 10×4 element linear array will have a 3 dB beamwidth along the larger and smaller array side, of about 10° and 25°, respectively. The same antenna array was characterized in [22], where the reported 3 dB beamwidth was 10° for the larger array side and 28° for the smaller side. These figures are closed to the ones obtained with the simple model calculation aforementioned. Moreover, in [22], the antenna gain was 17.6 dB and the mutual coupling between RX and TX was not a limiting factor due to the intrinsic rejection of the homodyne receiver used in the Doppler radar scheme. Therefore, we consider that a 10×4 antenna array is sufficient to fulfill the requirements of the selected application.

Antenna sidelobes can also affect the radar sensor performance, e.g., affecting the scanning selectivity and the capability of the radar to classify vehicles per lane, or affecting the capability of the system to detect moving objects when two different objects with various speeds are seen by the radar. However, the effects of the antenna sidelobes can be minimized by controlling the radiated power level so that the sensitivity of the system is adjusted to detect only the strongest Doppler echo and/or by filtering the Doppler estimation with a second step of calculation, for example by performing the calculation of the histogram of the Doppler frequencies detected. If two or more peaks are shown, the processing can understand the presence of two or more vehicles. It requires more processing but it is still possible with standard embedded microprocessors.

2.3. System Analysis

Based on the assumptions made above, the estimation of the system specifications is discussed next. Since there are two system operating modes, the analysis is carried out for both modes.

2.3.1. Doppler Radar Case

Working in radar mode, Eq. (1) shows the well-known radar free-space path loss (PL) equation [23]:

$$PL_{radar}\,(\mathrm{dB}) = -10 \log \frac{c^2 \sigma}{{f_0}^2 (4\pi)^3 R^4}, \tag{1}$$

where c is the speed of the light, f_0 the operating frequency, i.e., 24 GHz, R the detection range, and σ the radar cross section of the target, which is assumed to be 0.1 m^2 from [24].

Recalling that the receiver sensitivity is given by the sum of the minimum signal-to-noise ratio (SNR), the noise figure (NF) and the thermal noise power, the radar range can be written as a function of PL (Eq. (1)), therefore the Friis transmission equation can be written as [23]:

$$\begin{aligned} PL_{radar}\,(\mathrm{dB}) = {} & P_{TX} - NF_{radar} + G_{TX,sub} + G_{RX,sub} - P_{noise} \\ & - SNR_{\min} + CPG_{TX} + CPG_{RX} - LM - 2 \times L_\eta, \end{aligned} \tag{2}$$

where:

P_{TX} is the transmitted power for a single channel, which is assumed to be about 1 dBm in order to keep a low consumption and to deal with the low-voltage power supply of 90 nm technology.

NF_{radar} is the noise figure of the single channel receiver, which is assumed to be about 6 dB based on the investigation of the state of the art of the 24 GHz receiver FE.

$G_{TX,sub}$ and $G_{RX,sub}$ are the gain of a 10-patch $\lambda/2$-apart linear array, which is estimated to be around 16.7 dB by simulation with basic models.

P_{noise} is the thermal noise power for each channel, which is estimated by the equation: $P_{noise}\,(\mathrm{dB}) = -174 + 10\log BW_n$. In this equation, the equivalent noise bandwidth of the Doppler radar system, BW_n can be set according to the Doppler frequency shift f_D. The latter can be written as $f_D = f_0\frac{2v}{c}\cos\alpha$, where f_0 is the carrier frequency, i.e., 24 GHz; α is the angle between the antenna pointing and the direction of the moving target; and v is the target velocity, which is assumed to be lower than 250 km/h. So the maximum Doppler shift, $f_{D,\max}$ is around 11 kHz since the Doppler shift constant is 44 Hz per km/h. Consequently, the BW_n can be assumed for a first-order filter to be equal to: $f_{D,\max} \times \frac{\pi}{2} \approx 18$ kHz. Therefore, P_{noise} is calculated as -131.5 dBm.

$SNR_{\min}$ is the minimum SNR of the Doppler radar, which is assumed to be 12 dB because of the highly sensitive detection methods usually employed [25].

CPG_{TX} and CPG_{RX} represents the coherent process gain, which reflects the power and SNR enhancement of the Ph-A technology. It can be explained easily by assuming an N channel Ph-A transmitter with each single channel of P watts of emitting power. Along the pointed direction, the waves add coherently producing an amplitude N times bigger than the single channel, so the power is N^2P watts. Therefore, the power gain is $20\log(N)$ in dB. In reception, the Ph-A enhances the SNR of N times because of the coherent addition of the useful signals and the incoherent addition of the noise ($10\log(N)$ in dB) [26]. For a four-channel Ph-A, the CPG is 6 dB and 12 dB for the receiver and transmitter respectively.

LM is the link margin, which is assumed to be 10 dB. This margin could also include any antenna mismatch. However, it is assumed that the antennas are well matched, so that the mismatch is negligible.

L_η represents the array efficiency and takes into account the losses due to the combination of the Ph-A channels [27]. It can be roughly estimated of 2 dB, by comparing the antenna gain of a 10×4 array ($\sim$21.4 dB) with the theoretical combination of four isolated 10-element linear arrays. The losses are 16.7 dB + 6 dB − 21.4 dB = 1.3 dB.

Upon substituting the assumed values mentioned above in Eq. (2), the PL of the radar mode can be calculated as 152 dB. Furthermore, the sensitivity of the receiver can also be calculated as -113 dBm.

The final step is to estimate the radar detection range by inverting Eq. (1). The radar detection range corresponds to around 60 m, which gives a sufficient margin over the required 50 m of the studied scenario.

2.3.2. Transceiver Case

The inter-streetlight communication can use smaller and less directive antennas, pointing towards the nearby streetlights. Moreover, a single-channel transceiver is used because the beam steering feature is not necessary so the coherent process gain is not exploited. With a methodology similar to the previous case, the PL from the Friis formula can be written as:

$$PL_{com.}\,(\mathrm{dB}) = P_{TX,com.} - NF_{com.} + G_{TX,com.} + G_{RX,com.} - P_{noise,com.} - SNR_{\min,com.} - LM. \quad (3)$$

The meaning of each term is discussed as follow:

$P_{TX,com.}$ and $NF_{com.}$ are kept the same as the radar case because of the hardware reuse, and are 1 dBm and 6 dB respectively.

$G_{TX,com.}$ and $G_{RX,com.}$ are the antenna gains, which are estimated to be around 14.9 dB by simulating a 2×4 patch-array antenna with basic models.

Targeting a net data rate of 1 Mbps and assuming a duty cycle of 10% for the data transmission, the necessary peak data rate must be 10 Mbps. Exploiting a simple BPSK modulation, considering the bit error rate of 10^{-6} and no coherent demodulation, the $SNR_{\min,com.}$ is assumed to be 12 dB [28], and the channel bandwidth is around 25 MHz (so there are up to 10 channels in the ISM band).

Under these assumptions, the noise power floor, $P_{noise,com.}$ is equal to -100 dBm, and thus entails a sensitivity of -82 dBm.

By applying Eq. (3), a maximum PL of 103 dB is estimated and applying the one way free-space PL equation [23], we have

$$PL_{com.}\,(\mathrm{dB}) = -10\log\frac{c^2}{(4\pi R f_0)^2}. \quad (4)$$

A maximum communication range of 140 m is obtained. Since the range is more than twice than the distance between two adjacent streetlights, it will be possible, in case of node fault, to leap over one or two streetlights and communicate with the next in the line.

2.4. Proposed ASIC Architecture

Based on the system analysis, a four-channel Ph-A architecture as shown in Figure 3 is proposed. This FE consists of two parts: the antenna arrays and the application-specific integrated circuit (ASIC) front-end; meanwhile the digital back-end is out of the scope of this paper. The antenna part has two types of antennas: the 10×4 patch-array antenna used for the Doppler radar sensor and the 2×4 patch-array antenna for inter-communication. The radar type is the continuous-wave (CW) Doppler radar, which does not rely on any modulations to separate the radiated signal to the reflected one. This type of radar is robust to the coupling between TX and RX paths. The homodyne scheme can split the generated CW signal to feed the TX antenna and the RX mixer. The parasitic coupling between TX and RX antenna and circuits will be in any case smaller than the direct signal from the local oscillator (LO) and the RX mixer. The problem does not exist in transceiver mode due to the half-duplex working mode.

The ASIC FE consists of a direct-conversion receiver and a direct-modulation transmitter. A dedicated RF channel is used for the transceiver mode, while the baseband is reused. In this case, even if consuming a bit more chip area, no antenna switches are needed and the symmetry of the main four-channels can be preserved. The core of the Ph-A scheme is a 24 GHz phased-locked-loop (PLL) frequency synthesizer combined with a vector modulation phase shifter (VMPS). The phase shifters provide beam-forming functionality in radar mode as well as direct BPSK modulation in transceiver mode. The four VMPS outputs are split in order to contemporaneously feed the RX and TX paths as required by the continuous-wave Doppler radar scheme. The additional RX and TX paths for the transceiver are switched off during radar mode. For the radar RX paths, the VMPSs provide the phase-

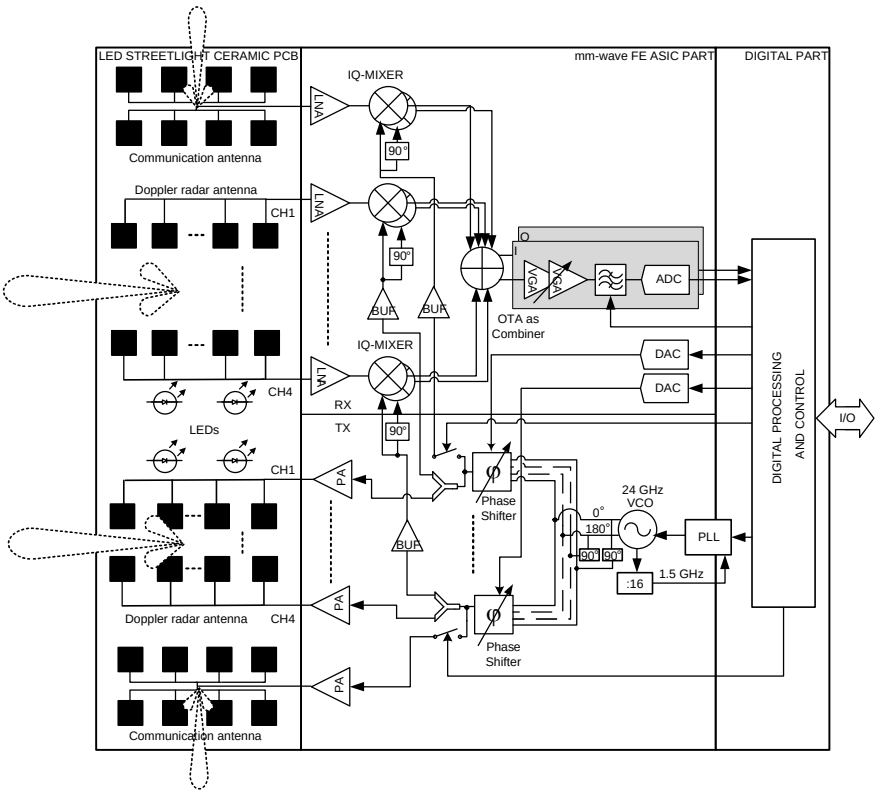

Figure 3. Architecture of the 24 GHz IC Ph-A Doppler radar sensor and transceiver system.

shifted LO signals to the mixers. Complex down-conversion is adopted so that the down-converted signals have the in-phase (I) and quadrature (Q) components. Thus, each channel of the Ph-A has a couple of mixers.

At the mixers outputs, the aforementioned coherent addition of the wanted signals and the rejection of the interferences take place. The resulting I and Q signals are processed in parallel by two identical baseband paths, consisting of: a low-pass filter (LPF), a variable-gain amplifier (VGA) and a multi-bit analog-to-digital converter (ADC). The baseband is shared in time division between transceiver and radar modes, therefore the LPF has to be reconfigurable in order to adapt the cut-off frequency to the wide bandwidth of the transceiver and the narrow bandwidth of the radar.

In the radar TX paths, the four phase-shifted signals are amplified to reach a power level of about 1 dBm on each channel. Thanks to the Ph-A architecture and the constant amplitude modulation, such a compression point is achievable also with a low-voltage power supply (1.2 V). By controlling the state of several switches in the RF paths' DC biases, the digital unit can manage the mode switchover so that a power-saving management is implemented by turning off the unused blocks.

3. CIRCUITS DESIGN AND MEASUREMENT RESULTS

The key building blocks, namely the LNA, the VGA, the VMPS and the voltage-controlled oscillator (VCO), were designed in 90 nm technology by United Microelectronics Corporation (UMC). The technology offers nine metal layers with a top layer thickness of 3 µm for high-Q inductors and scalable

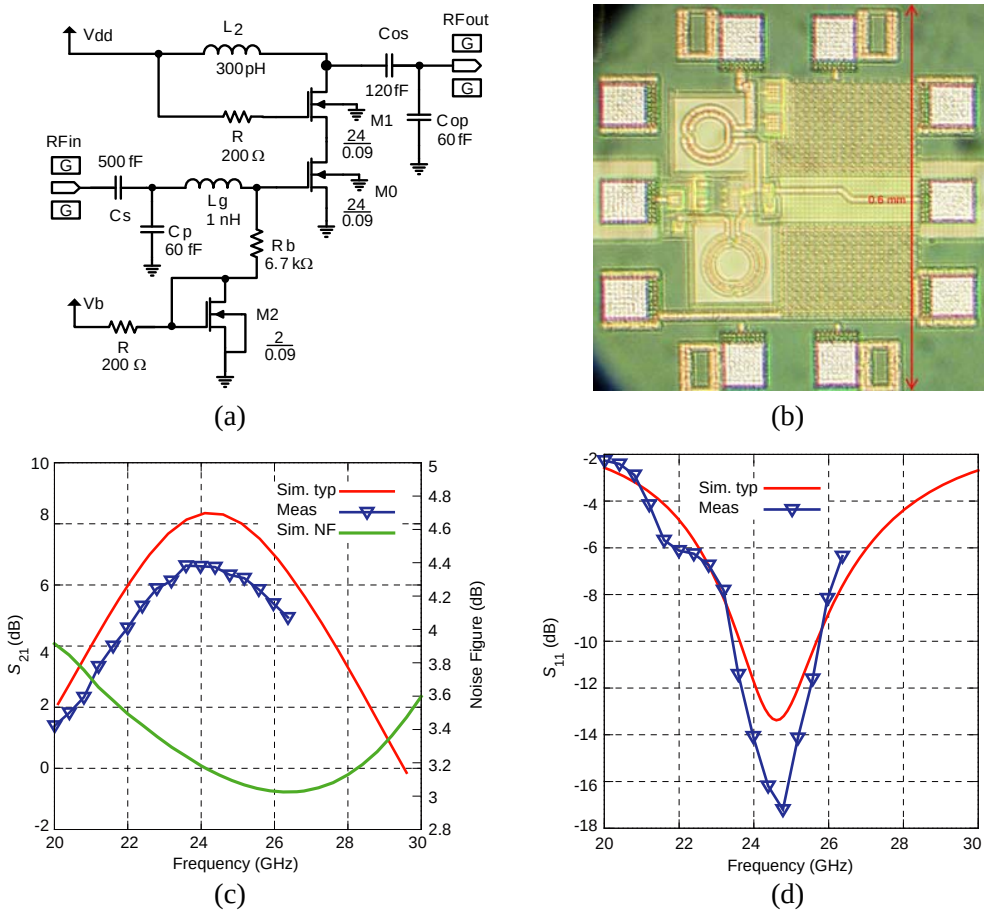

Figure 4. Single-stage LNA schematic, die photo, simulated and measured S-parameters. (a) Schematic of 1-stage LNA. (b) Die photo of 1-stage LNA. (c) Simulated and measured LNA gain. (d) Simulated and measured LNA return loss.

models for passive RF components. RF metal-oxide-semiconductor field-effect transistors (MOSFET) have $V_{\max}$ of 1.2 and 1.8 V. The designed blocks were implemented in a test tape-out with the purpose of refining the methodology used for the parasitics estimation.

The measured results shown below are all taken on-chip by using RF probes calibrated at the on-chip pads' plane.

3.1. Low-Noise Amplifier

The LNA design is based on a cascode amplifier as shown in Figure 4(a). Since little power gain is available at 24 GHz due to the MOSFET gain roll-off, the cascode configuration is used to increase the gain. For the same reason, and to get a better estimation of the parasitic ground inductance, the source inductor, commonly used for the simultaneous matching of the noise and gain, is omitted. All MOS transistors have a minimum length, i.e., 90 nm, and each cascode MOS has a total width of 24 μm obtained by connecting in parallel 24 fingers each 1 μm wide. The resulting MOS current density is almost 150 μA/μm, which is not far from the 250 μA/μm for the transition frequency (f_T) peak. The current-density reduction is due to the limited voltage headroom for the upper MOS, M1, which does not have the necessary overdrive (around 0.5 V) for the f_T peak. In Figure 4(c) and Figure 4(d), the measured gain and return loss are compared with the simulation results. The latter is based on the extracted layout view obtained by using the standard extraction tool available in Cadence®. The peak gain of 6.5 dB at 24.1 GHz is 2 dB lower than the simulated results, and the peak return loss is 4 dB better. The peak frequency also occurs exactly in the middle of the ISM band. Based on this comparison, the extraction method shows a quite good performance.

The noise figure cannot be measured with the available instrumentation because of the low LNA gain, and therefore the simulated NF of 3.2 dB is reported while an input referred 1 dB compression point (IP1 dB) of −12 dBm has been measured. Finally, the LNA power consumption is 4.3 mW at 1.2 V.

A gain of only 6.5 dB is certainly insufficient to set the receiver NF at the desired level of 6 dB, therefore, a three-stage LNA has been designed. It is based on a cascade of three cascode amplifiers as shown in Figure 5(a). The first stage is almost identical to the previous single-stage LNA; the second stage uses the MOSs with the same parameters but its matching networks are embedded in the previous and following stages. The third stage uses bigger MOSs, i.e., 60 μm wide, since it needs to boost the output compression point at about 1 dBm. Measurement results, reported in Figure 5(c) and Figure 5(d), show a peak gain of 18.6 dB at 23.9 GHz and a return loss of −16 dB. A considerable frequency down-shift is visible as well as a gain loss of about 5 dB. In this case, even if process variations are taken into account, the parasitic extraction method does not perform well.

The measured NF of 5.5 dB is also well above the simulated 3.8 dB. On the other hand, the output 1 dB compression point is about 2 dBm as was expected. The power consumption is 18 mW at 1.2 V.

In Table 1, the LNAs' performances are compared with the state of the art. The single-stage LNA consumes less than one half the power of an amplifier with similar gain and noise figure. The three-stage LNA shows almost the same gain as the other multi-stage amplifiers but generates more noise while consuming 20% more power. If its peak gain were like the simulated one, the comparison would have been favorable.

Table 1. 24 GHz LNA specification comparison.

Reference	[29]	[30]	[31]	Our 1-stage LNA	Our 3-stage LNA
Frequency (GHz)	24.0	24.0	24.0	24.1	23.9
Technology (nm)	90	130	90	90	90
Gain (dB)	7.5	19[a]	15.2[a]	6.5	18.6
Input matching (dB)	−16	−16	−12	−15	−16
Noise figure (dB)	3.2	3.8	2.9	3.2[b]	5.54
Power cons. (mW)	10.6	15	9.1	4.3	18

[a]Two-stage.
[b]Simulated.

3.2. Analysis of Parasitic Effects of the LNAs' Layouts

To investigate the parasitic effects of the LNAs' layouts, the measurement results and the extracted post-layout simulation results are compared. As shown in Figure 4 and Figure 5 and summarized in Table 2, these results do not match very well, especially for the three-stage LNA. It is likely that the

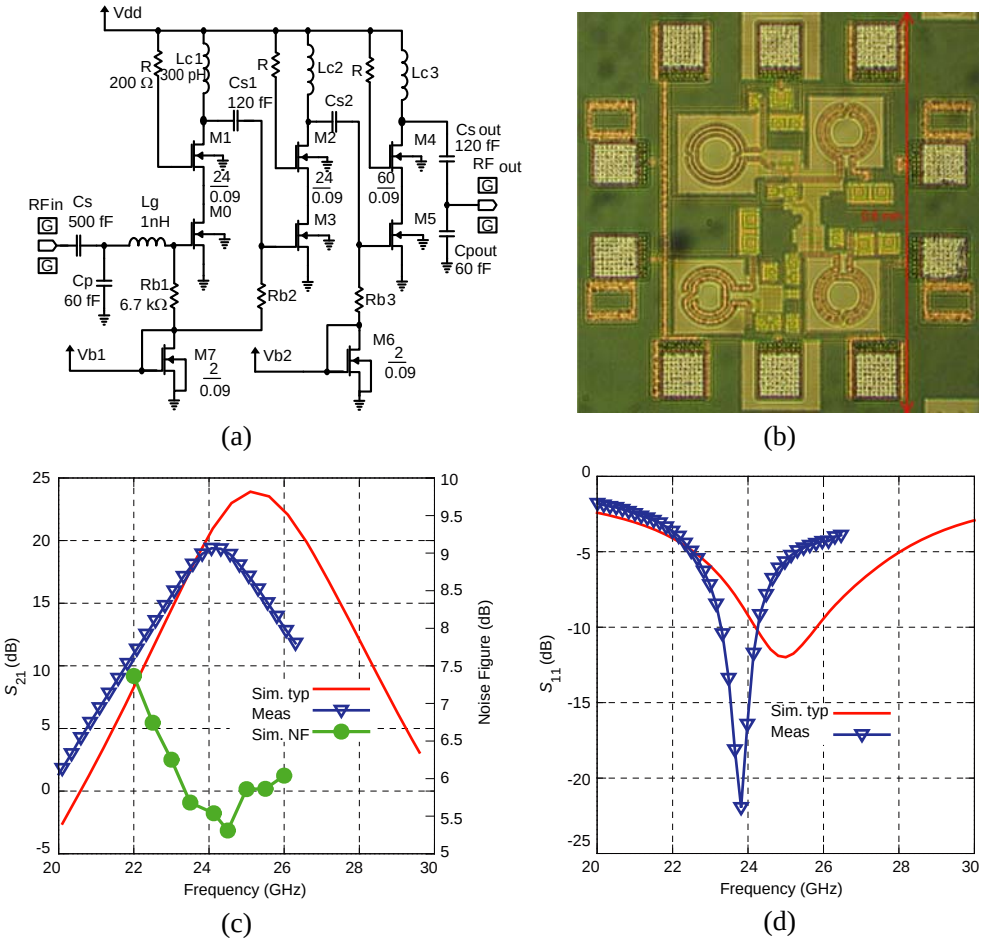

Figure 5. Three-stage LNA schematic, die photo, simulated and measured S-parameters. (a) Schematic of 3-stage LNA. (b) Die photo of 3-stage LNA. (c) Simulated and measured LNA gain. (d) Simulated and measured LNA return loss.

Table 2. LNA parasitic analysis with the comparison of Gain @ 24 GHz, NF and input matching.

	Gain (dB)	NF (dB)	Input matching (dB)
1-stage LNA			
Measurement	6.5	N/A	−18.3
Extracted post-layout	8.2	2.98	−12.4
Manual parasitic	6.5	3.52	−9.9
3-stage LNA			
Measurement	18.62	5.54	−19.2
Extracted post-layout	23.9	3.4	−12
Manual parasitic	16.86	5.12	−15.3

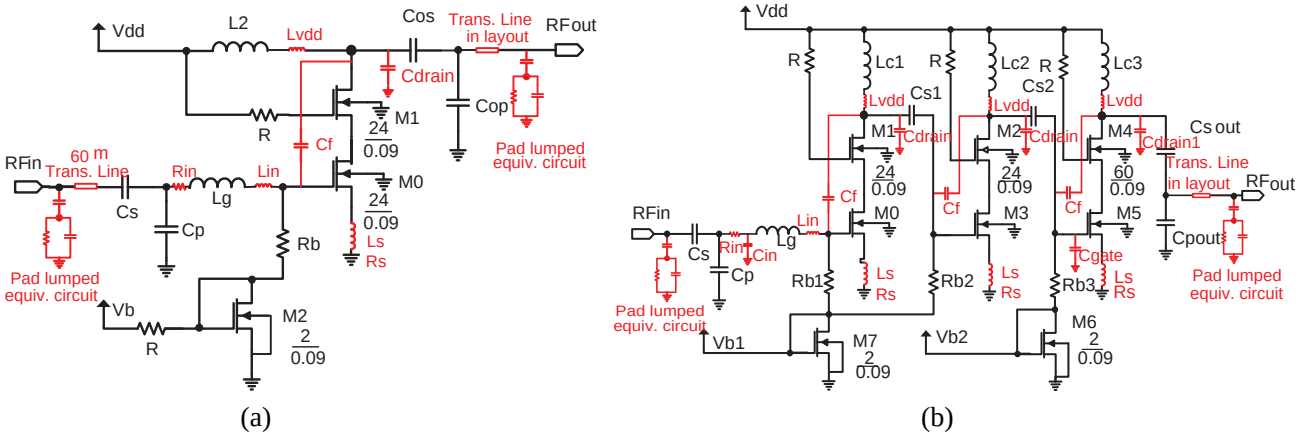

Figure 6. Parasitic schematic of the single-stage and three-stage LNAs. (a) 1-stage LNA parasitic schematic. (b) 3-stage LNA parasitic schematic.

inaccuracy comes from the parasitic extraction method implemented in the CAD tool. In order to get an in-depth understanding of the extraction methodology, a specific analysis was carried out. It was done by working at the schematic level and adding the key parasitic elements shown in red in Figure 6, namely: on-chip pads, microstrip lines for long connections, input series resistance R_s, source inductance L_s on cascode grounding, coupling capacitance C_f between input and output of the cascode amplifier, and tuning capacitances/inductances in parallel/series with the resonators.

For test purposes, some structures, such as transmission lines, RF pads and inductors, were included in the chip to allow their modeling. Specifically, L_{in} and L_{vdd} account for 10% tolerance of L_g and L_2 values; L_s is estimated to be around 50 pH and C_f is estimated to be about 4 fF. The transmission lines are modeled by microstrips with their physical length and the substrate model provided in the technology datasheet. Finally, the equivalent resistance in series with the gate, R_s, is estimated by adding the DC resistances of the vias and the metal paths.

Figure 7 shows a comparison between the schematic with parasitic and the measurements of the two developed LNAs. For the three-stage LNA, the same parasitics determined for the single-stage LNA are applied and only a slight tuning of the resonate loads is necessary for a good fitting. The parasitics modeling seems quite robust thanks to the physical model used. The reason why the extraction tool in Cadence® does not work very well at 24 GHz is not clear. The main mistake seems to be related to the estimation of the resistance in series with the gate. Indeed the 2 dB error of the noise figure is quite high. Also the coupling between inductors seems not to be considered even if the coupling option is selected. Finally, the schematic with parasitics shows a difference of less than 2 dB for the gain and 0.3 dB for the NF.

3.3. Variable-Gain Amplifier

The design of the VGA is based on the single-stage LNA upon which a current-steering technique is applied to control the current that flows into the load. Figure 8(a) shows the modification on the upper MOSFETs (M1 in Figure 4(a)) of the cascade configuration. This MOS is split into two groups: one is connected to the resonant load and the other is tied to the power supply. The amplifier gain is controlled by steering the current between these two groups of MOSFETs. The maximum gain is obtained when M2 and M4 are off while M1 and M3 are on, so that all the current flow into the load. Intermediate values of gain are achieved by controlling the number of the transistor fingers in conduction. Since the total current flowing in the lower MOS (M0 in Figure 8(a)) does not change, its gain and input impedance do not change, which results in a very stable input matching. It also entails that the phase of S_{21} parameter is also kept constant. This is an important feature for the implementation of the phase shifter in Section 3.4. Indeed, the digital control acts by switching on and off groups of fingers in which M2/4 and M1/3 are split. Through this way, the control scheme is scalable over the number of bits.

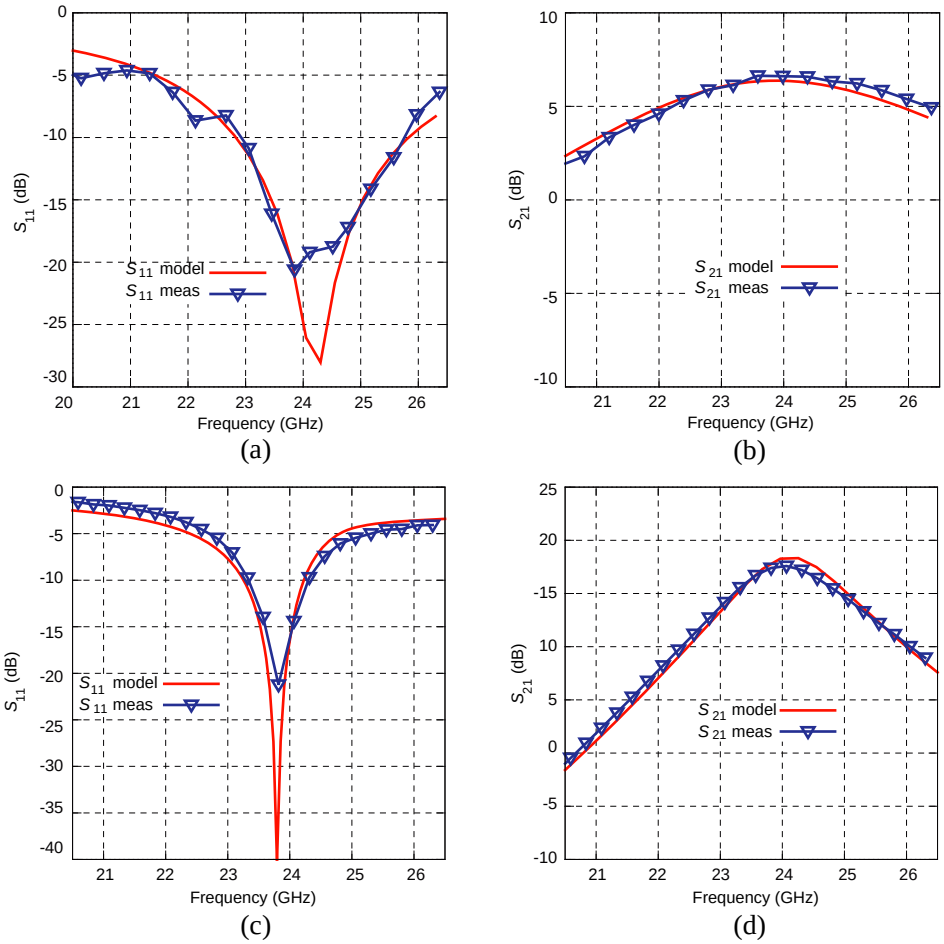

Figure 7. LNA parasitic models and their measurement results. (a) Measured and simulated S_{11} of 1-stage LNA: parasitic modelled. (b) Measured and simulated S_{21} of 1-stage LNA: parasitic modelled. (c) Measured and simulated S_{11} of 3-stage LNA: parasitic modelled. (d) Measured and simulated S_{21} of 3-stage LNA: parasitic modelled.

Table 3. Comparison of the measured results of the VGA.

Reference	[32]	[32]	[34]	Our VGA
Frequency (GHz)	4.93	21	26	23.8
Technology (nm)	90	180	130	90
Max. gain (dB)	12.2	3	5	5.9
Tuning states (bit)	6	3	4	2
Power cons. (mW)	28	112	4.5	4.5

Due to the limited number of available probes, the gain control is done with only two bits, whose states have been mapped to the maximum, half and minimum (isolation) gain. The size of the VGA is 0.3 mm × 0.15 mm, and 0.5 mm × 0.5 mm with the pads, as shown in Figure 8(b). The measured gains are 5.9 dB, 3.1 dB and −17 dB for the maximum, half and isolation states respectively. The S_{21} phase variation is just few degrees between the different states. Finally, by comparing the VGA with the state of the art in Table 3, one can see that the VGA shows the minimum power consumption, i.e., 4.5 mW at 1.2 V, for the considered working frequency and gain.

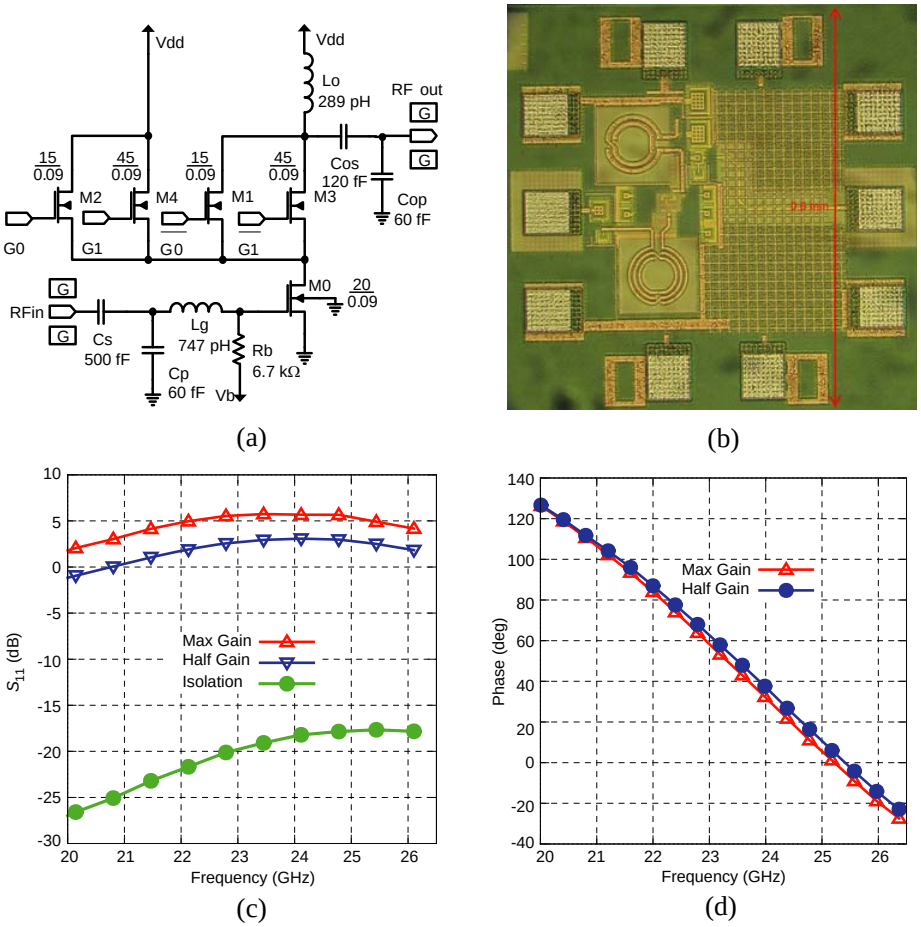

Figure 8. VGA schematic, die photo, simulated and measured results. (a) Schematic of VGA. (b) Die photo of VGA. (c) VGA measured gain for programmed states. (d) VGA measured phase for programmed states.

3.4. Vector Modulation Phase Shifter

The designed VMPS consists of two of the VGAs described in Section 3.3. Each VGA is placed at each I and Q channel. The output current from the I/Q channels is summed in a common inductor, i.e., L_o, as shown in the schematic of the VMPS in Figure 9(A). The VMPS has two input ports requiring two input signals with the quadrature phase relation. These can be provided by a quadrature VCO or poly-phase filters. The gains of the I and Q channels are controlled in opposition so that the total gain is kept constant and close to the maximum gain of a single channel. When the I channel has the maximum gain, the Q channel has the minimum and the VMPS has a phase shift ϕ_{0° that can be taken as the reference phase. Vice versa, when Q channel reaches maximum gain, the I channel has the minimum and the VMPS has a phase shift of $\phi_{0^\circ} + 90^\circ$. When the I and Q channels are set both at half gain at the same time, the combined gain is still the maximum gain of a single channel as for the other two states, meanwhile, the resulting phase shift is $\phi_{0^\circ} + 45^\circ$. According to this scheme, the 2-bit VMPS can be tuned over one quadrant with three states, i.e., 0°, 45° and 90°.

Figure 9(b) shows the die photo of the VMPS chip, which is 0.3 mm × 0.2 mm in core size and 0.75 mm × 0.5 mm with the pads included. Simulation results are shown in Figure 9(c), which illustrates 0.7 dB of gain variation around the nominal value of 2.3 dB gain. The phase tuning range is 90°. The absolute phase of the I channel at maximum gain state is taken as the reference (0°). When both channels are set to half gain, the phase shift is 42.1° at 24.125 GHz instead of the nominal 45°; meanwhile, at the quadrature state (Q channel at the maximum gain), an exact 90° phase shift is obtained. These phase

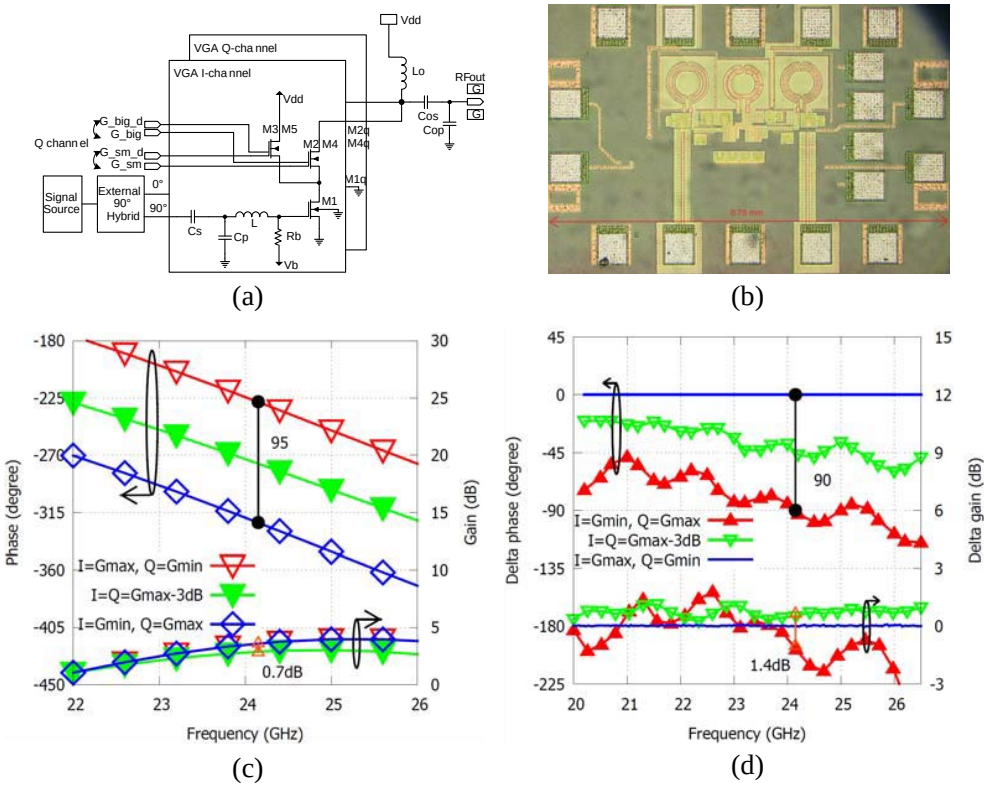

Figure 9. VMPS schematic, die photo, simulated and measurement results. (a) Schematic of the VMPS. (b) Die photo of VMPS. (c) VMPS simulated results. (d) VMPS measurement results.

Table 4. Performance comparison of VMPS.

Reference	[35][a]	[36]	[37]	Our VMPS
Frequency (GHz)	24	24	60	24.125
Technology (nm)	130	130	90	90
Tuning res. (°)	25	22.5	11.25	45
Gain (dB)	−2	−3	9	2
Phase imbalance (°)	N/A	11[b]	3	3
Gain imbalance (dB)	3	1.8[b]	N/A	1.4
Total power cons. (mW)	21.36	11.7	60	11.6

[a]Simulation results.
[b]RMS error.

and gain approximations are due to the discrete control of the VGA gain and mismatches in the layout.

Further approximations are introduced by the measurement setup. Indeed, the off-chip 90° hybrid, fabricated on a Roger 4003 substrate, is used to feed the two VMPS inputs, which is directly screwed on the GSGSG probe in order to minimize the imbalances and the losses. The hybrid shows a gain of −5 dB with the imbalance of 0.3 dB and less than 2° for the phase imbalance. From the VMPS measured results, shown in Figure 9(d), it can be seen that the overall (VMPS + hybrid) gain imbalance is +/ − 0.7 dB; meanwhile the phase is accurate to within 3°. Moreover, the measured nominal gain is 2 dB at 24 GHz.

The total consumption of the VMPS is 11.6 mW at 1.2 V power supply. In Table 4, the VMPS comparison with the state of the art shows very good performance in terms of gain, power and imbalance.

3.5. Voltage-Controlled Oscillator

The VCO scheme, as shown in Figure 10(a), is the usual cross-coupled pair, M1-M2, that provides the proper negative resistance to the LC tank. To couple with the low voltage supply, the current tail has been replaced with an inductor, L_{tail}, which does not reduce the headroom for the cross-coupled pair, but keeps the current constant at high frequency. Source follower buffers are used to reduce the VCO load pulling. Frequency tuning is achieved by using CMOS varactors. The whole design is parasitic-driven because the interconnections have parasitic capacitances, and the inductor and the varactor have resistive losses. The varactor losses are mitigated by connecting them in series with fixed, low-value, metal-insulator-metal (MIM) capacitors so that the varactor losses are slightly coupled with the LC tank. The slight coupling also improves the oscillator phase noise because the high tuning ratio of the varactor (which set the K_{VCO}) is reduced. The inductor is already optimized from the foundry with a thick metal layer. The parasitic capacitances are minimized by implementing a compact layout.

The measurement results, plotted in Figure 10(c) and Figure 10(d), show a frequency tuning range from 23.05 GHz to 23.93 GHz. The range is slightly (∼1%) lower than that of the ISM band because the effect of the parasitic is always underestimated in simulation, and needs to be compensated for in the next design iteration, likely by introducing a bank of switchable capacitors. The output power plot includes the cable losses of 6 dB therefore the oscillator on-chip power reaches −12 dBm. The power consumption is 10 mW at 1.2 V. The phase noise of the VCO has been measured by locking

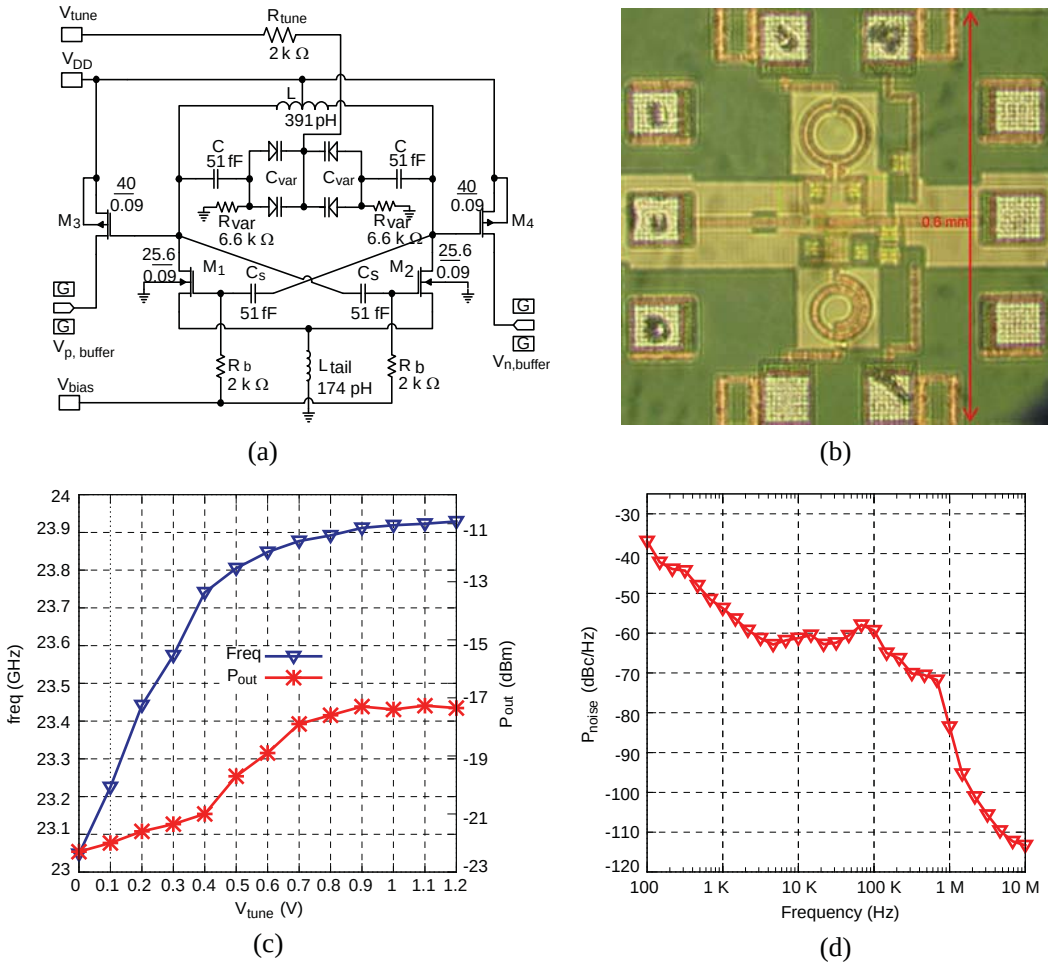

Figure 10. VCO schematic, die photo and measured results. (a) Cross-coupled VCO schematic. (b) Die photo of VCO. (c) VCO tuning range and output power without losses of cables and connectors. (d) Locked phase noise of the designed VCO with commercial PLL chip.

Table 5. Performance comparison of 24 GHz VCO.

Reference	[38]	[38]	[40]	Our VCO
Frequency (GHz)	22.8	23.7	24.0	23.5
Technology (nm)	130	90	130	90
Tuning range (%)	13	7.2	5.8	4.2
Output power (dBm)	4	−1.2	6[a]	−12
Phase noise (dBc/Hz) @ 1 MHz	−97	−102	−102	−85[c]
Phase noise (dBc/Hz) @ 2 MHz	−102	N/A	−112	−102[c]
Total power cons. (mW)	43	22[b]	64	10

[a]Power amplifier included.
[b]QVCO.
[c]External PLL chip measurement set-up.

the VCO with an off-chip PLL (ADF4107 by Analog Devices). The PLL circuit, implemented on an auxiliary printed circuit board, also contains a frequency divider chip (HMC447 by Hittite) and an LNA chip (HMC519 by Hittite) in order to satisfy the frequency and input power requirements of the PLL chip. The loop filter, also off-chip, has a 3 dB bandwidth of 100 kHz since the comparison frequency is 1 MHz. The measured phase noise plotted in Figure 10(d) shows the typical noise shape of a PLL synthesizer with an in-band phase noise of about −60 dBc/Hz, which is mainly due to the high value of the division ratio between the carrier frequency and the comparison frequency. The out-band phase noise is only −85 dBc/Hz at 1 MHz offset because of the loop filter bandwidth (1 MHz falls within the transition bandwidth) that could not be narrowed in the measurement setup. The noise quickly drops to −102 dBc/Hz at 2 MHz and −113 dBc/Hz at 10 MHz offset. Table 5 shows the comparison of our work with the state of the art. Our VCO shows the lowest power consumption. In order to compare the phase noise, the values at 2 MHz offset can be extrapolated from cited works by scaling the 1 MHz value of 6 dB per octave. In this way the −102 dBc/Hz measured at 2 MHz is only 6 dB worse than the concurrent work which consumes more power.

4. FE SYSTEM BUDGET ANALYSIS

Based on the system architecture proposed in Section 2.4 and the functional blocks developed in Section 3, the following sections will focus on the gain, noise figure and power consumption budget analysis of the two working modes of the FE. Other parameters such as linearity and filter selectivity are not considered for this budgetary analysis, which aims to show the feasibility of the architecture more than the development of an accurate model. Indeed, the missing blocks of the architecture, such as active I/Q mixers, a differential combiner, a PLL, an ADC, an IF amplifier and a tunable IF filter, are selected from the open literature and their parameters are used in the calculations.

4.1. Budget Analysis of the Doppler Radar Sensor Mode

When the FE works as a Doppler radar sensor, the block diagram in Figure 11 can be considered. The blocks selected from the open literature are tagged with the reference number between brackets while the blocks that have been implemented in this work are tagged with the name used in the previous sections and the parameters noted are the measured parameters.

First, the gain budget can be calculated. The necessary total receiver gain is estimated by the equation:

$$G_{RX}\,(\text{dB}) = G_{RF} + G_{IF} = 20\log\frac{V_{ADC,RMS}}{V_{R,radar}}, \tag{5}$$

where $V_{ADC,RMS}$ is the ADC full-scale range and $V_{R,radar}$ is the received signal amplitude.

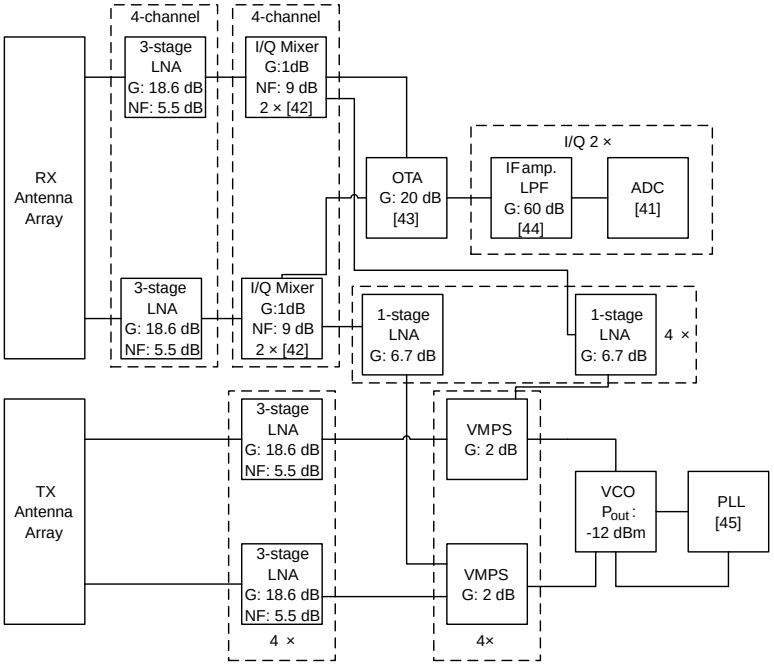

Figure 11. Block diagram in Doppler radar sensor mode.

The ADC block is taken from [41]. In this work, the full-scale range is 120 mV peak to peak. Meanwhile, the receiving power of the radar sensor is estimated by Eq. (2), which is rewritten:

$$\begin{aligned} P_{R,radar} &= P_{TX} + CPG_{TX} + G_{TX} - PL_{radar} + G_{RX} - LM \\ &= 1\,\text{dBm} + 12\,\text{dB} + 16.7\,\text{dB} - 152\,\text{dBm} + 16.7\,\text{dB} - 10\,\text{dB} \approx -116\,\text{dBm}. \end{aligned} \tag{6}$$

The calculated received power, i.e., −116 dBm, corresponds to 0.35 μV on 50 Ω. Thus, the voltage gain of the receiver path can be calculated by Eq. (5), which gives around 102 dB. The total receiver gain is the sum of the gain from the RF path (G_{RF}) and from the IF path (G_{IF}). The gain of the RF path has the contribution from one three-stage LNA, one mixer, one combiner and the coherent receiver process gain. The three-stage LNA can provide 18.6 dB of gain and 5.5 dB of NF. The specifications of the I/Q mixer can be selected from [43], which shows 1 dB of gain and 9 dB of NF. Four channels can be combined by an operational transconductance amplifier (OTA) with 20 dB of voltage gain [43]. The coherent addition provides 12 dB of signal gain according to the discussion in Section 2.1. Therefore, the IF path needs to provide a gain of: $G_{IF} = 102 - 18.6 - 1 - 20 - 12 \approx 50$ dB.

The IF amplifier and low-pass filter can be selected from [44], which shows an IF VGA tunable gain from 18 dB to 60 dB, a tunable low-pass bandwidth up to 32 MHz and a power consumption of 0.7 mW. The ADC in [41] is a five-bit flash ADC with 20 MHz of bandwidth and 28 mW of power consumption.

The gain budget in the LO path concerns the input LO power requirement of the active mixer, i.e., −3 dBm. The output power of the proposed VCO is −12 dBm. Therefore, after the VMPS gain of 2 dB, it still needs the gain of a single-stage LNA, i.e., almost 7 dB.

By applying the Friis formula to the blocks cascaded, a single-channel NF of 6 dB is worked out. This matches the desired value used in the radar range estimation in Section 2.1, which results in 60 meters of range.

In the transmitter path, the continuous-wave signal needs to be amplified before the antenna array. After the VMPS, the output power of the signal is −10 dBm. So it still needs an amplifier circuit used as a power amplifier, for example, one three-stage LNA, who has 18.6 dB gain and consumes 18 mW. The extra gain can be desired for the compensation of process-voltage-temperature variation, maybe adjusting the bias point for gain regulation.

Table 6 shows the power breakdown of the proposed FE in Doppler radar sensor mode. The total power is about 375 mW.

Table 6. Power consumption budget calculation of the Doppler radar sensor mode.

	Block	Quantity	Unit Pow. (mW)	Summed Pow. (mW)	Tot. Pow. (mW)
Receiver Path	3-stage LNA	4	18	72	195.9
	I/Q mixer [42]	8	6.9	55.2	
	Combiner [43]	1	12	12	
	IF amplifier & filter [44]	2	0.35	0.7	
	ADC [41]	2	28	56	
LO Path	VCO	1	10	10	107.3
	PLL [46]	1	33.3	33.3	
	VMPS	4	11.7	46.8	
	1-stage LNA	4	4.3	17.2	
Transmit Path	3-stage LNA	4	18	72	72
Total					375

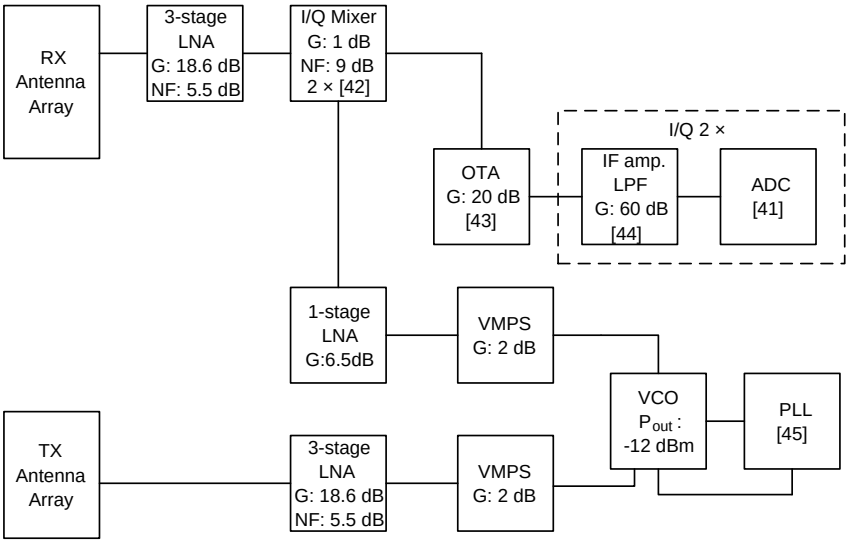

Figure 12. Block diagram in transceiver mode.

4.2. Budget Analysis of the Transceiver Mode

With the same methodology, the budget analysis of the transceiver mode is carried out. Figure 12 shows the block diagram of the components used in this working mode.

The gain budget of the receiving path is considered first. Recalling that the receiver sensitivity is $-85\,\text{dBm}$ ($17.7\,\mu\text{V}$ on $50\,\Omega$) and the ADC full-scale is $120\,\text{mV}_{PP}$, the receiver total voltage gain has to be approximately 68 dB. This can be achieved by using the same IF amplifier/filter already seen for the radar mode provided that the IF bandwidth is properly tuned so that both modes can work properly by sharing the hardware. As shown in Eq. (7), the receiver sensitivity is lower than for the radar mode because the IF bandwidth is wider, and the coherent gain does not appear because the Ph-A is not used.

$$\begin{aligned} P_{R,com.} &= P_{TX,com.} + G_{TX,com.} - PL_{com.} + G_{RX,com.} - LM \\ &= 1\,\text{dBm} + 14.9\,\text{dB} - 103\,\text{dBm} + 14.9\,\text{dB} - 10\,\text{dB} \approx -82\,\text{dBm}. \end{aligned} \tag{7}$$

Since the receiver path is exactly one channel of the radar mode, the single-channel NF is the same, i.e., 6 dB. The gain of the receiver path is around 68 dB, so the required gain for the IF path is 28 dB.

Table 7. Power consumption budget calculation of the transceiver mode.

	Block	Quantity	Unit Pow. (mW)	Summed Pow. (mW)	Tot. Pow. (mW)
Receiver Path	3-stage LNA	1	18	18	100.5
	I/Q mixer [42]	2	6.9	13.8	
	Combiner [43]	1	12	12	
	IF amplifier & filter [44]	2	0.35	0.7	
	ADC [41]	2	28	56	
LO Path	VCO	1	10	10	71
	PLL [45]	1	33.3	33.3	
	VMPS	2	11.7	23.4	
	1-stage LNA	1	4.3	4.3	
Transmit Path	3-stage LNA	1	18	18	18
Total					189.5

Table 8. Summarized front-end performance estimations in two working modes.

Reference	Doppler radar mode	Transceiver mode
G_{RX} (dB)	102	68
NF (nm)	6	6
Sensitivity (dBm)	-82	-85
P_{TX} (dBm)	7	1
SNR_{RX} (dB)	12	12
Range (m)	60	140
Power (mW)	375	190

Hence, the selected IF amplifier and LPF are reusable. Since all the assumptions made in the range calculation are valid, the calculated range of 140 meters in Section 2.1 is confirmed.

Similarly, the transmission path is just one channel of the radar array and therefore the same amplification (i.e., one three-stage LNA) is necessary to increase the power of the BPSK signal generated by the VMPS to the 1 dBm of the desired transmitted power.

Table 7 shows the power breakdown of the transceiver mode. The total power is about 190 mW.

5. CONCLUSIONS

This paper proposes a 24 GHz Ph-A FE for a smart streetlight application. This FE has two innovative points: first, the Ph-A scheme is used in a Doppler radar sensor for a low-cost and low-power IC in CMOS technology; secondly, communication functionality is added to the Doppler radar sensor enabling networking between sensors by reusing the same FE. The design and characterization of some fundamental building blocks of the FE, namely the LNAs, the VGA, the VMPS and the VCO developed in 90 nm CMOS technology, are reported. A practical method for parasitic extraction is shown and its results are compared with the measurements. Moreover, the performances of our blocks compares favorably with the state of the art, offering power saving without sacrificing other performances. A realistic scenario for the streetlight application is modeled and used for the calculation of the FE specification requirements. A radar range of 60 m and a communication range of 140 m are given as fundamental requirements for reliable communication between streetlight sensors and for continuous radar coverage. The feasibility of the entire FE is proved by means of a system analysis based on measured block performances. The latter are related to the designed blocks and to ones selected from

the open literature.

Table 8 shows the summarized performance calculations for both working modes. They are achieved with 190 mW and 375 mW of power consumption in transceiver and radar modes respectively. These are state of the art results for a 24 GHz Ph-A FE that combines Doppler radar and transceiver functionalities. To the authors' knowledge, this Doppler radar FE is unique, and can become the basic node of a future WSN for smart lighting systems and intelligent transportation infrastructures.

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