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# Comparison of Packaging Technologies for RF MEMS Switch

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**Abstract**—The present paper describes an integrated approach for design, fabrication and encapsulation of RF MEMS switches in view of the optimal performance subsequent to packaging. 'Top and bottom contact' fabrication approaches are explored using different RF MEMS switch topologies. In the 'bottom contact package (BCP)' the packaging cap alignment is less critical as compared to the top contact packaging (TCP) approach where contact via is an integral part of the cap. In this case, the connection layout through silicon via holes is independent of the cavity geometry. For the devices under consideration, bulk etched silicon cavity height has been optimized to 50 µm for optimal RF performance, e.g., isolation and insertion loss. Parasitic effects of top silicon cap are reduced by altering CPW impedance. Mechanical parameter damping is simulated for different cavity heights and found to be independent from cavity height after 20 µm onwards.

## 1. INTRODUCTION

The expansion of wireless communication applications and specific trend towards miniature energy-efficient devices is leading the development of RF-MEMS devices such as switches, antennas, and filters as futuristic devices. RF MEMS components in general offer small size, lower power consumption, lower losses, higher linearity, and higher $Q$ factors over conventional communication components [1]. In the last two decades, research work has been concentrated on MEMS switch design and fabrication [1–10] leading to successful demonstration of RF MEMS switches of various types [3–7]. In general, a reliable low cost packaging without degradation in performance is considered to be the last barrier in commercialization of MEMS devices. Packaging contributes to about 75% of the total cost of a device [1] and the performance and reliability of a device strongly depend on its packaging. The diverse nature of MEMS devices also makes it mandatory to customize the packaging to the specific requirements of devices and applications, with emphasis on the cost, performance, and reliability [8–12].

In this work, design analysis based on top and bottom contact methods for RF MEMS switch packaging is presented. As an example, two RF MEMS switches [7, 9] as shown in Figure 1 have been considered for current analyses. Two types of packaging approaches are discussed: the lateral packaging and the vertical packaging. In the lateral packaging (LP) approach, electrical connections are laterally brought outside the bonded cavity as shown in Figure 2(a). The approach is simple and easy to implement. However, wafer level packaging (WLP) is not possible in this case. It also results in longer signal lines and larger wafer area consumption. Depending upon the electrical connection approach, the vertical packaging can further be subdivided as top contact packaging (TCP, the conventional approach) [11–15] and bottom contact packaging (BCP) as shown in Figures 2(b) and (c) respectively. In vertical packaging, connections are provided either through the cap or device wafer in a direction perpendicular to the wafer and no lateral extension is required, thus saving the wafer area.

In the conventional TCP, electrical connections are made through silicon cap using 'through silicon via' (TSV) technology. Wafer and package alignment is critical as the alignment margin is decided by

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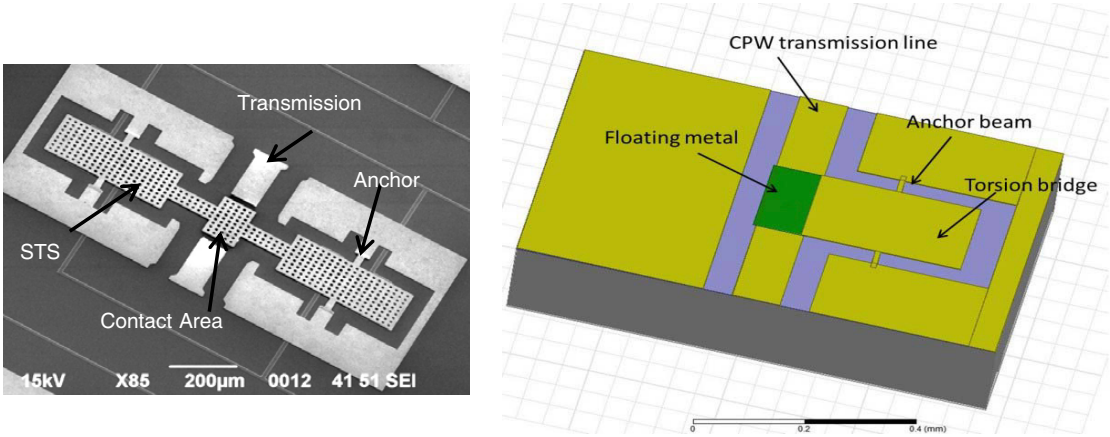
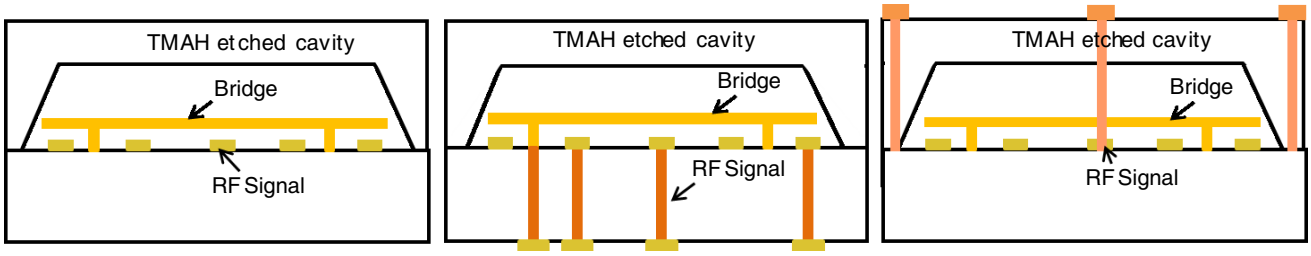


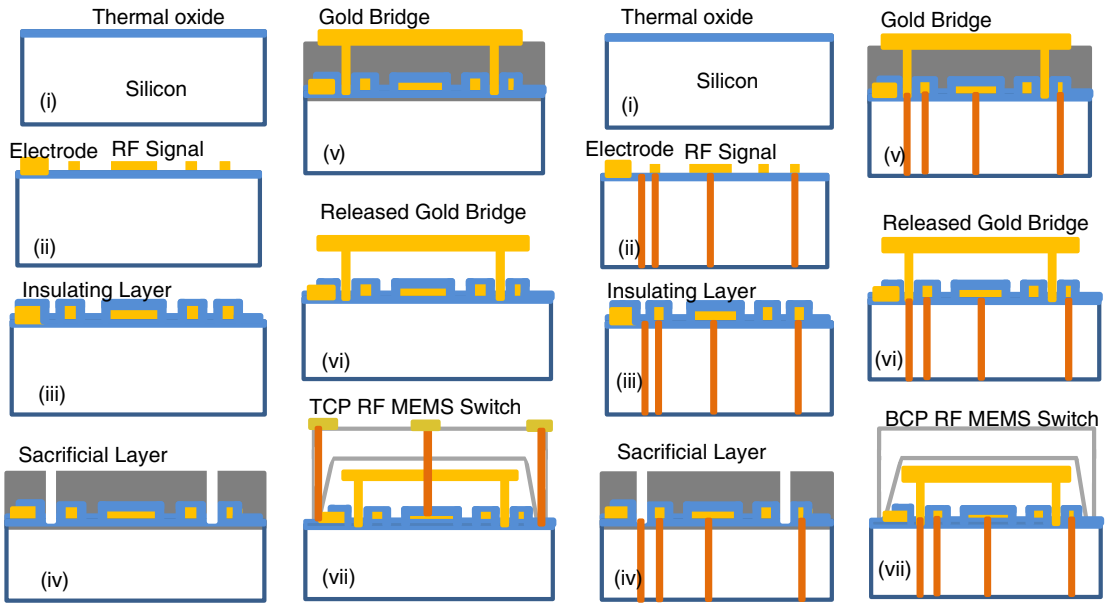

(a) Symmetric Toggle Switch (b) Torsional Switch

**Figure 1.** 3-D view of RF MEMS capacitive (a) symmetric toggle switch and (b) torsional switch.




(a) Lateral Packaged (LP) (b) Bottom Contact Packaged (BCP) (c) Top Contact Packaged (TCP)

**Figure 2.** Cross sectional view of (a) LP, (b) BCP and (c) TCP RF MEMS switch.




(a) TCP (b) TCP

**Figure 3.** RF MEMS switch fabrication process flow for (a) TCP and (b) BCP.

contact pads and TSVs geometry. A proper electrical connection to external world requires soldering ball reflow. On the other hand, in BCP, electrical connections are through the silicon wafer using TSV technology. In this approach TSVs, connections and device are fabricated simultaneously on the same wafer. Since the top cap is free of TSVs, the tolerance in alignment accuracy can be relaxed.

## 2. FABRICATION PROCESS

The RF MEMS switch fabrication without packaging has already been discussed in [7]. In the case of LP, subsequent to device fabrication, wafer is sealed with cavity and diced. In TCP, in addition to cap bonding, electrical connections are also realized through packaging cap as shown in Figure 3(a). In order to ensure low resistivity inter-connects, soldering reflow at connection pads entails high temperature and alignment of connection pads with packaging cap.

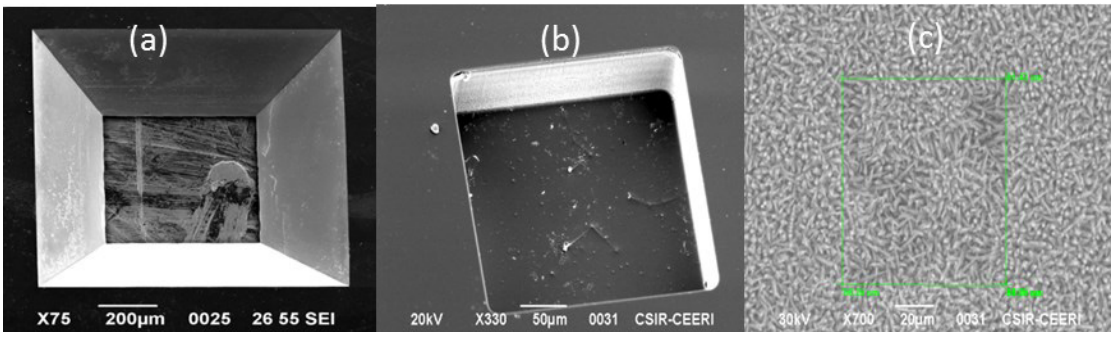



**Figure 4.** (a) and (b) TSV with TMAH etching and DRIE, (c) completely filled TSV.

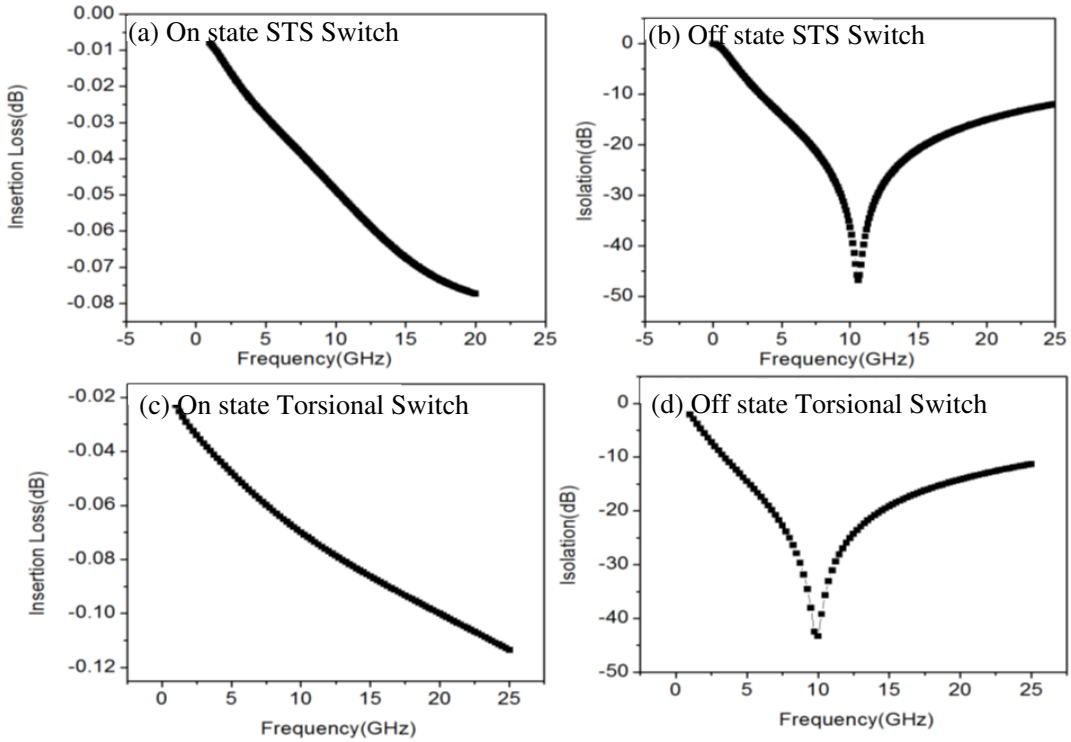


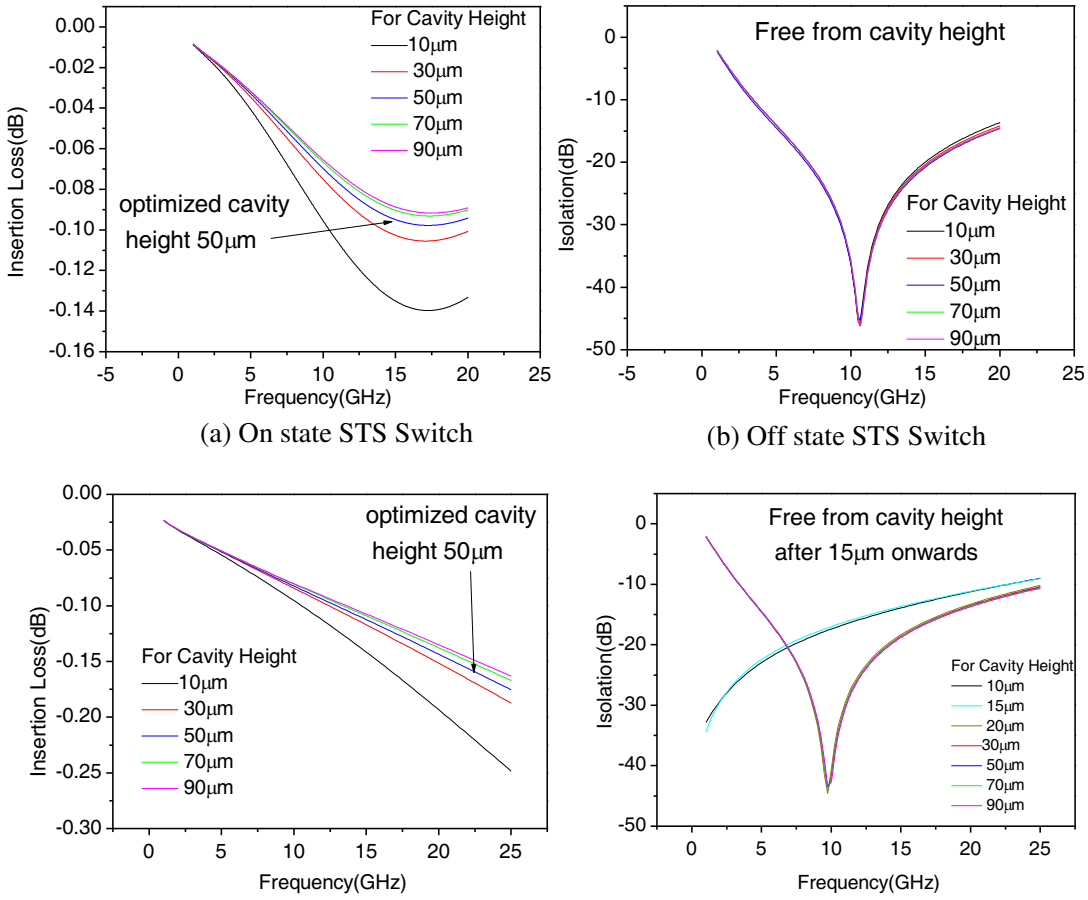

**Figure 5.** (a), (b) and (c), (d) are on state and off state response of RF MEMS STS and torsional switch without packaging.

In BCP, TSVs are made in the silicon wafer prior to device fabrication and filled with electroplated copper. The subsequent fabrication steps are similar to the process reported in [7]. Switches are fabricated on via filled wafer as shown in Figure 3(b). High resistive silicon top cavities are etched using TMAH in a separate process and diced. Prior to device wafer dicing, each device is covered with silicon cavity using chip aligner cum cavity bonder. The last step is to dice the packaged devices.

TSV formation and filling are the key processes in MEMS packaging. TSVs are made using both TMAH and DRIE process as shown in Figures 4(a) and (b). Using TMAH, minimum opening required for through hole on 2" wafer of thickness 275 µm is $275 * \tan(54.7^\circ) = 389$ µm. Therefore, DRIE process is preferred for smaller devices. Seed layer (Cr/AU) deposition is done followed by copper electroplating process to fill TSV. Reverse pulse plating supply is utilized for plating in order to avoid edge crowding and make uniform deposition. Completely filled via is shown in Figure 4(c).

## 3. SIMULATION RESULTS & DISCUSSION

Electrical parameters such as insertion loss and isolation are optimized for RF MEMS switch in view of the packaging using high resistive (HR) silicon cavity. RF MEMS capacitive type switches namely STS and torsional switch developed in our laboratory [7, 9] are used as reference for package design. The design and simulations are carried out using commercially available software 'High Frequency Structure Simulator (HFSS)' to optimize the cavity height with due considerations to parasitic elements added by cavity. On and off state response of an unpackaged switch is shown in Figure 5 where insertion loss




(a) On state STS Switch

(b) Off state STS Switch

(c) On state Torsional Switch

(d) Off state Torsional Switch

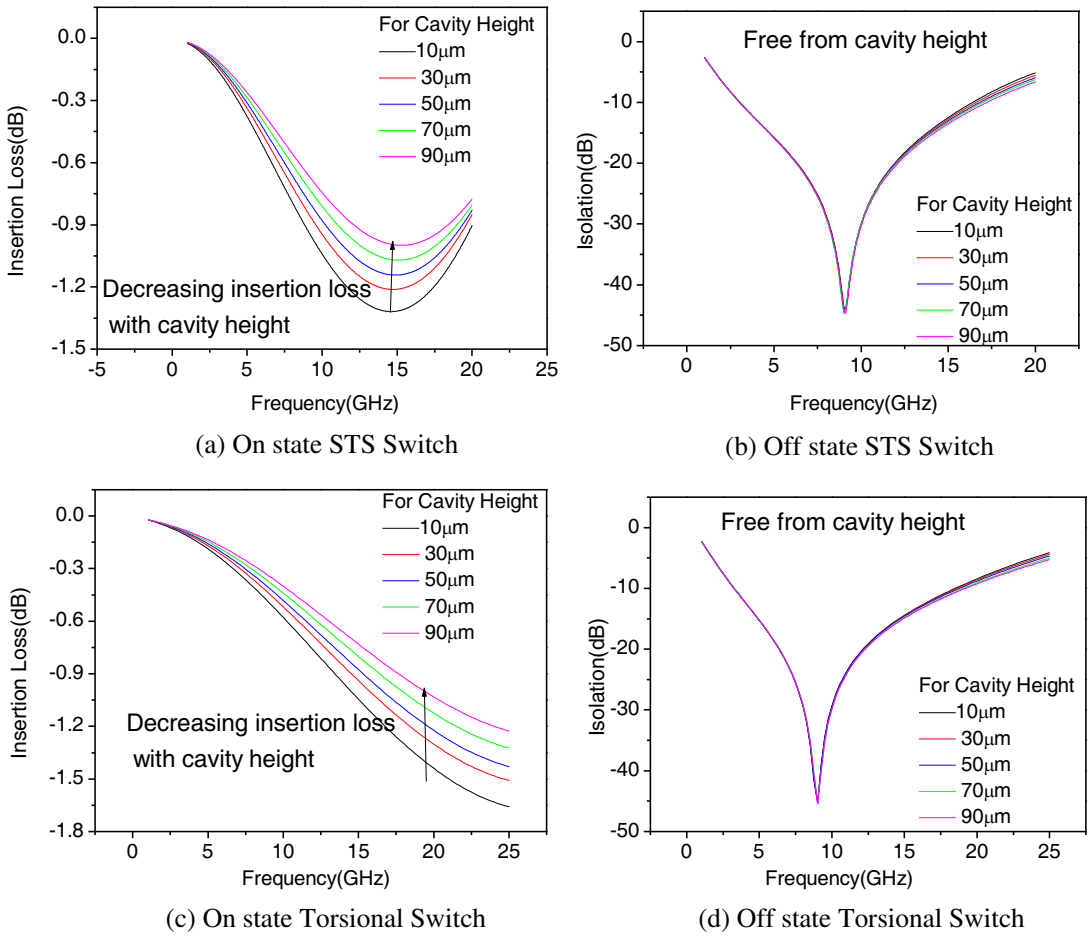
**Figure 6.** (a), (b) and (c), (d) are on state and off state response of LP RF MEMS STS and torsional switch respectively.

is −0.05 to −0.07 dB at 8–10 GHz for STS and torsional configuration. Isolation is better than −40 dB for both switches.

Figures 5, 6, and 7 demonstrate the on and off state response of LP, TCP and BCP approaches respectively for STS and torsional switch. In the off state, isolation is better than −40 dB at 8–12 GHz in all types of packaging approaches and is independent of the cavity height in the case of STS switch.

For torsional switch, the optimal isolation is obtained with a cavity height of more than 20 µm. In on state, insertion loss changes with cavity height and differs for all cases. LP switch has minimum insertion loss of −0.07 dB at 8–12 GHz for cavity height of 50 µm as compared to −0.8 dB at 8–12 GHz for vertical packaging (TCP and BCP) for STS switch. Similar behavior is observed for torsional switch; except insertion loss magnitude. In the case of vertical packaging, as TSVs are made either in cavity or wafer itself, the additional impendence alters the standard 50 ohm impedance of CPW line. This increases the insertion loss in vertical packaging as compared to lateral packaging.

The selected CPW configuration made on silicon substrate with SWS as 55-90-55 µm has 50 ohm impedance. Packaging with silicon cap results in passing fringing field lines through silicon cap ($\varepsilon = 12$), rather than air ($\varepsilon = 1$) as shown in Figure 9. Hence increase in capacitance take place which decreases the CPW impedance and increases insertion loss. With increase in cavity height effect of field lines is reduced and results in lower losses. In BCP, after cavity height of 30–50 µm, field line effect is negligible. In TCP, electrical signals are taken from top through silicon; hence field effect will decrease with cavity height. Total elimination of parasitic through cavity is not achieved with change in cavity height. The analytical calculations of CPW impedance are beyond the scope of present paper and detailed analysis is discussed in [18].



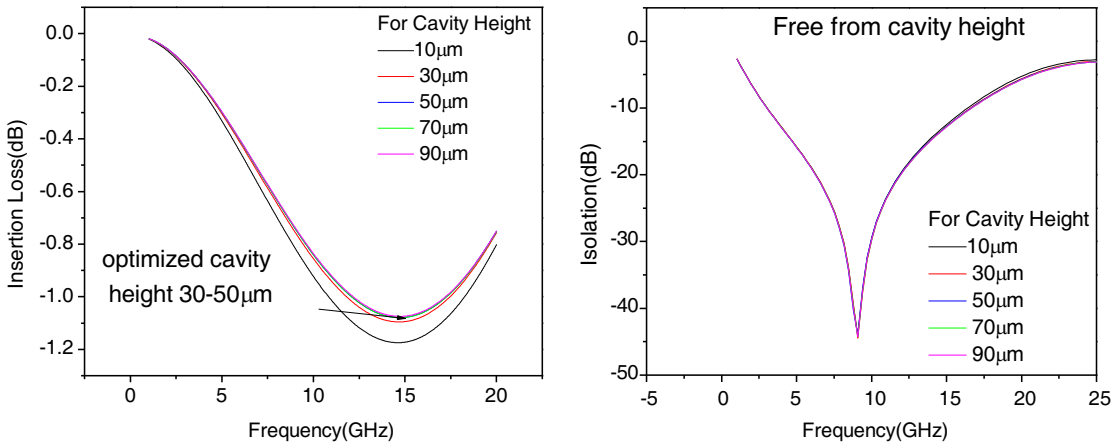

(a) On state STS Switch

(b) Off state STS Switch

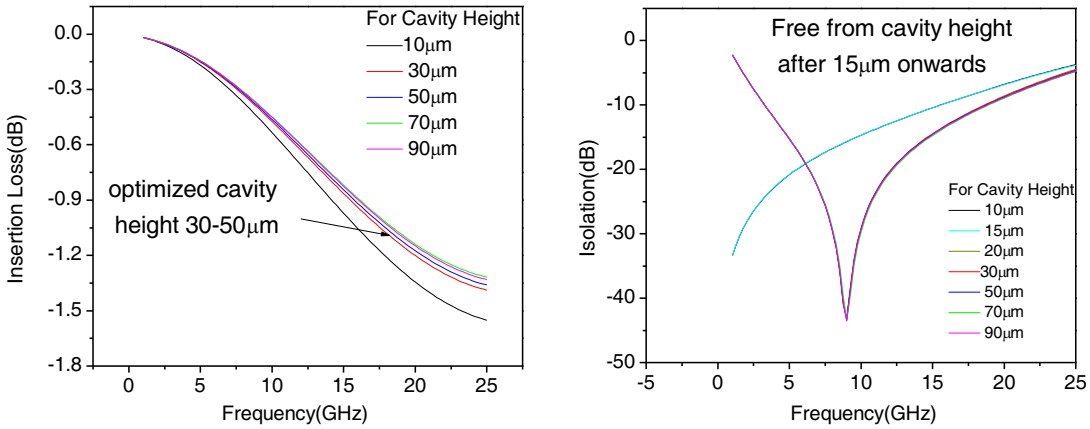
(c) On state Torsional Switch

(d) Off state Torsional Switch

**Figure 7.** (a), (b) and (c), (d) are on state and off state response of TCP RF MEMS STS and torsional switch respectively.

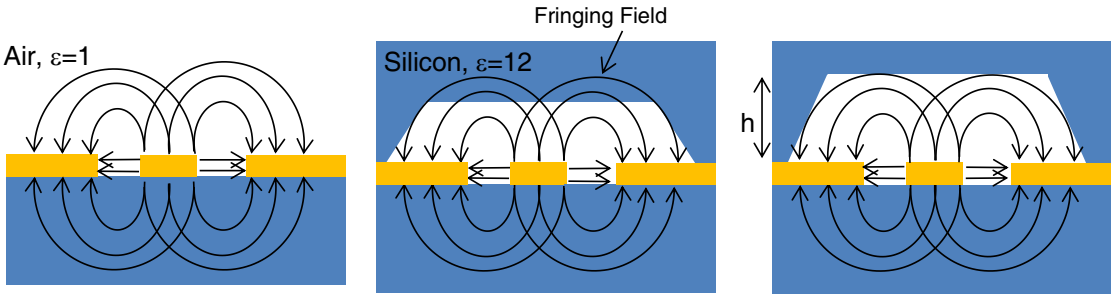



(a) On state STS Switch (b) Off state STS Switch




(c) On state Torsional Switch (d) Off state Torsional Switch

**Figure 8.** (a), (b) and (c), (d) are on state and off state response of BCP RF MEMS STS and torsional switch respectively.




(a) Without Packaging (b) With Packaging (c) Packaged with optimized

**Figure 9.** Effect of fringing field lines on cavity height.

### 3.1. Electrical Analysis

In case of RF MEMS capacitive switch, on state capacitance is very small (2–80 fF) [7, 9] and insertion loss is directly co-related to capacitance value. Fringing capacitance also lies in same range (20–60 fF) [19]. Therefore fringing field effect is significant and insertion loss is affected by parasitics added by top cavity. Whereas, in off state, capacitance is of the order of 2–10 pF and parasitic capacitance has negligible effect on isolation. Isolation is almost independent from cavity height.

Parasitic effect is minimum in LP as compared to BCP and TCP. Increased capacitance due to

packaging leads to decrease in overall impedance of CPW line as its impedance is inversely proportional to square root of capacitance. Therefore to compensate parasitic capacitance effect, CPW impedance in increased by increasing the gap between signal line and ground. In case of LP, as shown in Figure 10(a) for fixed cavity height (50 µm) and signal width (90 µm), CPW gap is increased from 50 µm to 250 µm to optimize insertion loss and minimum loss is obtained at 150 µm gap corresponding to 69 ohm CPW line. Parasitics capacitance added by packaging loads the CPW line and converts back it into 50 ohm signal line. Insertion loss is reverted back from −0.12 dB to 0.08 dB.

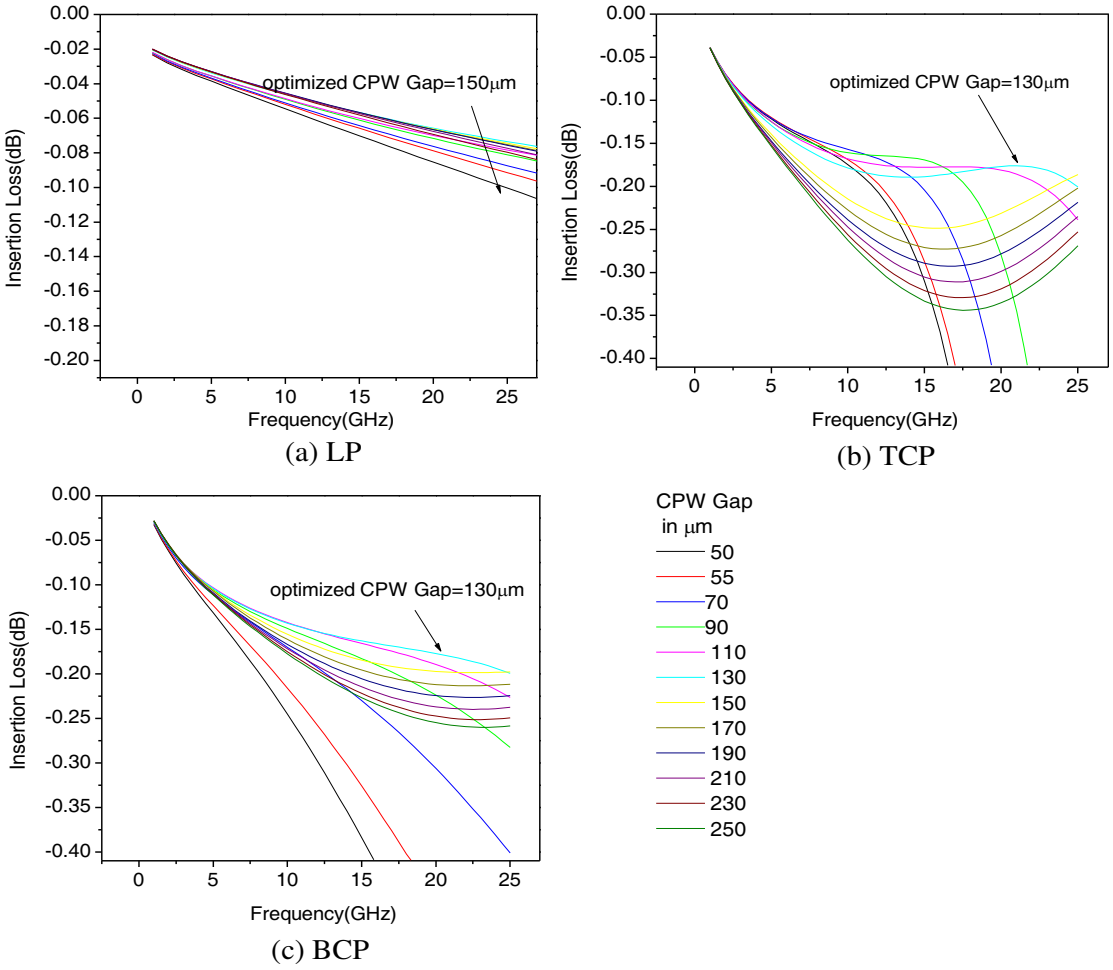



**Figure 10.** (a), (b) and (c) are on state response of LP, TCP and BCP RF MEMS switch for torsional configuration.

In the case of BCP and TCP for fixed signal width of 90 µm, optimized CPW gap is 250 µm corresponding to 81 ohm CPW which leads to increase in overall switch size. To cope with size, higher impedance of CPW is archived by reducing signal line width from 90 µm to 40 µm. Optimization of minimum insertion loss for BCT and TCP is done by changing the CPW gap from 50 µm to 250 µm and optimized gap is 130 µm as shown in Figures 10(b) and (c) corresponding to 81 ohm CPW. Insertion loss is decreased from −1.2 dB to −0.15 dB still larger than unpackaged due to induction loss caused by TSVs.

### 3.2. Mechanical Analysis

Involvement of moving parts in MEMS structures results in customizing new packaging techniques different from traditional IC packaging. Damping coefficient plays a key factor in RF MEMS packaging. For switching applications, bridge should be over damped to avoid fluctuations. Critical damping

coefficient for torsional configuration is 1.34e-5 Ns/m extracted using Coventorware. Impact of cavity height on damping coefficient is explored at 1 atm pressure inside the cavity. Damping coefficient has almost exponential dependent on cavity height till 10 µm and constant onwards as shown in Figure 11. Damping coefficient is 1.15e-4 Ns/m for packaged torsional switch after 20 µm which is more than its critical value. Switch will operate in over damped conditions without bouncing back. Cavity height beyond 20 µm for RF MEMS switch is acceptable for mechanical analysis like damping. Being mechanical in nature, it is independent of the type of packaging, e.g., LP, TCP and BCP.

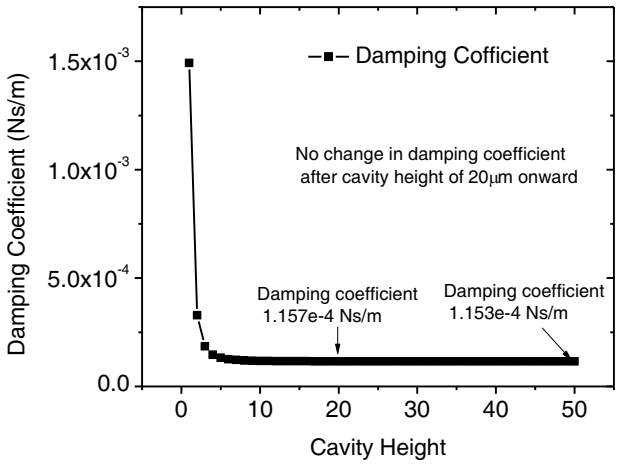



**Figure 11.** Top cavity height impact on damping coefficient of RF MEMS switch.

## 4. CONCLUSIONS

Vertical packaging is preferred over lateral packaging as wafer area consumption is minimal, and batch processing with wafer level packaging is possible. Among vertical packaging approaches, bottom contact packaging (BCP) is found to be easier as compared to top contact packaging (TCP). In this approach, TSVs are made prior to device fabrication. The alignment error is only limited by lithography and connection fabrication does not require high temperature soldering reflow.

Isolation is independent of the cavity height and is better than −40 dB in both lateral and vertical packaging cases for STS switch configuration. Almost similar behavior is observed in torsional switch, except minimum cavity height requirement is 20 µm. Insertion loss behavior is also similar for both STS and torsional switches. Insertion loss is found to be −1.2 dB for cavity height of 30–50 µm at 8–10 GHz in both TCP and BCP approaches and further change in insertion loss is insignificant with increase in cavity height. Insertion loss is reduced from −1.2 dB to −0.15 dB for torsional switch configuration by altering CPW from 75-90-75 to 130-40-130 configuration.

BCP appears to be a better choice than TCP, and cavity height of 50 µm is optimal for MEMS devices packaging.

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