

Effect of Second and Third Harmonic Input Impedances in a Class-F Amplifier

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Abstract—In this paper, the design of a class-F radio frequency power amplifier with a multiharmonic input transmission line network is presented. Harmonic signal components at the gate come from several sources including nonlinear device capacitances and imperfect output harmonic terminations that create harmonic components that are fed back to the gate through the gate-drain capacitance. The effect of these harmonic generation mechanisms and the potential to shape the gate waveform to improve power efficiency are investigated. The study shows that a second harmonic short is most beneficial and the effect of a third harmonic termination is less significant. The concepts are applied to the design of a 10 W GaN class-F amplifier and the design is supported by theoretical, simulation and experimental results. The fabricated design has a measured drain efficiency of 78.8% at an output power of 40.5 dBm for a frequency of 990 MHz. The amplifier was also tested with a 8.8 dB peak-to-average power ratio 5 MHz WCDMA signal. With the modulated signal, the adjacent channel power ratio was -33.1 dBc at a drain efficiency of 46.1% without predistortion correction.

1. INTRODUCTION

The need for high efficiency power amplifiers (PA) in wireless communication systems continues to motivate research work focused on optimizing PA circuit designs and evaluating trade-offs between different circuit topologies. Examples of high efficiency amplifier circuits include harmonically tuned amplifiers such as class-F [1–6] and switch-mode amplifiers based on class-E [7] and class-D [8]. In this paper, the focus is on class-F amplifiers and specifically the relationships between power efficiency and harmonic input impedances at the gate of the power device.

In studying the effect of harmonic input impedance at the gate of a class-F amplifier several questions arise. First, why are there harmonics at the gate terminal and where do they come from? Second, how sensitive is the design to harmonic impedance control at the gate and what are the best impedance choices for controlling the harmonics? Within the framework of these questions, the scope in this paper is limited to a consideration of the second and third harmonic components of the current and voltage waveforms. In practical class-F designs, harmonic control up to the third harmonic provides a good balance between power efficiency, matching circuit complexity, and matching circuit losses.

Class-F amplifiers are inherently nonlinear and use harmonic impedance control in the output circuit to shape the voltage waveform at the drain. In an ideal class-F design, the device is cut-off for half the cycle similar to class B, and harmonics are created in the output circuit because the drain current is a half sinusoid. Harmonic termination impedances in the output circuit preserve the shape of the current waveform by shorting even harmonics. The drain voltage waveform is shaped to reduce overlap with the current waveform by open termination impedances at odd harmonics. There are however other important mechanisms that create harmonic frequency components including deviations from the class B bias point, nonlinear device capacitances [9], and nonlinear device transconductance.

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Of these mechanisms, nonlinear gate-source capacitance C_{gs} and nonlinear gate-drain capacitance C_{gd} can directly create harmonic components at the gate. There are also feedback mechanisms including C_{gd} and source inductance which can couple drain harmonics to the gate. For example, an imperfect second harmonic termination in the output match creates a second harmonic voltage component that can be coupled to the gate through C_{gd} . The effect of harmonic signal components at the gate is that the gate waveform is not sinusoidal and consequently the drain current waveform deviates from an ideal half sinusoidal shape. Therefore harmonic termination impedances at the gate can be used to shape both the gate waveform and the drain current waveform.

The relationship between power efficiency and input harmonic impedances for class-F amplifiers has been studied by others [10–16] and a summary is presented in Table 1. Most work listed in the table has focused on evaluating the effect of fundamental and second harmonic impedance terminations at the input of the device. In these papers, the mechanisms that generate harmonics in the device have been less important, and the work has focused on investigating harmonic termination impedances using harmonic load pull and time domain techniques. Although these techniques are general and can be extended to all harmonics, the experimental work presented in these papers has been limited to circuits with input harmonic terminations for fundamental and second harmonic impedances.

Table 1. Class-F amplifier designs with input harmonic termination networks.

Ref.	Type	Device	Input Harmonics	Approach
[10]	class-F, class-F ⁻¹	GaN	$f_o, 2f_o$	harmonic tuning
[11]	class-F, class-B	PHEMT	$f_o, 2f_o$	device level
[12]	class-F, class-F ⁻¹	AlGaAs/GaAsN	$f_o, 2f_o$	phase relationship
[13]	class-FG, class-E	GaAs MESFET	$f_o, 2f_o$	power balance
[14]	class-F	Power MESFET	$f_o, 2f_o$	load/source pull
[15]	class-FG	Power MESFET	$f_o, 2f_o, 3f_o$	phase relationship
[16]	class-F	PHEMT	$f_o, 2f_o, 3f_o$	load/source pull
This work	class-F	GaN HEMT	$f_o, 2f_o, 3f_o$	device level

This paper extends the investigation of input harmonic impedance to include the effect of third harmonic terminations on the power efficiency of a class-F amplifier. A systematic comparison of the power efficiency for a design with fundamental, second harmonic, and third harmonic terminations is made. The study begins with simulations of a simplified device model where the relationship between device capacitances and the harmonic levels at the gate are investigated. The impact of the gate to drain capacitance, C_{gd} , is particularly important as it provides feedback from the output to the input. The feedback, combined with imperfect output harmonic termination impedances, can lead to the injection of both odd and even harmonics to the gate terminal.

Simulation studies with the device model show that power efficiency is strongly dependent on second harmonic impedances at the gate and relatively insensitive to third harmonic impedance termination conditions. The model is also used to investigate the sensitivity of the design to nonlinear device capacitances. A comparison is made between a model with linear capacitances and a model with nonlinear capacitances. Without a second harmonic impedance termination, the discrepancy is significant, but with the addition of a second harmonic short, the sensitivity to nonlinear device capacitances is reduced significantly. Once a second harmonic impedance is created, the improvement in power efficiency for a third harmonic termination is much smaller. Therefore, the simulation work gives further insight into how harmonic terminations desensitize a design to nonlinear device capacitance.

As a verification of the input harmonic study, an experimental prototype of a class-F amplifier was built. The design uses a 10 W GaN power device from Cree and includes fundamental, second and third harmonic matching networks in both the input and output circuits. The experimental work is new and includes a third harmonic input impedance which has not been reported in other experiment results [10–16].

The paper is organized as follows: In the next section, a simplified device model is shown for the unpackaged Cree device. The model is used in harmonic balance simulations of a class-F power amplifier

with different input harmonic termination conditions. After drawing conclusions on the input harmonic termination network, the model is extended to include package parasitics. The design methodology for implementing a class-F amplifier with third harmonic input and output networks is described in Section 3, and the paper concludes with simulated and measured results to verify the design concepts.

2. HARMONIC ANALYSIS

2.1. Device Model

In this work, an experimental design of a class-F amplifier is implemented with a 10 W Cree GaN HEMT (model CGH40010). Although a comprehensive large signal model for the device is available from Cree, it is difficult to use this model to gain insight into the mechanisms which create gate harmonics as well as investigate the sensitivity of the design to device parameters. Therefore, we begin with a simplified device model that is extracted from a large signal die level device model for the Cree CGH60015D. Later, in Section 3, the model is extended to include the device package and the implementation of the harmonic networks includes compensation for the package.

A simplified device model is shown in Figure 1. The device model consists of a nonlinear transconductor, nonlinear device capacitances (C_{gs} , C_{gd} and C_{ds}), terminal resistances (r_g , r_d and r_s) and terminal inductances (L_g , L_d and L_s). The model parameters are obtained by matching components in the simplified model with extracted values of y or z parameters obtained from the large signal model of the die. The method is similar to constructing equivalent device models from experimental results [17].

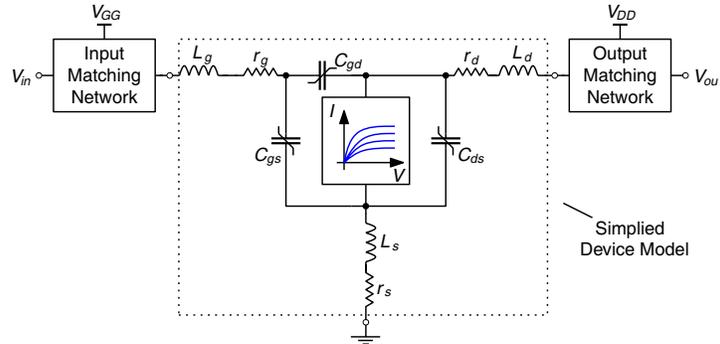


Figure 1. Class-F amplifier with simplified device model.

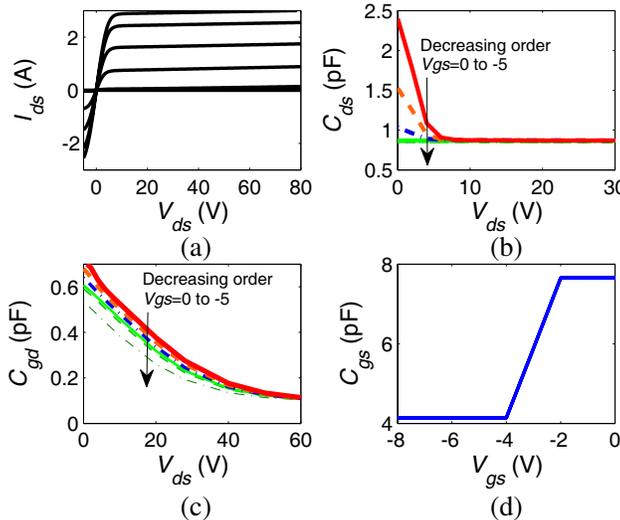


Figure 2. Cree GaN HEMT (CGH60015D) device characteristics: (a) DC-IV curve, (b) drain-source capacitance, (c) gate-drain capacitance, and (d) gate-source capacitance.

The DC-IV characteristics and nonlinear capacitances for the simplified model are shown in Figure 2. The other device model values are $r_g = 0.6 \Omega$, $r_d = 0.62 \Omega$, $L_g = 92 \text{ pH}$ and $L_d = 88 \text{ pH}$. The values for r_s and L_s are negligible relative to other components in the model and they are set to zero. As shown in Figures 2(b) and (c), the extracted values for the capacitances, especially C_{gd} , show significant variation with drain-source voltage. Although nonlinear device capacitances create harmonics, C_{gd} inherently provides feedback from the drain to gate and even a linear C_{gd} will also lead to harmonics at the gate. The variation in the device capacitances over the operating range of the device are summarized in Table 2. The table also includes the nominal device capacitances given on the Cree datasheet for the die, model CGH60015D [18].

Table 2. Summary of device capacitances for a Cree GaN HEMT (CGH60015D).

Model				Model	Datasheet
$V_{gs} = -5 \text{ V to } 0 \text{ V}, V_{ds}=0 \text{ V to } 60 \text{ V}$				$V_{gs} = -8 \text{ V and } V_{ds}=28 \text{ V}$	$V_{gs} = -8 \text{ V and } V_{ds}=28 \text{ V}$
Capacitance	Min.	Max.	Linear	Value	Typical
C_{ds}	0.87 pF	2.4 pF	0.92 pF	0.87 pF	0.9 pF
C_{gd}	0.1 pF	0.7 pF	0.36 pF	0.19 pF	0.2 pF
C_{gs}	4.14 pF	7.65 pF	6.17 pF	4.14 pF	4.1 pF

2.2. Output Matching Network

The transmission line model for the output matching network (OMN) is shown in Figure 3. For ideal class-F [19, 20] operation, the input impedance of the OMN looking towards the load is

$$Z_{\text{OMN}} \begin{cases} Z_{L,\text{opt}} & f_0 \\ \infty & (2n + 1) f_0 \\ 0 & 2n f_0. \end{cases} \quad (1)$$

In this equation, $Z_{L,\text{opt}}$ is the optimum load at the fundamental frequency f_0 , and n is a positive integer denoting the harmonic number. For this work, the OMN provides terminations for the first, second and third harmonics. As described later in Section 3, the combination of $TL_{\text{out}1}$, $TL_{\text{out}2}$ and $TL_{\text{out}3}$ provides a short at the second harmonic and an open at the third harmonic at the drain terminal of the device. A complex conjugate match ($Z_{L,\text{opt}}$) for maximum power transfer at the fundamental frequency is implemented with a single stub matching circuit consisting of $TL_{\text{out}4}$ and $TL_{\text{out}5}$.

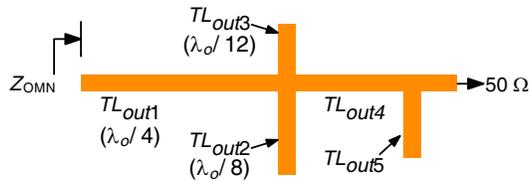


Figure 3. Output matching network (OMN) structure.

2.3. Simulation Experiments

A series of simulation experiments were run to compare the performance of class-F amplifier designs with different harmonic terminations at the gate. Simulation experiments were also run to compare power efficiency with linear device capacitances, nonlinear device capacitances, and imperfect output matching networks which generate even harmonics in the voltage waveform as well as odd harmonics. The results were generated from harmonic balance simulations run in Keysight Technologies Advanced

Design System (ADS). The complete simulation model with provisions up to third harmonic termination impedances at the gate is shown in Figure 4.

Before describing the results of the simulation experiments, an overview of the class-F amplifier design is presented. The amplifier is designed for a fundamental frequency of 990 MHz. The drain bias (V_{DD}) is 30 V and the gate bias (V_{GG}) is -2.6 V. The optimum load and source impedances at the fundamental frequency were found using source and load pull [21] test benches in the simulator. The transmission line elements TL101 and TL102 in Figure 4 implement the fundamental frequency source match, and the transmission lines TL109 and TL110 implement the fundamental frequency output match. The output matching circuit consists of three other transmission lines, TL106, TL107, and TL108, which create a second harmonic short and third harmonic open at the drain. We remark that further optimization of the third harmonic stub can be made to compensate for the output reactance of the device at the third harmonic. However, the optimization of the output matching network with the

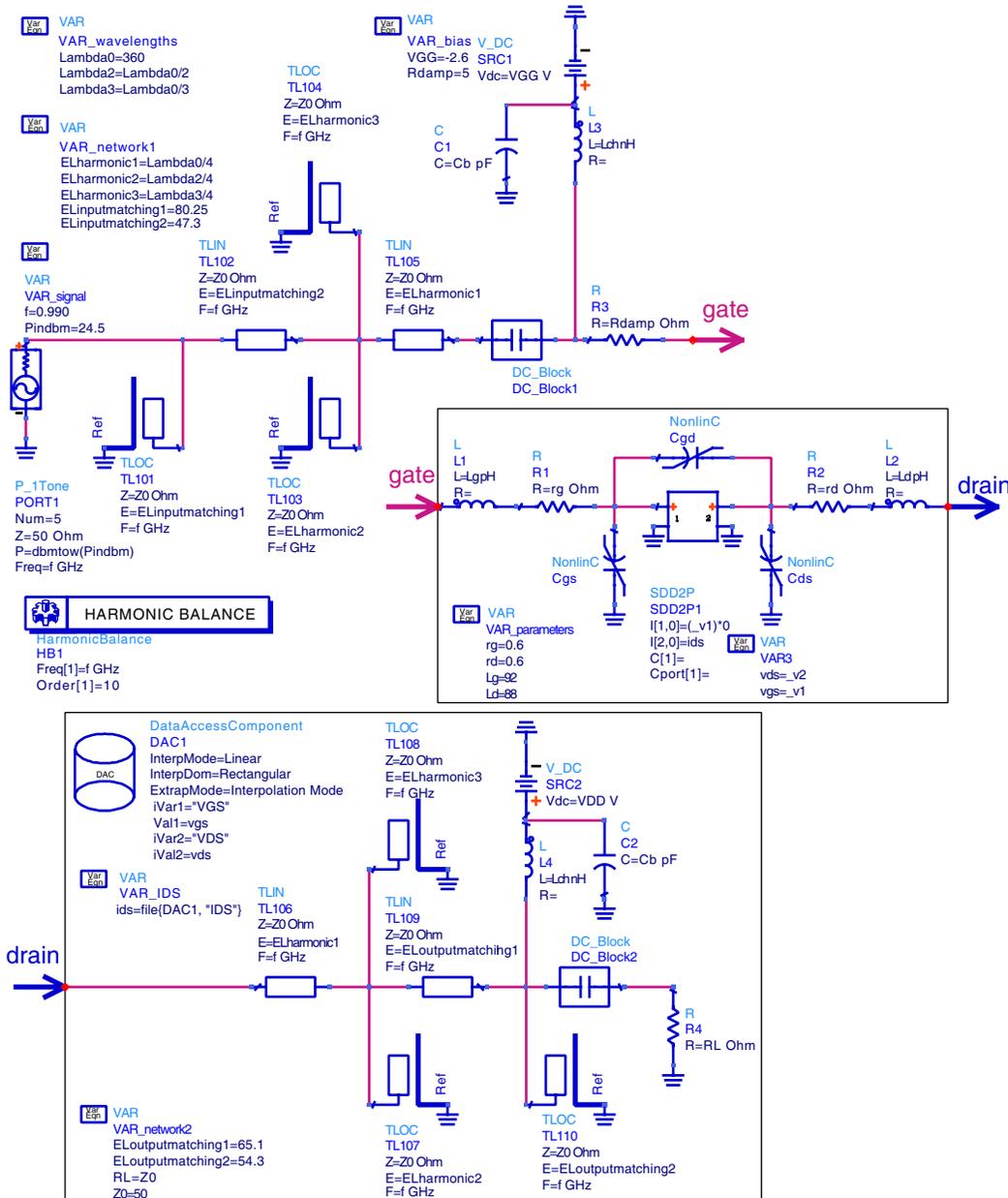


Figure 4. Schematic for the class-F PA.

simplified device model is not of primary focus here and we constrain the output network topology to be the same for all design studies of the input matching network (see Figure 3). Instead, in our work we adjust the length of the output harmonic stubs and vary C_{gd} to create different harmonic injection levels that are fed back to the gate. In this way, the significance of the input harmonic terminations versus power efficiency can be swept for different harmonic injection levels at the gate. The input matching circuit also has three transmission lines, TL103, TL104 and TL105, which are used to experiment with different input harmonic terminations at the gate.

For the first simulation experiment, the device model consists of fixed (linear) device capacitance values. The fixed capacitance values are selected to be the expected value of the nonlinear capacitances over the operating range of the circuit. The fixed capacitance values are: $C_{gs} = 6.17$ pF, $C_{ds} = 0.92$ pF and $C_{gd} = 0.36$ pF. When the device capacitances are linear, the only mechanism for generating harmonics at the gate is feedback from the output circuit to the input circuit through C_{gd} .

The effect of feedback through C_{gd} is illustrated by comparing the harmonic spectrums at the drain and gate. In Figure 5, the spectrums are shown for the case where C_{gd} is zero. The drain spectrum for the voltage has DC, fundamental and third harmonic components. The second harmonic is zero because the harmonic is shorted in the output circuit. The corresponding gate spectrum has only a DC and fundamental frequency component as expected because there is no feedback from the drain to gate. On the other hand, when C_{gd} is not zero, harmonic components from the drain voltage are fed back to the gate. An example of gate harmonics created by feedback from C_{gd} is illustrated in Figure 6 for $C_{gd} = 0.36$ pF. The amount of harmonic feedback from the output to the input of the device depends not only on the size of C_{gd} but also on the harmonic levels in the output circuit.

In the next set of simulation experiments, the device model with linear capacitances is used to compare the power efficiency of three class-F amplifier designs with different input matching circuits.

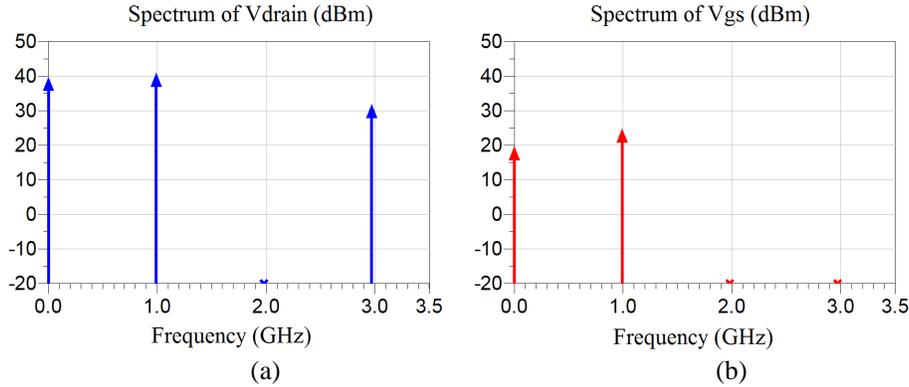


Figure 5. Spectrum for the case where $C_{gd} = 0$ pF: (a) drain voltage and (b) gate voltage.

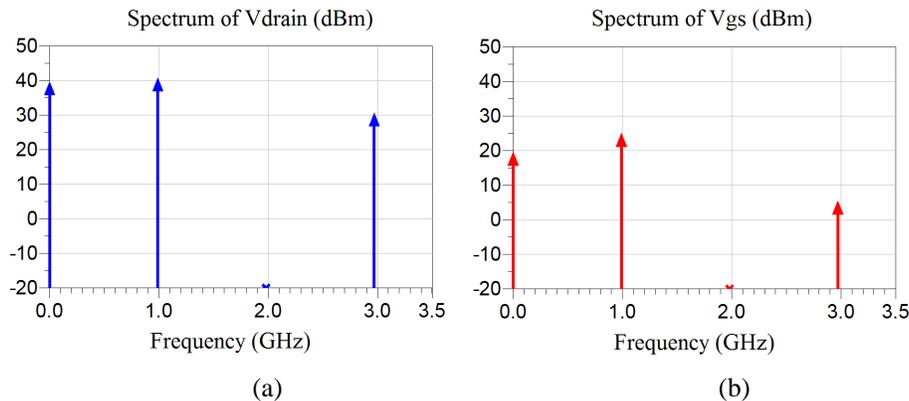


Figure 6. Spectrum for the case where $C_{gd} = 0.36$ pF: (a) drain voltage and (b) gate voltage

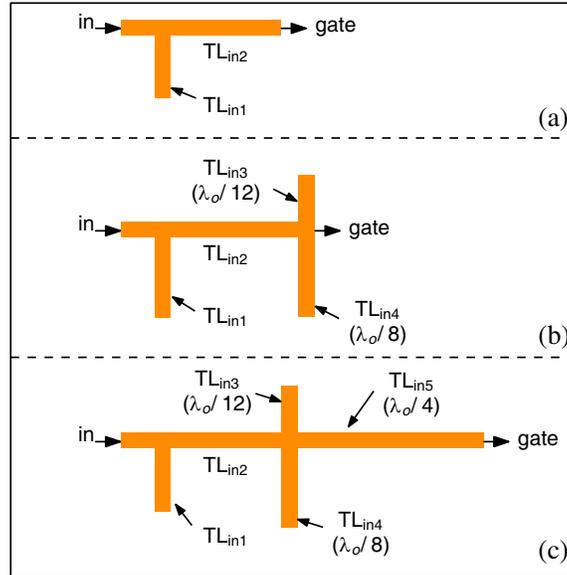


Figure 7. Input matching network circuits: (a) Design 1, (b) Design 2 and (c) Design 3.

Table 3. IMN transmission line lengths for a device model with linear capacitances.

Design	Harmonic input impedances			TL_{in1}	TL_{in2}	TL_{in3}	TL_{in4}	TL_{in5}	$\Gamma_{in,2f_o}$	$\Gamma_{in,3f_o}$
	f_o	$2f_o$	$3f_o$							
1	$Z_{S,opt}$	-	-	74.8°	30.9°	-	-	-	$1\angle 343^\circ$	$1\angle 58.5^\circ$
2	$Z_{S,opt}$	Short	Short	77.4°	26.65°	30°	45°	-	$1\angle 180^\circ$	$1\angle 180^\circ$
3	$Z_{S,opt}$	Short	Open	80.25°	47.3°	30°	45°	90°	$1\angle 180^\circ$	$1\angle 0^\circ$

The matching circuits are shown in Figure 7. In the first design (Design 1), the gate is matched at only the fundamental frequency. In the second design (Design 2), the input matching circuit provides a fundamental frequency match and a short at the second and third harmonics. Finally, in the third design (Design 3) the input matching circuit provides a match at the fundamental frequency, a short at the second harmonic and an open at the third harmonic. Table 3 summarizes the input matching network (IMN) designs.

As shown in Figure 6, odd harmonics in the drain voltage are fed back to the gate through C_{gd} . With linear device capacitances, and an ideal second harmonic short in the output, there are no even harmonics at the gate. However, when device capacitances are nonlinear or imperfect second harmonic terminations in the output circuit are considered, there are even harmonic components at the gate as well. In the next simulation experiment, the same device model with linear capacitances is used except the level of second harmonic distortion at the gate is swept over a large range by tuning the length of TL107 to create an imperfect second harmonic short in the output circuit; in other words, the second harmonic phase at the drain is swept from 150 to 180 degrees. An imperfect second harmonic short is created in practical class-F amplifier designs as soon as the frequency is shifted from the design frequency.

The results of the second harmonic sweep for the three different input matching circuit designs is summarized in Figure 8. It can be seen that the input matching circuit design is significant when the second harmonic level at the drain is high — for example greater than -20 dB relative to the fundamental frequency component. For a second harmonic level of -11 dB, going from Design 1 (fundamental match only) to Design 2 the power efficiency increases by 5.5%. A small but measurable improvement in power efficiency is obtained with Design 3 when a third harmonic open is added to the gate matching network.

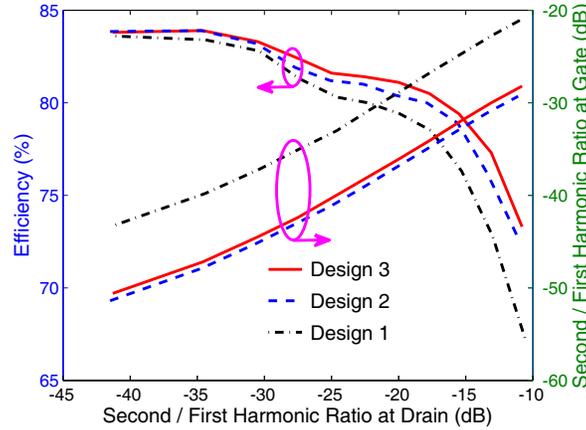


Figure 8. Simulated drain efficiency as a function of second harmonic level for a device model with linear capacitances.

If the second harmonic level is low, for example less than -30 dB, the power efficiency of the different designs are similar which is expected. From these results it is clear that incremental improvements in power efficiency can be obtained with harmonic terminations at the gate and the most significant improvement is gained by a second harmonic short with a smaller improvement gained by adding a third harmonic open. As discussed earlier, the amount of harmonic feedback from the drain to the gate depends on the size of C_{gd} . When there is no feedback, the gate signal has only a fundamental frequency component and the performance of the three designs are similar. On the other hand, as C_{gd} is increased, the significance of harmonic input impedance becomes increasingly important.

In the next set of simulations, the previous results for a device model with linear capacitances are compared with simulation results for a device model with nonlinear capacitances. With reference to Figure 1, a simplified device model is used with the nonlinear device capacitance characteristics shown in Figure 2. Similar to the previous simulations, the device model is evaluated with three different input harmonic matching circuit designs shown in Figure 7. The output matching circuit in these simulations has perfect harmonic terminations at the second and third harmonic.

A comparison of the three different designs with nonlinear device capacitances is shown in Table 4. The results are consistent with the results shown in Figure 8 for linear capacitances in that the biggest improvement in power efficiency results from adding a second harmonic short at the gate and a small improvement of less than 1% is obtained by adding a third harmonic open at the gate. Also, the improvement in power efficiency going from Design 1 to Design 2 with nonlinear device capacitances is larger than the result with linear capacitances. For example, for linear device capacitances and a second harmonic level of approximately -16.5 dB in Figure 8, the power efficiency of Design 1 is about 77.5%, similar to the power efficiency of Design 1 with nonlinear capacitances (Table 4). If Design 2 values are compared, the result for the linear capacitance model is about 79.5% or an increase of 2% compared to Design 1, while the result for the nonlinear capacitance model is 83.2%, an increase of 5.7% compared to Design 1.

Table 4. Summary of simulation results for a device model with nonlinear capacitances.

Design	Harmonic input impedances			TL_{in1}	TL_{in2}	TL_{in3}	TL_{in4}	TL_{in5}	η_d (%)
	f_o	$2f_o$	$3f_o$						
1	$Z_{S,opt}$	-	-	79.1°	31.9°	-	-	-	77.5
2	$Z_{S,opt}$	Short	Short	80.0°	21.9°	30°	45°	-	83.2
3	$Z_{S,opt}$	Short	Open	81.9°	47.4°	30°	45°	90°	83.7

The device level modeling work also shows that the performance of an amplifier with linear device capacitances has a power efficiency within a few percent of an amplifier with nonlinear device capacitances. In other words, the harmonic injection by C_{gd} is very significant. Also, the simulation experiments show that a second harmonic short at the input is very significant in terms of improving power efficiency in a class-F amplifier. The second harmonic short at the gate node desensitizes the design to second harmonic injection from both feedback through C_{gd} as well as second harmonic components created by nonlinear device capacitances. A small but slightly higher power efficiency can be obtained with an additional input third harmonic termination.

3. IMPLEMENTATION AND DESIGN METHODOLOGY

In this section, the design of a class-F PA with multiharmonic input and output matching networks using a Cree 10 W GaN HEMT device is described. The simplified device model for the packaged die is extended to include the parasitic capacitance of the package. The package parasitics modify the harmonic impedances required at the terminals of the device and the appropriate matching circuits must be synthesized. The design methodology for implementing the harmonic matching networks is described next.

3.1. Packaged Device Model and Load/Source Pull Set-up

The device model for the packaged die is shown in Figure 9. It consists of a bare die model as shown earlier in Figure 1 with additional lead inductances (L_{pg} , L_{pd}) and capacitances (C_{pg} , C_{pd}). These parasitic components can be extracted based on the procedure presented in [22, 23]. The extracted values for the package model are $L_{pg} = 0.7$ nH, $L_{pd} = 0.6$ nH, $C_{pg} = 0.41$ pF and $C_{pd} = 0.4$ pF. Due to these parasitic components, the optimum impedances at the drain and gate terminal planes of the package should create a corresponding short at $2f_0$ and an open at $3f_0$ at the intrinsic ports of the device. The required impedances at the terminal planes of the device were determined from a load pull test bench in the simulator using the packaged device model. The results are shown in Table 5 for a fundamental frequency of 990 MHz with a bias of $V_{DD} = 30$ V and $V_{GG} = -2.6$ V.

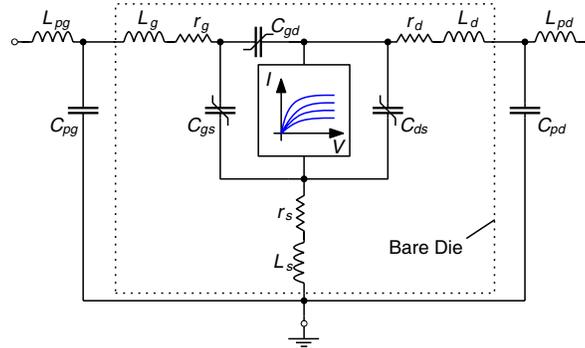


Figure 9. Device model for packaged die.

Table 5. Source and load pull harmonic impedances for the class-F amplifier.

P_{in} (dBm)	P_{out} (dBm)	$PAE(\%)$	$\Gamma_L(f_0)$	$\Gamma_L(2f_0)$	$\Gamma_L(3f_0)$	$\Gamma_S(f_0)$	$\Gamma_S(2f_0)$	$\Gamma_S(3f_0)$
24.5	40.5	81.6	$0.34\angle 142.67$	$1.0\angle 166$	$1.0\angle 329.38$	$0.44\angle 146.11$	$1.0\angle 170.2$	$1.0\angle 33.91$

3.2. Input and Output Matching Network Design

The circuit topologies for the matching networks in the class-F design are shown in Figure 10 and the matching networks can be designed using the impedance buffer methodology described in [24]. With

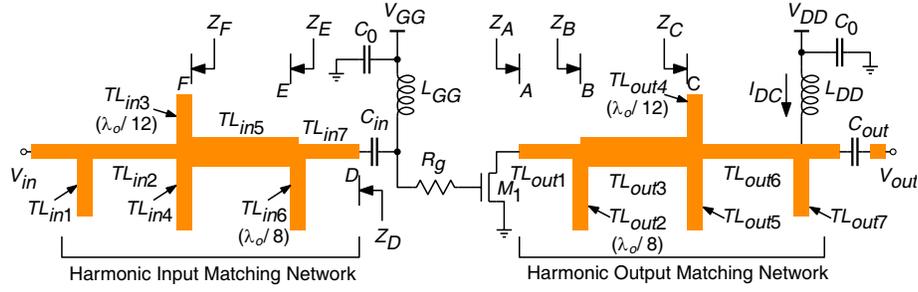


Figure 10. Schematic of the class-F PA with output and input matching circuits and bias networks.

reference to Figure 10, the output matching network at reference plane A should provide optimum load impedances of $Z_L(f_0)$ at f_0 , $Z_L(2f_0)$ at $2f_0$ and $Z_L(3f_0)$ at $3f_0$. The corresponding load reflection coefficients at these frequencies are given in Table 5. In the design, all transmission lines have a characteristic impedance of 50Ω except for TL_{in5} and TL_{out3} which have a characteristic impedance of 36Ω .

The synthesis of the output match begins with the second harmonic network. The transmission line TL_{out2} is 90° at the second harmonic frequency and creates a short at plane B. Consequently the reflection coefficient looking to the right of plane B at the second harmonic is $1 \angle 180^\circ$. The addition of the series transmission line TL_{out1} modifies the phase to provide the match $\Gamma_L(2f_0)$ at plane A. The next step in the synthesis of the output circuit is to add transmission lines TL_{out3} and TL_{out4} to create the third harmonic match. Transmission line TL_{out4} is 90° at the third harmonic frequency which creates a short at reference plane C. The short is transformed through transmission line TL_{out3} that ideally maps to an open circuit at the device, but in practice is modified to compensate for the impedance contributions of the second harmonic network and create the required reflection coefficient $\Gamma_L(3f_0)$ at plane A. Also, the characteristic impedance of TL_{out3} is 36Ω and selected to improve the bandwidth of the fundamental frequency match by transforming the lower output impedance at the device terminal plane to a higher impedance close to 50Ω . The fundamental frequency output match is implemented with a double stub circuit consisting of TL_{out5} , TL_{out6} , and TL_{out7} . For this design the double stub circuit results in a more compact fundamental frequency match than a single stub matching circuit.

A similar design methodology is used for the input matching circuit design with the exception of a series resistor R_g added to improve the stability of the device. Rollet's stability factor is given by [25]

$$k = \frac{2 \operatorname{Re}(Z_{11}) \operatorname{Re}(Z_{22}) - \operatorname{Re}(Z_{12} Z_{21})}{|Z_{12} Z_{21}|} \quad (2)$$

and a series gate resistor increases the real part of Z_{11} to improve stability. Since R_g also reduces gain, the choice of R_g is a compromise between stability and gain. In this design, a value of 2Ω is selected.

3.3. Implementation and Optimization

Based on the proposed topology shown in Figure 10, a class-F amplifier was implemented using a 10 W packaged GaN HEMT from Cree (CGH40010). The design was fabricated using copper tape transmission lines on a 1.524 mm Rogers 4350 substrate with dielectric constant of 3.70. Using the method described in the previous subsection, the initial values of the transmission lines in the matching networks were determined. The transmission line lengths were then optimized in the simulator using the large signal device model from Cree. The final design values for the matching networks are summarized in Table 6.

The simulated drain and gate waveforms for the final class-F amplifier design are shown in Figure 11. For these simulations, the current and voltage are shown referenced to the terminal planes of the packaged device. The shape of the waveforms are modified relative to the waveforms at the intrinsic device plane of the device because of the package parasitics. Other simulations results are shown in the next section where they are compared with experimental results.

Table 6. Transmission line lengths for load and source matching networks.

	TL_{out1}	TL_{out2}	TL_{out3}	TL_{out4}	TL_{out5}	TL_{out6}	TL_{out7}
in mm	2	22.7	48.9	15.2	21.9	28.8	30.6
in degree	4.1°	46.2°	102.4°	31°	44.6°	58.6°	62.2°
	TL_{in1}	TL_{in2}	TL_{in3}	TL_{in4}	TL_{in5}	TL_{in6}	TL_{in7}
in mm	29.6	27.5	27	15.7	43.7	21.3	1.3
in degree	60.2°	56.1°	54.9°	32°	92.3°	43.3°	2.7°

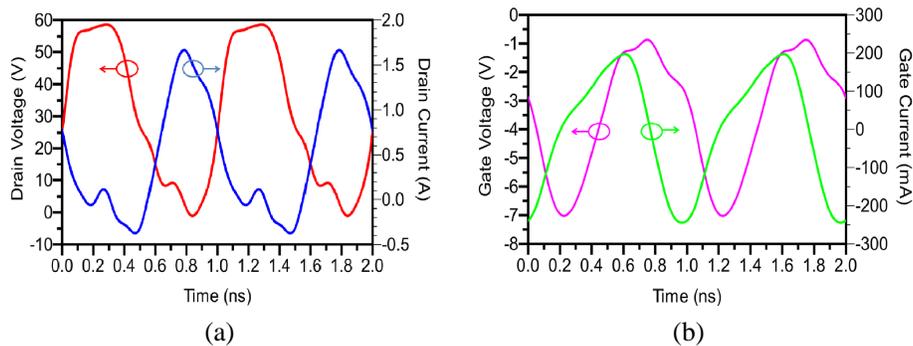


Figure 11. Simulated (a) drain voltage and drain current waveforms and (b) gate voltage and drain current waveforms.

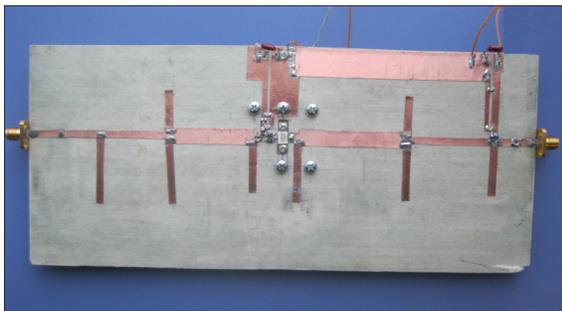


Figure 12. Photograph of the class-F power amplifier.

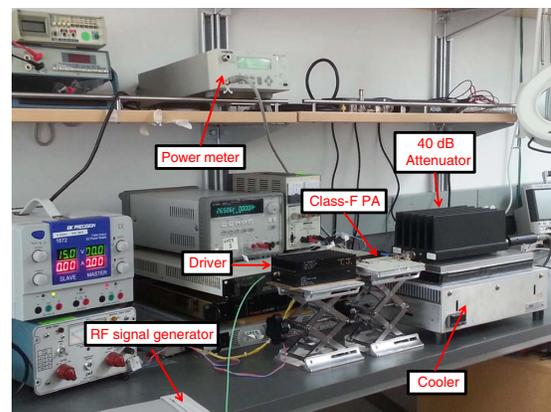


Figure 13. The class-F PA test bench.

4. EXPERIMENTAL RESULTS

The experimental class-F amplifier design is shown in Figure 12 and a picture of the experimental test bed is shown in Figure 13. The amplifier design was tested with both continuous wave (CW) and modulated signals. The results for each test signal are described in the following subsections.

4.1. CW Performance

The power efficiency of the class-F amplifier for a CW input signal is shown in Figure 14. The measured power efficiency reaches a maximum value of 78.8% at an output power of 40.5 dBm. At maximum

efficiency, the quiescent drain current is 19% of the maximum DC current. The figure also includes simulation results for the same test conditions. Although good agreement between simulation and measurement results are obtained, the discrepancy at high power may be related to the self-heating in the device. At low output power, the differences between simulated and measured performance may be related to the switch mode operation of the model [26–28].

The power efficiency and output power as function of frequency are shown in Figure 15. Power efficiency is greater than 60% over a frequency range of approximately 120 MHz. The bandwidth is primarily limited by the impedance variation of the input harmonic stubs near the fundamental frequency. Although a double stub input match is added to compensate for the harmonic stub impedances at the fundamental frequency, the network is inherently narrowband. This illustrates the trade-off between bandwidth and power efficiency which can result by shaping the gate waveform with harmonic terminations at the input.

4.2. Modulated Performance

After characterizing the amplifier with CW test signals, the amplifier was tested with a 5 MHz WCDMA test signal. The WCDMA signal had a 8.8 dB peak-to-average (PAR) power ratio and was generated using a Tektronix AWG70002A arbitrary waveform generator. Performance of the amplifier was

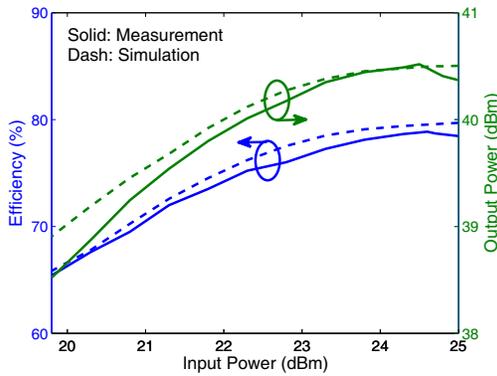


Figure 14. Measured and simulated drain efficiency and output power as a function of input power for a CW test signal.

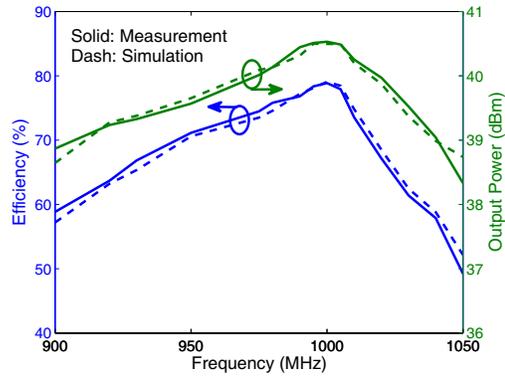


Figure 15. Measured and simulated drain efficiency and output power as a function of frequency for a CW test signal.

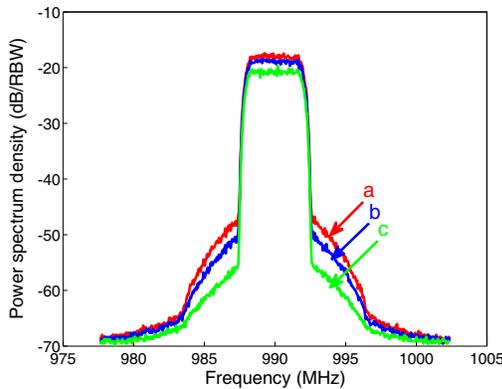


Figure 16. Measured output spectrums for a WCDMA signal at three different output power levels: (a) 35.1 dBm, (b) 33.4 dBm, and (c) 31.6 dBm.

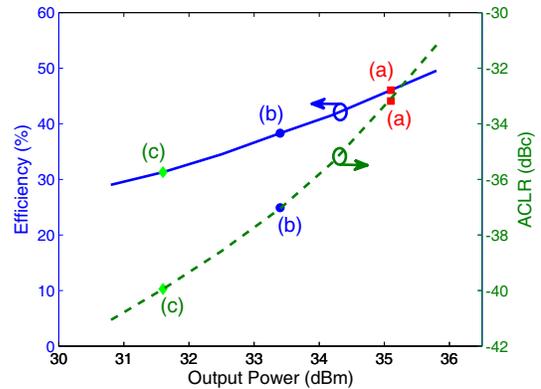


Figure 17. Measured drain efficiency and ACLR as a function of output power for a WCDMA signal.

measured without linearization. The measured output spectrums for the WCDMA signals are shown in Figure 16 with a resolution bandwidth (RBW) of 30 KHz. A summary of the adjacent channel leakage ratio (ACLR) and power efficiency as function of output power is shown in Figure 17.

In the figures, three different output power levels are identified for comparison. At point (a), the average output power is 35.1 dBm. The CW saturated output power is approximately 40.5 dBm (see Figure 14); therefore the peak power of the modulated signal at point (a) is compressed by about 3.4 dB. The corresponding ACLR is -33.1 dBc and the power efficiency is 46.1%. With the addition of digital predistortion, improvements in linearity of 15 dB or more could be expected [29, 30]. The other two points, (b) and (c), are measured under back-off conditions and as expected linearity improves at the expense of power efficiency.

5. CONCLUSION

In this work, the effect of second and third harmonic impedances in a class-F amplifier were systematically studied using a simplified device model. Different input matching networks were compared to shape the gate waveform and evaluate power efficiency. The device model was modified to change the device capacitance characteristics and evaluate the sensitivity to nonlinear capacitance. The model also shows how harmonic injection through C_{gd} is clearly evident and how imperfect output termination impedances can affect the input. The results show that a second harmonic short at the gate in a class-F amplifier is very beneficial to enhance power efficiency and the incremental improvement in power efficiency by terminating the third harmonic is less significant. The second harmonic short is also very effective in desensitizing the design to nonlinear device capacitances.

The design concepts were verified by building a class-F amplifier with fundamental, second, and third harmonic input and output matching networks. Good performance was obtained and the experimental results were compared with simulation results. Future work is planned to evaluate the relationship between the device model characteristics and the incremental power efficiency gains of input harmonic matching in an inverse class-F amplifier.

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