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Design of Asymmetrical Doherty Power Amplifier with Reduced Memory Effects and Enhanced Back-off Efficiency

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Abstract—This paper presents the design of an asymmetrical Doherty power amplifier (DPA) with improved linearity and efficiency performance. Resonator-type drain bias networks, providing high impedances at the carrier frequency and low impedances with small variation at the envelope frequency, are introduced to reduce the DPA's memory effects when transmitting wideband signals. The general criteria for DPA design are summarized, and the approach to obtain optimum fundamental and harmonic impedances is proposed to achieve back-off efficiency enhancement. For experimental validation, the asymmetrical DPA is designed and implemented using two identical GaN HEMTs. Measured with continuous wave (CW), the proposed DPA delivers a saturation power greater than 49.3 dBm from 3400 to 3600 MHz, along with high drain efficiency of over 62% and 48% at peak and 8-dB back-off power, respectively. Driven with 100-MHz LTE-advanced signals, the adjacent channel leakage ratio (ACLR) asymmetry of the DPA at 20-MHz offset is lower than 1-dB. After digital predistortion (DPD) linearization, the proposed DPA achieves an ACLR of better than −48 dBc at an average output power about 41 dBm and the drain efficiency over 45% across the frequency band.

1. INTRODUCTION

The ever-increasing demand for higher data rate and larger network capacity has driven the utilization of more complex modulation schemes in modern wireless communication systems, resulting in the signals characterized with high peak-to-average power ratio (PAPR) and wider occupied bandwidth. In order to satisfy the stringent linearity requirements imposed by the wireless communication standards, the power amplifier (PA) in transmitter usually has to operate at back-off power with low efficiency, which will cause thermal problems, waste of energy and/or shorter battery life. The Doherty power amplifier (DPA), with simple circuit configuration, high back-off efficiency and proven linearizability, has regained researchers' attention and has been extensively investigated and widely deployed in the base stations of the third generation wireless communications systems.

Research efforts on DPA have been mainly made to enhance the efficiency, improve the linearity and extend the bandwidth of the DPA. To overcome the efficiency degradation due to incomplete load modulation, solutions such as uneven power drive [1], gate bias adoption [2], asymmetrical structure [3] and modified load modulation network [4] were proposed. In addition, harmonic tuning [5], knee voltage effect mitigation [6] and digital DPA [7] were devised to further enhance the back-off efficiency. With respect to the linearity improvement of the DPA, digital pre-distortion (DPD) is the most prevalent technique, while approaches at the circuit level are seldom reported, except the fine tuning of the carrier and peaking amplifier's bias voltages for distortion cancellation [8]. To fulfill the multi-band/multi-standards requirement of the base stations and to cope with the fact that signals occupied much wider instantaneous bandwidth (e.g., up to 100-MHz aggregated bandwidth for LTE-advanced

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systems), bandwidth extension of the DPA is in urgent need and has recently became a research hotspot. Bandwidth limiting factor such as the load modulation network, output matching network and phase alignment of the cell amplifiers' current were well analyzed and schemes including modified output combining network with reduced impedance transformation ratio [9], broadband DPA via real frequency technique [10], transformer-less load modulated (TLLM) architecture [11], wideband output compensation stages [12] and coupled-line couplers [13] were proposed.

The majority of research efforts on DPA focused on only one aspect of the three competing specifications mentioned above. This is because, on one hand, the DPD technique makes it possible for linearity to make room for efficiency and/or bandwidth [14]; on the other hand, traditional efficiency enhancement approaches for DPA, such as preserving ideal load modulation and harmonic tuning, are difficult to realize over the entire frequency band when the aim is to enlarge the bandwidth. However, as the signal bandwidth increases, the impact of the electrical memory effect on the DPA's linearity could no longer be ignored because the bandwidth dependent distortion level and distortion asymmetry will limit the linearity improvement benefitting from the linearization techniques [15]. Under such circumstance, linearity performance should be taken into consideration as well as the efficiency in the design of Doherty power amplifier.

Therefore, this paper presents the design of an asymmetrical DPA with improved performance in terms of linearity and back-off efficiency for 100-MHz LTE-advanced applications. With the introduction of resonator-type drain bias networks, which can provide low baseband impedance with small variation, the electrical memory effects are reduced. In order to achieve high back-off efficiency, asymmetrical structure is employed, approach to obtain the optimum fundamental and harmonic impedances is proposed and the harmonic components are tuned by the output matching network together with the bias network. The proposed asymmetrical DPA shows a saturation power of over 49.3 dBm and achieves a high drain efficiency of over 62% and 48% at peak and 8-dB back-off power, respectively. When tested with 100-MHz LTE-advanced signals, the proposed DPA exhibits an adjacent channel leakage ratio (ACLR) asymmetry of lower than 1-dB. With DPD technique, an average drain efficiency of higher than 45% and a linearized ACLR of better than −48 dBc were attained at about 41 dBm average output power from 3400 to 3600 MHz.

2. MEMORY EFFECTS AND RESONATOR-TYPE DRAIN BIAS NETWORKS

Memory effects generally refer to variation of distortion characteristic over the modulating signal bandwidth in the power amplifier, which mainly result from the impedances presented to the active device, temperature variation and the charge trapping [16]. Although the distortion itself is not a memory effect, the distortion in power amplifier is adversely influenced by the memory effects in the form of bandwidth dependent distortion level and distortion asymmetry, especially when the signals has wide bandwidth [15]. This in turn limits the achievable distortion compensation of the linearization techniques, as analyzed in [17] and demonstrated by the experimental results in [18]. Among the mechanisms leading to the memory effects, the impedance, mostly at the baseband frequency, seems to be the only factor that can be coped with at the circuit level and is controlled mainly through the bias networks.

To reduce the memory effects, the baseband impedances are required to be short circuit or at least maintained at a low level with constant value to minimize the envelope frequency voltage components [17]. Therefore, an optimized bias circuit with an envelope frequency decoupling capacitor located within the quarter-wave transmission line was proposed in [8], and the ACLR asymmetry was reduced to less than 2 dB over a broad power range. In [15], the LC series resonant circuits were directly connected to the gate and drain electrodes of the transistor die and the flat IMD3 characteristic was achieved with the two-tone carrier spacing exceeding 50-MHz. Unfortunately, the RF impedances were drastically reduced by those circuits, resulting in difficulties in the design of matching networks.

In this paper, a parallel LC resonant circuit, simultaneously providing low baseband impedances and high RF impedances, is proposed and utilized in the drain bias networks of the DPA for memory effects reduction. As illustrated in Fig. 1, the proposed bias network is composed of a 0.8 pF capacitor 600S0R8BT250, two parallel inductors 0603HP-3N3 (for higher current carrying capacity and lower equivalent series resistances) and a series of decoupling capacitors. Simulated with the s2p files of the

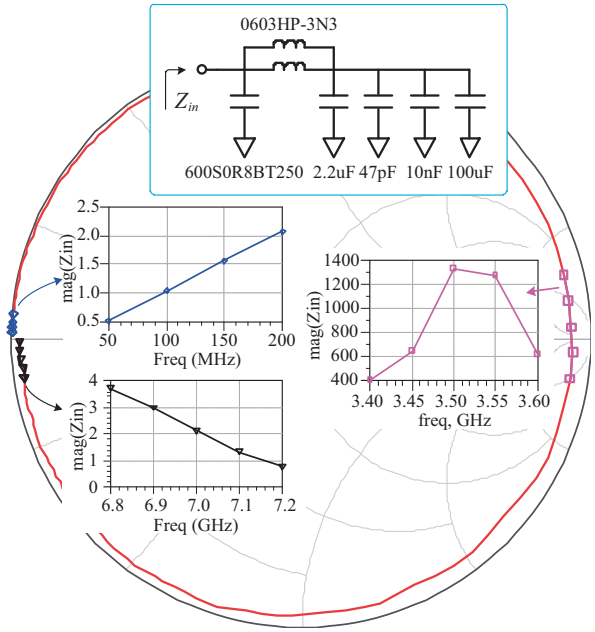


Figure 1. Schematic and simulation results of the resonate-type bias network.

capacitors and inductors, the baseband impedances from 50 MHz to 200 MHz are lower than 2.2 Ω with small variation. A RF impedances of higher than 400 Ω from 3400 MHz to 3600 MHz are sufficient to prevent RF power leakage into the bias circuit and their impact on the output matching networks can be neglected. While the second harmonic impedances of the resonator-type drain bias networks, near short circuit, should be taken into consideration if the harmonic tuning is employed for efficiency enhancement.

3. BACK-OFF EFFICIENCY IMPROVEMENT

In this section, the criteria that should be met in the DPA design are summarized, followed by the analysis of the relation between the carrier transistor's load impedances at the peak and back-off power, then the approach to determine the optimum fundamental and harmonic impedances of the asymmetrical DPA for back-off efficiency improvement is presented.

3.1. General Design Criteria of the DPA

It is generally recognized that the DPA should achieve the highest possible efficiency at back-off power and deliver maximum possible output power at peak power [8]. This is because the probability density function (PDF) of the modulated signal is mainly concentrated in the back-off region, and consequently the DPA's average efficiency is mainly determined by its back-off efficiency [11]. On the other hand, the peak of the modulated signal, although rarely appears, must be linearly amplified to maintain an acceptable linearity performance. To achieve these two goals, the following criteria are to be satisfied in the design of the DPA:

(1) At the peak power, the carrier and peaking transistors should be presented with load impedances $Z_{opt,C,H}$ and $Z_{opt,P,H}$ that will enable the carrier and peaking amplifiers to yield a maximum output power of $P_{\max,C}$ and $P_{\max,P}$, respectively, as shown in Fig. 2. And the ratio between $P_{\max,C}$ and $P_{\max,P}$ is expected to be equal to δ to achieve the complete load modulation, where δ is the predetermined peaking to carrier amplifier power ratio and is related to the output power back-off range (OBO) [19], as shown in Eq. (1).

$$\delta = \frac{P_{\max,P}}{P_{\max,C}} = 10^{\frac{\text{OBO}}{20}} - 1. \tag{1}$$

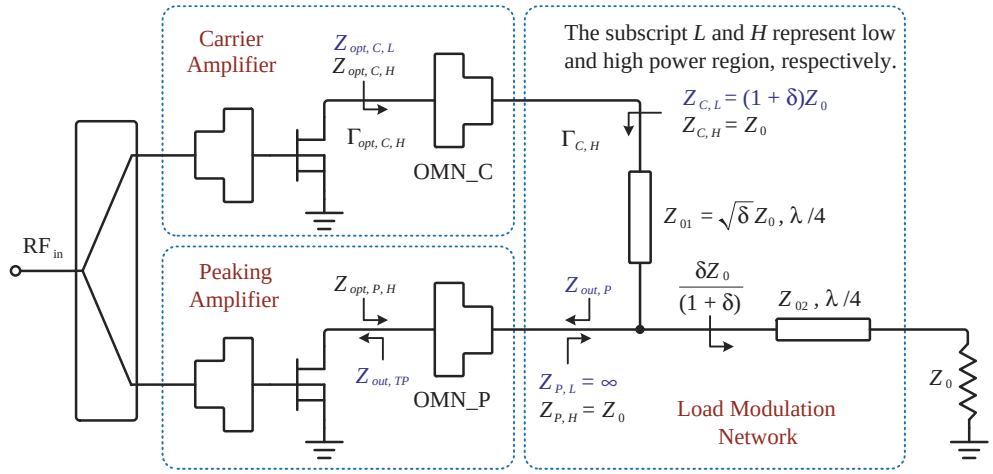


Figure 2. Schematic diagram of the asymmetrical Doherty power amplifier.

(2) The carrier transistor should be matched with load impedance $Z_{opt,C,L}$ which exhibits the highest possible efficiency with the saturation power of $P_{C,\mathrm{OBO}} = P_{\max}/(1+\delta)^2$ before the peaking amplifier tuning on, where $P_{\max}$ represents the maximum output power of the DPA [20].

(3) The peaking amplifier's off-state output impedance is supposed to be large enough to prevent the RF power leakage. And the peaking amplifier should start to conduct when the carrier amplifier delivers a output power of $P_{C,\mathrm{OBO}}$.

3.2. Constant Voltage Standing Wave Ratio (VSWR) Circle

Therefore, the carrier transistor is required to be matched to $Z_{opt,C,L}$ and $Z_{opt,C,H}$ at back-off and peak power, respectively. Another criterion, related to $Z_{opt,C,L}$ and $Z_{opt,C,H}$, can be derived providing that the carrier amplifier's output matching network (OMN_C) is lossless and reciprocal. Assuming that OMN_C has been designed to transform $Z_{C,L}$ to $Z_{opt,C,L}$, the S-parameters of OMN_C can be expressed as follows selecting $Z_{C,L}$ as the reference impedance [11]

$$\mathbf{S} = \begin{bmatrix} S_{11} & \sqrt{1-|S_{11}|^2}e^{j\theta_{21}} \\ \sqrt{1-|S_{11}|^2}e^{j\theta_{21}} & -S_{11}^{*}e^{j2\theta_{21}} \end{bmatrix}. \tag{2}$$

Terminating OMN_C with $Z_{C,H}$, the reflection coefficients at the input and output ports of OMN_C can be written as

$$\Gamma_{opt,C,H} = S_{11} + \frac{S_{12}S_{21}\Gamma_{C,H}}{1-S_{22}\Gamma_{C,H}}. \tag{3}$$

Now selecting $Z^{*}_{opt,C,L}$ and $Z_{C,L}$ as the reference impedances of OMN_C's input and output ports, respectively, it can be derived that $S_{11} = 0$ by the definition of the generalized scatting parameters [21]. Extended to generalized reflection coefficient, Eq. (3) can be rewritten as

$$\Gamma_{opt,C,H} = \Gamma_{C,H}e^{j2\theta_{21}}. \tag{4}$$

where $\Gamma_{opt,C,H}$ and $\Gamma_{C,H}$ in Eq. (4) are calculated as follows

$$\Gamma_{opt,C,H} = \frac{Z_{opt,C,H} - Z_{opt,C,L}}{Z_{opt,C,H} + Z^{*}_{opt,C,L}}, \tag{5}$$

$$\Gamma_{C,H} = \frac{Z_{C,H} - Z_{C,L}}{Z_{C,H} + Z_{C,L}}. \tag{6}$$

Substituting the values of $Z_{C,H}$ and $Z_{C,L}$ shown in Fig. 2 into Eq. (6), $\Gamma_{C,H}$ can be obtained and Eq. (4) can be rewritten as

$$\begin{aligned} \Gamma_{opt,C,H} &= \frac{-\delta}{2+\delta} e^{j2\theta_{21}}, \\ \mathrm{VSWR}_{opt,C,H} &= 1+\delta. \end{aligned} \tag{7}$$

It can be seen from Eq. (7) that if OMN_C is designed to convert $Z_{C,L}$ to $Z_{opt,C,L}$ for high back-off efficiency, $Z_{opt,C,H}$ will locate on a constant VSWR circle centring at $Z_{opt,C,L}$ with a radius of $1+\delta$, the precise location of which is fully determined by the OMN_C's phase θ_{21}. This is an extra constraint imposed on $Z_{opt,C,H}$ in addition to generating an output power of $P_{\max,C}$, both of which should be met in the selection of $Z_{opt,C,H}$. All the design constraints, related to the carrier and peaking transistors' load impedances and peaking amplifier's off-state output impedance, are summarized in Table 1.

Table 1. Design constraints of the Doherty power amplifier.

Impedances	Constraints	
$Z_{opt,\,C,\,L}$	deliver output power of $P_{C,\,\mathrm{OBO}}$ with highest possible efficiency when the peaking amplifier turning on	$\mathrm{VSWR}_{opt,\,C,\,H} = 1+\delta$
$Z_{opt,\,C,\,H}$	deliver output power of $P_{\max,\,C}$ at the peak output power	
$Z_{opt,\,P,\,H}$	deliver output power of $P_{\max,\,P}$ at the peak output power	$P_{\max,\,P}/P_{\max,\,C} = \delta$
$Z_{out,\,P}$	be as high as possible to minimize the RF power leakage	

3.3. Optimum Fundamental and Harmonic Impedances Selection

The asymmetrical DPA (ADPA) implemented with same size devices often suffers from the efficiency degradation, which results from the larger load impedance presented to the carrier amplifier for wide back-off range and the on-resistance of the transistor [22]. An alternative approach to achieve wide back-off range for ADPA is reducing the drain voltage of the carrier cell, in which, unfortunately, two or more supply voltages are required. In this paper, the harmonic tuning technique [5] is adopted to mitigate the efficiency decrease of the ADPA. Following the design criteria outlined in Table 1, the optimum fundamental and harmonic impedances of the carrier and peaking transistors are obtained as follows.

(1) Bias the peaking transistor at class C mode, the break point of the DPA ($P_{\mathrm{in,\,break}}$) can be obtained through calculation or simulation. Simulating with the large signal nonlinear model, select the impedance that yields maximum possible output power $P_{\max,P}$ as $Z_{opt,P,H}$ and record the corresponding input power $P_{\mathrm{in,max}}$.

(2) With the knowledge of $P_{\max,P}$ and the expected back-off range, which is mainly determined according to the PAPR of the signal, the carrier amplifier's output power at the break point and peak power ($P_{C,\mathrm{OBO}}$ and $P_{\max,C}$) can be calculated.

(3) Driving the deep class AB biased carrier transistor with power of $P_{\mathrm{in,\,break}}$, perform the harmonic load pull simulation to obtain $Z_{opt,C,L}$ and the corresponding harmonic load impedances under which the carrier transistor achieves output power of $P_{C,\mathrm{OBO}}$ with highest possible efficiency. If the carrier transistor is unable to deliver power of $P_{C,\mathrm{OBO}}$ due to the low level of $P_{\mathrm{in,\,break}}$, the gate bias voltage of the peaking transistor should be reduced to avoid the early turning on of the peaking amplifier, then repeat step (1) and (2).

(4) Increase the drive power of the carrier transistor to $P_{\mathrm{in,max}}$ and plot the power contours of the carrier transistor using the loadpull data, as shown in Fig. 3. The constant VSWR circle, centring at $Z_{opt,C,L}$ with radius of $1+\delta$, will usually intersect the power contour of $P_{\max,C}$ at two points,

which are the candidates for $Z_{opt,C,H}$. The final choice should be made taking into consideration of the bandwidth and design complexity of the output matching network.

Only the carrier transistor's harmonic impedance at back-off power is obtained in the above mentioned procedure since the back-off efficiency of the DPA is mostly dependent on the carrier amplifier [11]. In addition, considering that the resonator-type drain bias network shown in Fig. 1 presents near-short impedances at the second harmonic frequency, a region instead of a point for the second harmonic impedance of the carrier transistor, as illustrated in Fig. 3, is selected to facilitate the design of output matching network.

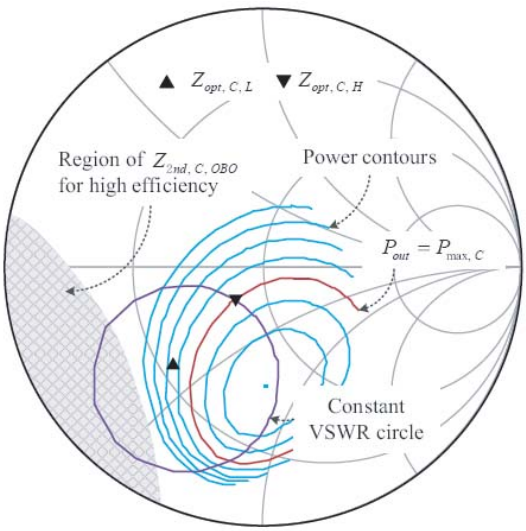


Figure 3. Selection of the carrier transistor's optimum fundamental and harmonic impedances. The driver power of the carrier transistor is $P_{\text{in,break}}$ and $P_{\text{in,max}}$, respectively, to obtain $Z_{opt,C,L}$ and $Z_{opt,C,H}$.

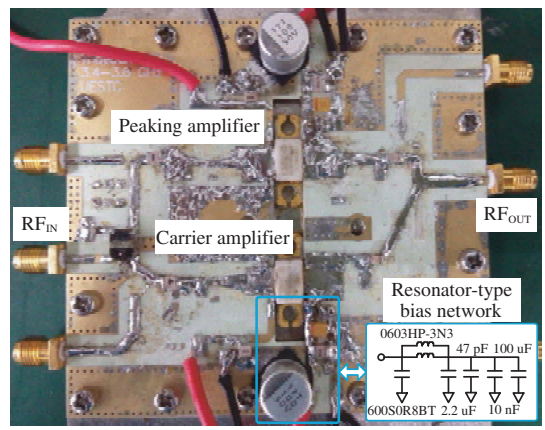


Figure 4. A photograph of the fabricated asymmetrical DPA.

4. IMPLEMENTATION AND EXPERIMENTAL RESULTS

4.1. Implementation of the Asymmetrical DPA

To experimentally verify the effectiveness of the proposed bias network and method to selecting the optimum load impedances in linearity and back-off efficiency improvement, an asymmetrical DPA with 8-dB back-off range is designed and implemented using two 60 W Cree CGH35060F GaN HEMTs. The substrate Rogers 4350B has a thickness of 30 mil and dielectric constant of 3.48 at the frequency band of 3400–3600 MHz. The carrier amplifier was biased at class AB mode with 0.26-A quiescent current, which is the same condition as in the procedure for optimum load impedances selection, while the gate bias voltage of the peaking amplifier was fine tuned to improve the linearity of the DPA. A photograph of the fabricated ADPA is shown in Fig. 4, the printed circuit board (PCB) and the power transistors of which were directly soldered on the heat sink for better thermal conductivity and reduction of thermal memory effects.

4.2. Experimental Results

Measured with continuous wave (CW), the gain and drain efficiency characteristics of the proposed ADPA versus output power are depicted in Fig. 5. Driven by the driver amplifier block with 40 dB gain and about 41.8 dBm 1 dB compression power, the ADPA delivers a saturation power of about 49.2 dBm from 3400 to 3600 MHz and has about 11 dB gain at 41 dBm output power with the gain flatness less

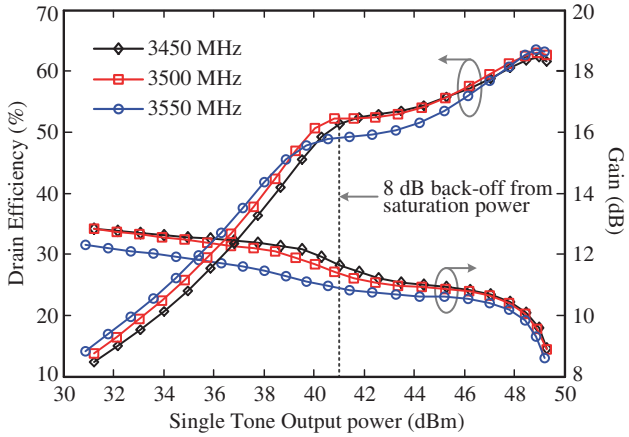


Figure 5. A photograph of the fabricated asymmetrical DPA.

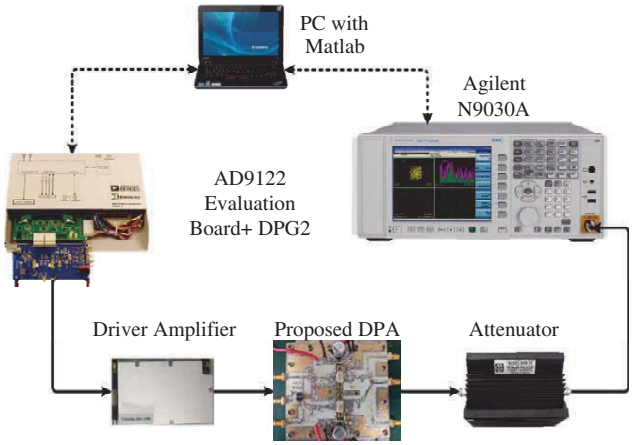
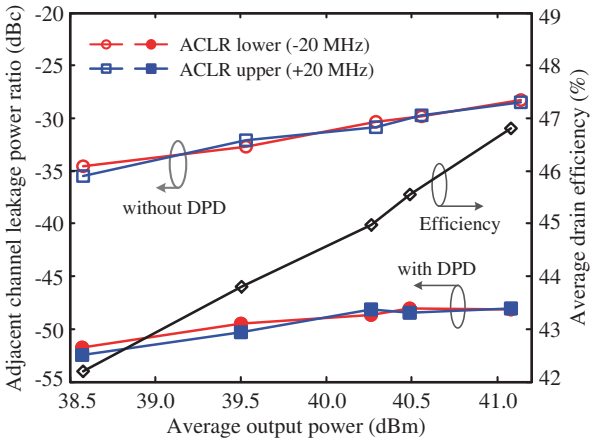
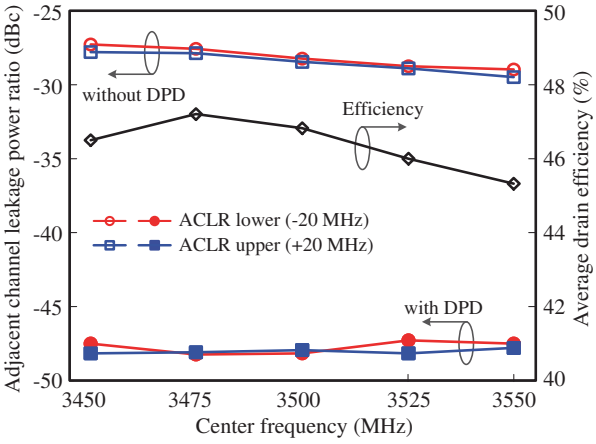


Figure 6. Schematic of the linearization experimental test bench.



(a)



(b)

Figure 7. Measured performance of the proposed ADPA excited with 100-MHz LTE-advanced signals. (a) The measured ACLR and drain efficiency versus output power at 3500 MHz. (b) The ACLR and drain efficiency performance versus operating frequency at about 41 dBm average output power.

than ±0.5 dB. A high drain efficiency of over 62% and 48% is achieved at peak and 8-dB back-off power, respectively.

To evaluate the performance of the proposed DPA excited by signals with wide instantaneous bandwidth, a contiguous five-carrier LTE-advanced signal with 100-MHz bandwidth and PAPR of about 8-dB was used to access the efficiency and linearity performances. The 64-QAM modulated LTE-advanced signal is generated in MATLAB, and the PAPR of the signal is reduced before be downloaded into the AD9122 evaluation board, as shown in Fig. 6. After digital to analog conversion and up-conversion, the I/Q baseband signal was transformed to RF signal and fed to the driver amplifier and the proposed ADPA. With the Agilent signal analyzer N9030A, the attenuated signal was down-converted, demodulated and uploaded to the computer to obtain the inverse model of the ADPA for linearization. The pre-distorted signal can be generated with the inverse PA model and then downloaded into the AD9122 evaluation board again as the input signal to correct the nonlinearity of the ADPA.

The measured performances of the asymmetrical DPA when driven with 100-MHz LTE-advanced signals are depicted in Fig. 7. The adjacent channel power leakage ratio (ACLR) at ±20 MHz offset is lower than −27 dBc at an average output power about 41 dBm. And the ACLR asymmetry of lower

Table 2. Performance comparison with 3500 MHz DPA.

Ref.	Freq. (GHz)	Gain (dB)	$P_{1\,\mathrm{dB}}$ (dBm)	P_{sat} (dBm)	Eff.@ 8 dB back-off	Signal BW (MHz)	P_{AVG} (dBm)	$\mathrm{Eff}_{\mathrm{AVG}}$ (%)	ACLR No/with DPD (dBc)
[23]	3.5	9.1	36.0*	51	35*	28	43	27.8	N/A
[24]	3.53	11.2	40.3*	46.3	38*	20	40	43.0	−38/ − 45
[12]	3–3.6	11.5	N/A	43	37–41*	N/A	N/A	N/A	N/A
[18]	3.4–3.5	N/A	N/A	46	32*	100	37	30	30*/ − 40.4
[4]	3.4–3.5	9.5	40.5*	49.5	40–45*	100	40	43.5*	−29/ − 48
This work	3.4–3.6	12.3	41.0	49.2	48–52	100	41	45.2–47.5	−27/ − 48

* Graphically estimated.

than 1 dB is attained, which is mainly attributed to, in the authors' opinion, the employment of the resonator-type drain bias networks. With the digital predistortion technique, the proposed DPA shows a corrected ACLR of better than −48 dBc at about 41 dBm average output power and achieves a drain efficiency of higher than 45% from 3450 to 3550 MHz. The proposed asymmetrical DPA is compared with the similar 3500 MHz DPA in literatures, as listed in the Table 2. It can be seen that, with the proposed design approach, the asymmetrical DPA in this paper shows comparable or even better performance than the reported similar DPA.

5. CONCLUSION

In this paper, an asymmetrical Doherty power amplifier with improved linearity and enhanced back-off efficiency is proposed. The resonator-type drain bias network is introduced to reduce the memory effect of the ADPA when amplifying 100-MHz LTE-advanced signals. For efficiency enhancement, the general criteria for DPA design are outlined, and the procedure to obtain the optimum fundamental and harmonic impedances is presented. Driven with 100-MHz LTE-advanced signals, the ACLR asymmetry of the proposed ADPA is lower than 1.2-dB over a wide power range, which verifies the effectiveness of the proposed bias network in memory effects reduction. The average drain efficiency of the DPA is higher than 45% at about 41 dBm output power along with an linearized ACLR of lower than −48 dBc from 3450 to 3550 MHz. Experimental results demonstrate that the proposed asymmetrical DPA can achieve good linearity performance without degrading the average efficiency.

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