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Common-Mode Suppression Design for Gigahertz Differential Signals Based on C-Slotline

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Abstract—For wideband common-mode noise suppression in high-speed differential signals, a low-cost compact filter is proposed and designed by etching two coupled C-slotlines on the ground plane. It is found that the bandwidth of the common-mode stopband over −10 dB is from 2.4 GHz to 6.35 GHz with no degradation of the differential-mode insertion loss and group delay within the wide common-mode stopband. In time domain, the differential signal eye diagram is not deteriorated as well. In addition, an equivalent circuit model is developed and provides a quickly prediction of the common-mode stopband. The results show a good consistency between the simulations and measurements.

1. INTRODUCTION

With the trend of high data rate transmission, differential signals have played an important role in the high-speed digital circuits because of their high immunity to noise, low crosstalk, and low electromagnetic interference (EMI) [1, 2]. Several high-speed serial link formats, such as PCI-Express 2.0, Gigabit Ethernet, SATA III etc., have data rates over 5 Gbps under the differential signal transmission. However, the common-mode noise is unavoidable in practical circuits due to timing skew, amplitude unbalance along the differential signal paths, or different rising/falling time. The common-mode noise above gigahertz frequency range will degrade the signal integrity and power integrity of the high-speed circuit system. Moreover, in high-speed serial link applications, cables are always necessary to transmit differential signals between the different electronic devices and the common-mode noise may couple to the I/O cables and induce EMI issues [3]. As a result,suppressing the common-mode noise without affecting the differential signal quality has become a necessity in high-speed circuit design.

Several researches have contributed to the suppression of common-mode noise. The common-mode choke using a high permeability ferrite core is one of the most general approaches [4, 5], but this approach is valid only at MHz frequency range and the size reduction is difficult for the high density digital circuits [1]. For this reason, a broadband and miniaturized common-mode filter was proposed by Wu et al. [3] on the low-temperature co-fired ceramic (LTCC) with the common-mode noise suppression over −10 dB in the frequency range of 3.8–7.1 GHz. Recently, common-mode suppression filters employing the dumbbell-shaped [1] and UH-shaped [2] patterned ground plane were proposed based on PCB process. The proposed filter of [2] is more advanced than the one of [1] due to smaller size and bandwidth enhancement. Besides, periodic complementary split ring resonators (CSRRs) [6] are used by Naqui et al. to the application of common-mode suppression. In [7], a common-mode filter consisted of meandered signal pair and an improved mushroom-type cell embeded in a PCB or package substrate is proposed to efficiently reduce the EMI, but four layers and two metal vias are needed resulting in a complex design and high cost. The common-mode suppression behavior is also

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investigated based on planar electromagnetic bandgap structures by Orlandi et al. in [8]. Besides, the artificial transmission line [9] and the multilayer liquid crystal polymer technology [10] are used in the common-mode suppression as well, and the balanced bandpass filters based on them are successfully designed.

In this paper, a novel miniaturized and simplified common- mode filter is proposed for a wideband GHz common-mode noise suppression based on standard 2-layer PCB process. The proposed common-mode filter consists of a pair of coupled microstrip lines on top of the substrate, and two symmetrical coupled C-slotlines etched on the ground plane. The inner coupling between the C-slotlines can effectively broaden the common-mode stopband bandwidth. An equivalent circuit model is established to explain the common-mode suppression characteristics and to quickly predict the common-mode stopband by the calculation of the common-mode insertion loss (S_{cc21}). Compared with the previous work [1, 2, 6] which all implemented on 2-layer PCB, the proposed structure has the smallest electric size as well as the maximum fractional bandwidth. Moreover, the proposed common-mode filter has the advantages of simple configuration design in contrast to the previous design in [2, 3, 6–9].

This paper is organized as follows. Section 2 presents the common-mode filter based on C-slotline and its design concept. In Section 3, common-mode stopband enhanced filter based on coupled C-slotlines and its equivalent circuit mode are proposed and discussed. To demonstrate the excellent common-mode noise suppression performance, the experimental results are given in Section 4. Finally, the conclusions are drawn in Section 5.

2. COMMON-MODE FILTER BASED ON C-SLOTLINE

In [11], periodical straight slotlines are used to design a novel compact forward-ware directional coupler, and it has pointed out that the straight slotline can also be utilized to suppress the common-mode noise. Fig. 1(a) shows such a common-mode filter with the coupled microstrip lines on top of the substrate and a straight slotline etched symmetrically on the ground plane. Here, in this paper, only one straight slotline is applied instead of periodic slotlines in [11]. To reduce the size in the y direction shown in Fig. 1(a), the straight slotline is bent and formed a so-called "C-slotline" in Fig. 1(b). It will be shown, in the following, that the C-slotlines can easily be coupled with each other to broaden the common-mode stopband bandwidth as well as decreasing the size in the y direction. In order to avoid the magnetic field coupling between the coupled microstrip lines and the short-circuited terminal of the C-slotline, the distance d is taken as 1 mm in this paper, as shown in Fig. 1(b).

The corresponding geometrical parameters are denoted as (W_m, S_m) for the coupled microstrip lines, (L, W) for the straight slotline (see Fig. 1(a)) and (L_1, L_2, L_3, W_s) for the C-slotline (see Fig. 1(b)). The substrate is chosen as FR4 ($\varepsilon_r = 4.5$, $\tan\delta = 0.035$) with a of $h = 0.4$ mm. If we choose the geometrical parameters $W_m = 0.55$ mm, $S_m = 0.36$ mm, the odd- and even-mode characteristic impedance of the coupled microstrip line are 50 Ω and 65 Ω, respectively. The 50 Ω odd-mode characteristic impedance

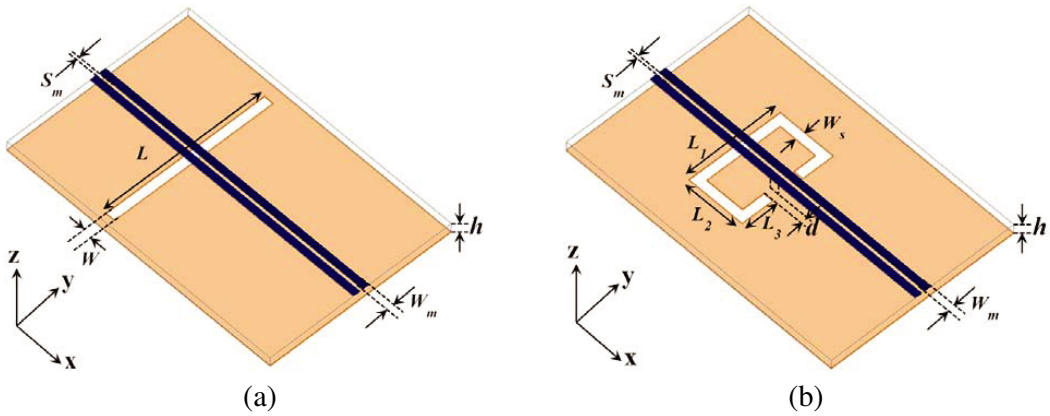


Figure 1. Three-dimensional view of the common-mode filter based on (a) a straight slotline, (b) C-slotline.

Table 1. Geometrical parameters for the common-mode filters shown in Fig. 1.

Fig. 1(a)	$L = 26\,\text{mm}$		$W = 1\,\text{mm}$	
Fig. 1(b)	$L_1 = 10\,\text{mm}$	$L_2 = 6\,\text{mm}$	$L_3 = 6\,\text{mm}$	$W_s = 1\,\text{mm}$

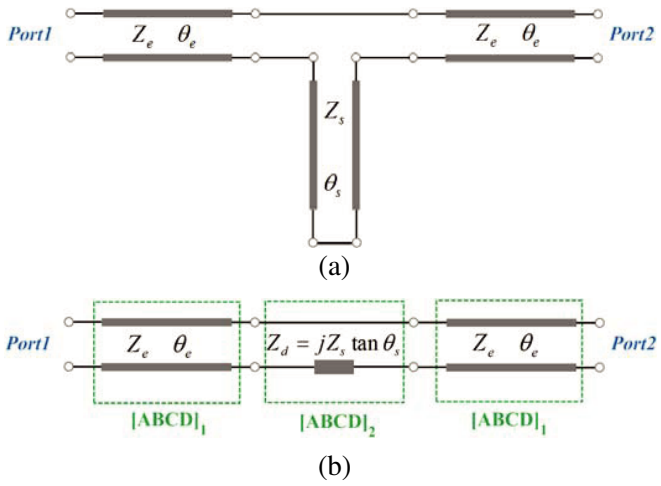


Figure 2. Equivalent circuit model of the common-mode filter shown in Fig. 1 for the even-mode analysis: (a) general model, and (b) its simplified model.

is chosen for the differential signal transmission on the coupled microstrip line. An example of the geometrical parameters of the common-mode filters in Figs. 1(a) and (b) is listed in Table 1, in which the total length of the C-slotline is equal to that of the straight slotline.

Due to the symmetry of the structures in Fig. 1, the even-mode equivalent circuit model is shown in Fig. 2(a) by applying the perfect magnetic wall at the central plane between the coupled microstrip lines [11, 12]. The coupled microstrip lines will work in odd mode to propagate the differential signal, while the even mode is actually the common-mode for the coupled microstrip lines. Therefore, we only give the even-mode equivalent circuit model and will focus on investigating the even-mode in the following.

As illustrated in Fig. 2(a), two transmission lines of characteristic impedance Z_e and electric length θ_e are connected by a short circuited slotline with the characteristic impedance Z_s and the electric length θ_s, which can be calculated by the formulas (1)–(3) in [12].

$$\begin{aligned} Z_{\text{s}} &= 73.6 - 2.15 \cdot \varepsilon_r + (638.9 - 31.37 \cdot \varepsilon_r)\left(\frac{W_s}{\lambda_0}\right)^{0.6} + \left(36.23\sqrt{\varepsilon_r^2 + 41} - 225\right)\frac{W_s/h}{(W_s/h + 0.876 \cdot \varepsilon_r - 2)} \\ &\quad +0.51(\varepsilon_r + 2.12)\left(\frac{W_s}{h}\right)\ln\left(100 \cdot \frac{h}{\lambda_0}\right) - 0.753 \cdot \varepsilon_r \frac{(h/\lambda_0)}{\sqrt{W_s/\lambda_0}} \end{aligned} \tag{1}$$

$$\theta_s = \beta_{slotline} l_{slotline} = \frac{2\pi}{\lambda_s} l_{slotline} \tag{2}$$

$$\begin{aligned} \frac{\lambda_s}{\lambda_0} &= 0.9217 - 0.277 \cdot \ln(\varepsilon_r) + 0.0322\left(\frac{W_s}{h}\right)\left(\frac{\varepsilon_r}{W_s/h + 0.435}\right)^{0.5} \\ &\quad -0.01 \cdot \ln\left(\frac{h}{\lambda_0}\right)\left[4.6 - \frac{3.65}{\varepsilon_r^2\sqrt{W_s/\lambda_0(9.06 - 100 \cdot W_s/\lambda_0)}}\right] \end{aligned} \tag{3}$$

In fact, the equivalent circuit model in Fig. 2(a) can be simplified as Fig. 2(b) with $Z_d = jZ_s \tan\theta_s$.

From Fig. 2(b), the transmission matrix can be written as

$$[ABCD]_T = [ABCD]_1 [ABCD]_2 [ABCD]_1 = \begin{bmatrix} A_T & B_T \\ C_T & D_T \end{bmatrix} \tag{4}$$

and the common-mode insertion loss is

$$S_{cc21} = \frac{2}{A_\mathrm{T} + B_\mathrm{T}/Z_0 + C_T Z_0 + D_T} \tag{5}$$

where Z_0 is the port impedance.

The calculated common-mode insertion loss is shown in Fig. 3 for the common-mode filters in Fig. 1(a) and (b). The results by the full wave software HFSS [18] are also added for comparison. One can see that good agreement is achieved. The slight discrepancy is mainly due to it that the transmission line model of the slotline is assumed to be ideal short-circuited. It can also be observed that there is a narrow common-mode stopband bandwidth ($|S_{cc21}| < -10\,\mathrm{dB}$ @ 3.6 GHz–5.6 GHz) for both of the C-slotline and the straight slotline. This is because only one unit cell (straight slotline and/or C-slotline) is used. To broaden the common-mode stopband bandwidth, two coupled C-slotlines are used in the following design.

3. PROPOSED COMMON-MODE FILTER BASED ON COUPLED C-SLOTLINES

Figure 4 illustrates the proposed common-mode filters based on coupled C-slotlines, where the gap width W_g between the two C-slotlines is 0.5 mm. Other geometrical parameters are taken the same as those in Section 2. The coupled C-slotlines structure is introduced here to broaden the common-mode stopband bandwidth due to its inner coupling.

In order to predict the common-mode stopband for the common-mode filter in Fig. 4, the equivalent circuit model and its corresponding simplified model are, respectively, given in Figs. 5(a) and (b) for the even-mode analysis. To provide a conceptual understanding of the equivalent circuit model, one half configuration of the proposed common-mode filter is also included in Fig. 5(a).

In the simplified equivalent circuit model (Fig. 5(b)), there are 4 blocks which are all two-port networks. Based on the definition of the port voltages and currents of the 4 blocks, one can see that block 1 and block 2 are in series to form a large block 12. The impedance matrix of this block 12 can then be expressed as

$$[Z]_{12} = [Z]_1 + [Z]_2 \tag{6}$$

where $[Z]_1$ and $[Z]_2$ are, respectively, the impedance matrices of the blocks 1 and 2. In block 2, there are 3 subblocks in cascaded in which the transmission matrix for the coupled slotlines in subblock 2 is

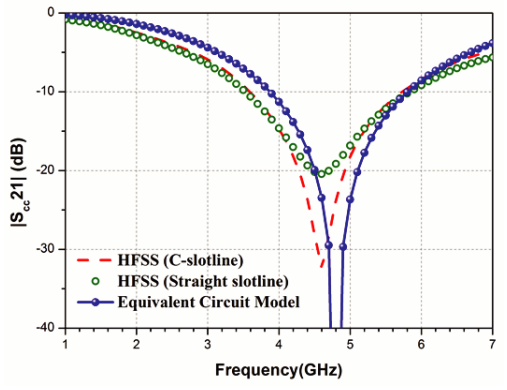


Figure 3. Comparsion of the common-mode insertion loss by the equivalent circuit model and HFSS for the common-mode filter in Fig. 1.

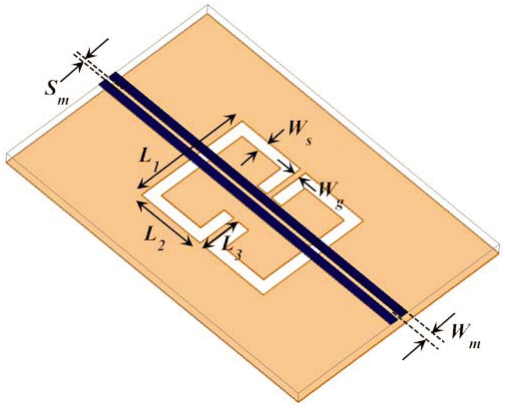


Figure 4. Proposed common-mode filters based on coupled C-slotlines.

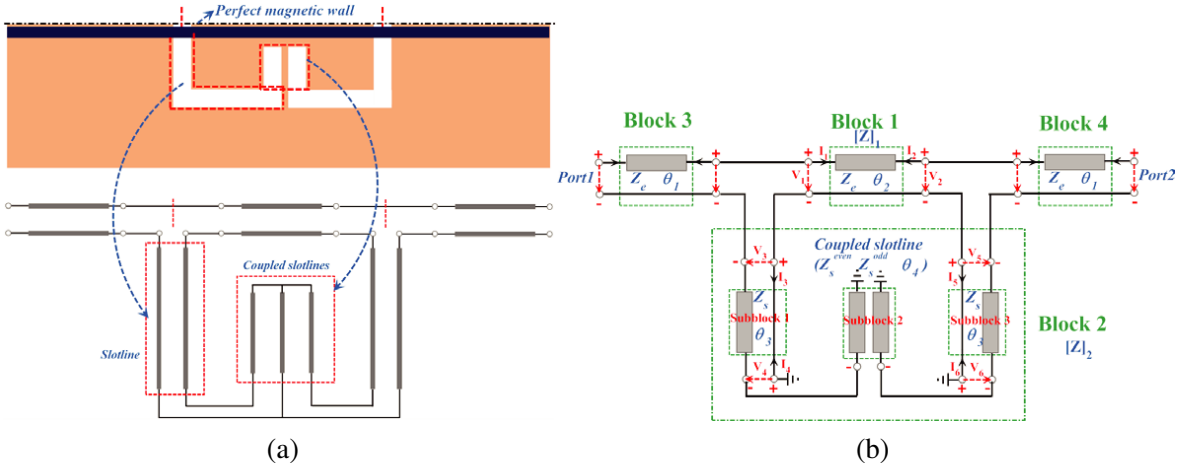


Figure 5. Equivalent circuit model of the proposed common-mode filter for even-mode analysis: (a) the original model, (b) the simplified model.

given here for clearance [13]:

$$[ABCD]_{s2} = \begin{bmatrix} \dfrac{Y_s{}^{odd} + Y_s{}^{even}}{Y_s{}^{odd} - Y_s{}^{even}} & j\dfrac{2\tan\theta_4}{Y_s{}^{odd} - Y_s{}^{even}} \\ -j\dfrac{2Y_s{}^{odd}Y_s{}^{even}\cot\theta_4}{Y_s{}^{odd} - Y_s{}^{even}} & \dfrac{Y_s{}^{odd} + Y_s{}^{even}}{Y_s{}^{odd} - Y_s{}^{even}} \end{bmatrix} \tag{7}$$

with $Y_s{}^{odd} = \frac{1}{Z_s{}^{odd}}$ and $Y_s{}^{even} = \frac{1}{Z_s{}^{even}}$. $Z_s{}^{even}$, $Z_s{}^{odd}$ can be obtained from the numerical method [14, 15] or the extraction from the coupled slotlines model [17] as

$$Z_s^i = Z_0\sqrt{\frac{(\mathrm{S}_{21,i}^2 - \mathrm{S}_{11,i}^2 - 1) - 2\mathrm{S}_{11,i}}{(\mathrm{S}_{21,i}^2 - \mathrm{S}_{11,i}^2 - 1) + 2\mathrm{S}_{11,i}}}\, i = even,\ odd \tag{8}$$

and θ_4 is defined according to the electric length of the even mode of the coupled slotline (i.e., coplanar waveguide mode) [16] because the even/odd mode dielectric lengths of the coupled slotline in Fig. 5(b) are approximately equal. The transmission matrices of the subblocks 1 and 3, together with blocks 1, 3 and 4, are easily obtained and not given here.

Figure 6 gives the simulated results by the equivalent circuit model in Fig. 5 and HFSS. It can be observed that there is a broadened common-mode stopband due to the coupling between the two C-slotlines, compared with that in Fig. 5. Good agreement between the equivalent circuit model and HFSS can be seen. Moreover, two transmission zeros (2.7 GHz and 5.8 GHz) can also be observed which agrees with the HFSS result. Therefore, the equivalent circuit model in Fig. 5 can be used to quickly predict the common-mode stopband bandwidth at the initial design. It should be noted that the equivalent circuit model proposed in this paper is different from the one of the common-mode suppression design based on coupled defected ground structure (DGS) in [2]. The coupled C-slotline is modeled as transmission line in this paper, while the DGS is modeled as lumped LC circuits. A peak around 6 GHz in the curve of equivalent circuit model is mainly caused by the resonance, where $L_1 + L_2 + L_3 - W_s = 13$ mm (Fig. 5(b)) is about one guided wavelength at 6 GHz.

Finally, the effect of the design parameter L_3 and W_g on the lower and upper bound cutoff frequencies (f_L, f_H) is investigated by parametric analysis, respectively. In the parametric analysis, the total length of the C-slotline is unchanged and other geometrical parameters of the C-slotline described in Section 2 are used. For the calculation of f_L and f_H, the common-mode stopband is defined as $|S_{cc21}| < -10$ dB which is good enough in high-speed digital circuit application [2, 3]. The calculated results by the equivalent circuit model and HFSS are shown in Figs. 7(a) and (b). Good consistency is observed. It can be seen that the change of W_g will have more influence on the f_L and f_H than that of

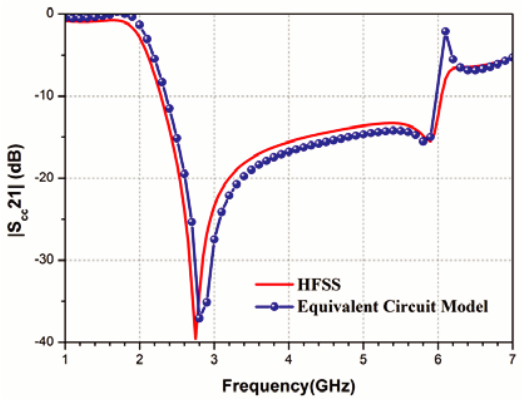


Figure 6. Comparison of $|S_{cc21}|$ by the equivalent circuit model and HFSS for the proposed commonmode filter of Fig. 4.

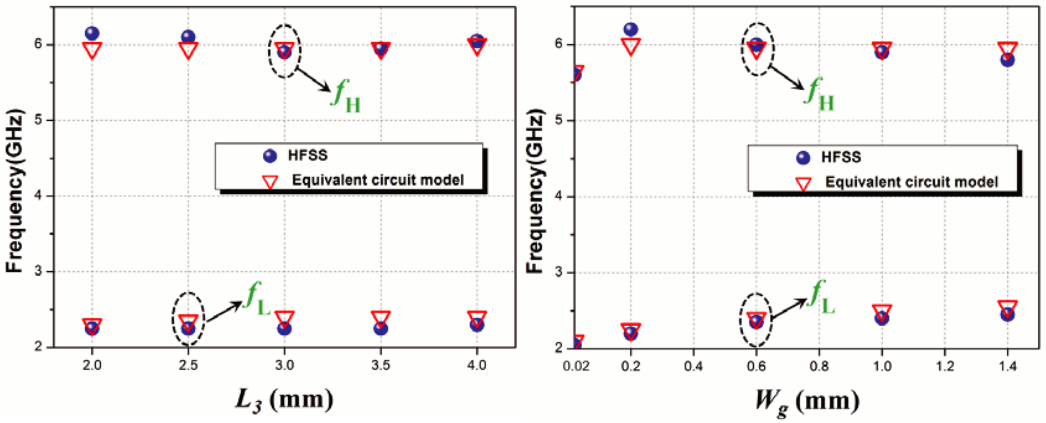


Figure 7. Calculated f_L and f_H of the proposed common-mode filter by equivalent circuit model compared with HFSS (a) with different L_3, (b) with different W_g.

L_3. When W_g decreases, f_L will decrease and f_H will increase. If W_g is very small, e.g., 0.02 mm, f_H will decrease since the common-mode stopband will split into two stopbands according to the criterion of $|S_{cc21}| < -10$ dB. Hence, $W_g = 0.5$ mm and $L_3 = 4.0$ mm are chosen in this paper based on the consideration of the common-mode stopband bandwidth, suppression level and fabrication tolerance, etc..

4. RESULTS AND DISCUSSION

The proposed common-mode filter in Fig. 4 with the geometrical parameters described in Section 3 is fabricated, and its photograph is shown in Fig. 8. A four-port vector network analyzer (Agilent N5244A) was used for the mixed-mode S-parameter measurement with Short-Open-Load-Thru (SOLT) calibration. Fig. 9(a) depicts the measured insertion losses for the differential-mode (S_{dd21}) and the common-mode (S_{cc21}). The results by equivalent circuit model and HFSS are also added for comparisons.

From Fig. 9, reasonably good consistency between the measured and simulated results can be seen, and there is a wide stopband of 2.4–6.35 GHz for the common-mode insertion loss (S_{cc21}). On the other hand, the differential-mode insertion loss (S_{dd21}) is not deteriorated within the common-mode stopband. The discrepancies between the measurements and the simulations for the common-mode and differential-mode insertion losses at high frequencies are mainly come from the fabrication tolerance,

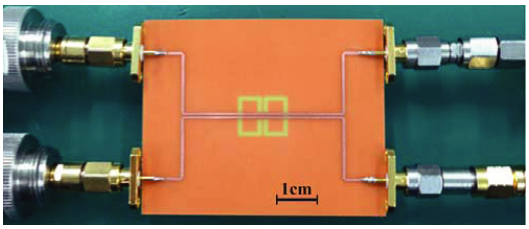
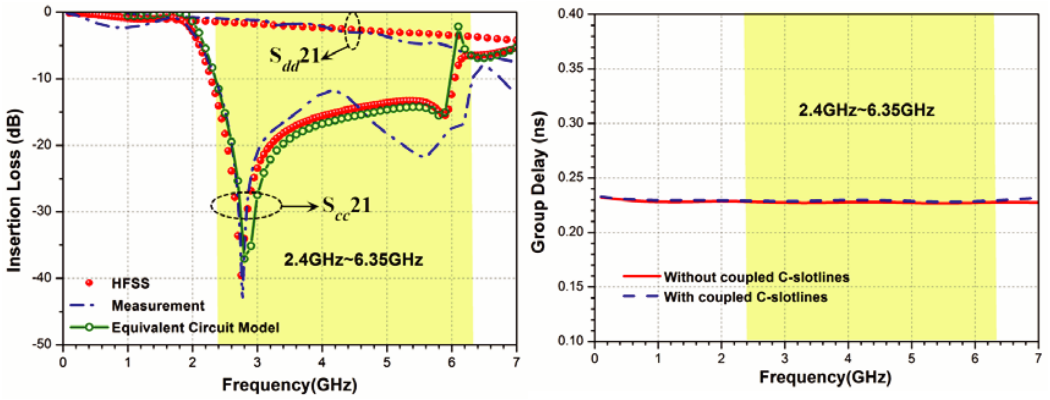


Figure 8. The photograph of the fabricated common-mode filter.

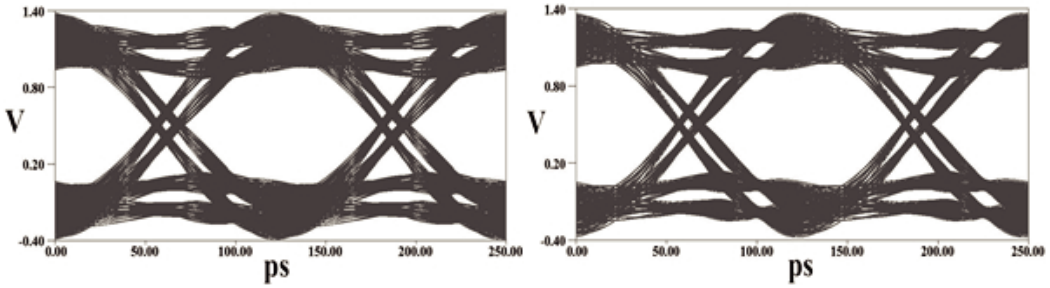


(a) (b)

Figure 9. The comparisons of (a) the insertion losses for the differential and common modes, and (b) the group delay for the differential-mode with and without the coupled C-slotlines.

Table 2. Eye diagram summary.

	Max. Eye Width	Max. Eye Height	Jitter
Common-mode filter	106 ps	869 mV	20 ps
Reference board	107 ps	888 mV	18 ps



(a) (b)

Figure 10. Simulated differential-mode eye diagrams for: (a) common-mode filter and (b) reference board.

substrate loss of FR4 and the conductor loss of the SMA used.

To keep good signal integrity for the differential signals, the group delay for the differential-mode also cannot be distorted by the coupled C-slotlines. Fig. 9(b) compares the differential-mode group delay of the proposed common-mode filter with and without the coupled C-slotlines. It is found that

the group delay in the common-mode stopband is almost the same with maximum error of 0.5%.

Figures 10(a) and (b) show the simulated differential-mode eye diagrams by Ansoft Designer [19] for the common-mode filter board and the reference board whose ground plane is solid, respectively. The input signal is 8 Gbps with 1 V amplitude. The eye diagram quality in terms of maximum eye height, maximum eye width, and jitter is compared and summarized in Table 2. It can be seen that the signal integrity of the differential signal is maintained by the proposed common-mode filter. It is verified again in time domain that the proposed common- mode filter exhibits excellent signal integrity of the differential signal.

As shown in Table 3, compared to previously reported data which realized on 2-layer PCB technology [1, 2, 6], the proposed common-mode filter has the maximum fractional bandwidth and the most compact electrical size with a simple configuration design. Regarding the common-mode suppression design in [8], the proposed common-mode filter has a larger fractional bandwidth and a simpler structure, while the suppression level and the electrical size are worse than those in [8]. The deep common-mode suppression level (with $|S_{cc21}| < -20$ dB) of the common-mode filter ([1, 6, 8]) is better

Table 3. Characteristic of the proposed common-mode filter compared with previous literatures.

Ref.	Design Technique	Frequency Range (GHz)	Fractional Bandwidth	Suppression Level $\lvert S_{cc21}\rvert$	Electrical Size $\lambda_g{}^2$	Technology	Configuration Design	Substrate material
[1]	Dumbbell-shaped (3 unit cells)	3.3–5.7	53.3%	< -20 dB	0.47×0.76	2-layer PCB	Simple	FR4
[2]	UH-shaped	3.8–9.7	87%	< -10 dB	0.44×0.44	2-layer PCB	Complex	FR4
[3]	Metamaterial Transmission Line	3.8–7.1	60.6%	< -10 dB	0.16×0.26	4-layer PCB	Complex	LTCC substrate ($\varepsilon_r = 7.8$)
[6]	CSRR (3 unit cells)	1.1–1.6	37.0%	< -20 dB	–	2-layer PCB	Complex	Rogers RO3010 ($\varepsilon_r = 10.2$)
[7]	Meandered Signal Pair and Improved Mushroom-type Cell	1.65–5.2	103.6%	< -10 dB	0.11×0.11	4-layer PCB	Complex	FR4
[8]	Artificial Transmission Line	2–4	67%	< -20 dB	0.32×0.22	2-layer PCB	Moderation	$\varepsilon_r = 2.43$
[9]	Multilayer LPC Technology	3.2–5.5	53%	< -10 dB	0.43×0.19	Multilayer LPC	Moderation	$\varepsilon_r = 3.15$
This Work	Coupled C-Slotlines	2.4–6.35	90.3%	< -10 dB	0.3×0.38	2-layer PCB	Simple	FR4

due to the application of periodic structure. For the multilayer common-mode filters (based on the metamaterial transmission line [3] and the hybrid structure of meandered signal pair and an improved mushroom-type cell [7], and LPC technology [9]), this work shows a good compromise between the common- mode suppression, design complexity and fabrication cost.

5. CONCLUSION

In this paper, a novel common-mode suppression design based on C-slotline is proposed. The common-mode stopband enhancement is investigated based on coupled C-slotlines. Its even-mode equivalent circuit model is established to characterize the common-mode suppression performance and provide a quick prediction of the common-mode stopband. Finally, the excellent common-mode suppression performance is demonstrated by the full-wave simulation and measurement. Compared with previous common-mode filters, the proposed structure has significantly simplified the design as well as improving the common-mode suppression performance and reducing the electrical size.

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