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Design of Sub-Harmonic Mixer MMIC for EHF Satellite Links

Diego Palombini[1, *], Tommaso Cavanna[2], Sergio Arena[2], and Ernesto Limiti[1]

Abstract—This paper presents the design flow of a compact GaAs MMIC for Extremely High Frequency (EHF) satellite communications. The proposed circuit enables sub-harmonic mixing capability and integrates a LO buffering section, thus allowing for low frequency and low power reference signal interface. Circuit design is described in detail providing a comprehensive view of the followed theoretical approach, starting from mixer core definition until the complete synthesis of LO/RF/IF interfaces. In particular, the design flow of an innovative three-conductor Marchand balun is deeply analysed. Fabricated MMIC operates in the 43.5–50 GHz band and results in a compact layout ($2.4 \times 2.4\,\mathrm{mm}^2$) featuring a port-to-port isolation better than 25 dB with a typical conversion loss of 12 dB.

1. INTRODUCTION

During past decades, intense research efforts in spaceborne electronic field have dramatically changed the satellite industry and lead to profound implications in radio-communication networks. New electronic devices and circuit topologies have been introduced while high performance fabrication processes have been progressively qualified: all these technology improvements have contributed to the growth of the satellite communication segment which is fairly close to becoming the real backbone for high-speed digital data links [1].

Although Ku and Ka bands have traditionally played a key role in the successful realization of robust satellite links, recent years have been characterized by a gradual migration toward higher frequency ranges, as a consequence of the crowding of conventional Super High Frequency (SHF) bands, together with pressing demand for challenging data-rates and high quality-of-service (QoS) requirements [2]. While moving toward higher frequency bands could resolve for spectrum allocation and bandwidth issues, on the other hand it necessarily leads to manifold technical drawbacks, particularly related to degraded propagation characteristics: improvement in antenna directivity is counterbalanced by the worsening of atmospheric fading at EHF range which imposes severe limitations on feasible radio link performance [3, 4]. The search of a trade-off between attainable bandwidth and channel propagation characteristics identifies Q/V band as one of the most favourable transmission windows for the realization of broadband satellite links.

Such an evolution in space communication segment has strongly driven the industrial as well as academic interest in microwave theory and technique, settling the technological roadmap: in this context, remarkable example of GaAs multifunctional chipset and TX/RX front-end can be found in literature [5, 6]; furthermore, different contributions proved the feasibility of RADAR and communication payloads at EHF domain [7, 8]. In particular, commercial-grade GaAs technologies were successfully employed in the realization of different functionalities as low noise amplification and complex signal conditioning [9, 10].

Recently, several effective implementations of Q-band mixers have also been demonstrated both as standalone circuit [11, 12] and as a building block in down-converters [13] and modulators [14]. This

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* Corresponding author: Diego Palombini (diego.palombini@uniroma2.it).

[1] Department of Electronic Engineering, University of Rome Tor Vergata, Via del Politecnico 1, Rome 00133, Italy. [2] Wave Advanced Technology Applications s.r.l., Via Ardito Desio 60, Rome 00131, Italy.

contribution presents the design and performance of a MMIC mixer for EHF operation, enabling the realization of compact and low-power consuming communication payloads in a robust space-qualified technology. Aim of the project, sponsored by the Italian Space Agency, is to allow the implementation of reliable satellite links, capable to support high data rate digital communication in a quite unexploited range of the electromagnetic spectrum. In the present contribution, Section 2 is dedicated to the analysis of the mixer architecture. Section 3 deals with the detailed design of different functional blocks. Finally in Section 4, mixer experimental results are illustrated and compared with simulations.

2. MIXER ARCHITECTURE

Although technological feasibility of stand-alone mmW mixers has already been proved, new difficulties arise when complex satellite payloads are concerned: in particular, as the frequency of the system increases, local oscillator generation and distribution become an issue; moreover, if the correct phase relationship between radiating elements represents a key feature, as in beam forming operation, LO signal delivery emerges as the main criticality. Implementation of reliable space communication systems can only be accomplished if the most effective approach for LO frequency reduction is selected: main strategies are substantially based on sub-harmonic mixing (SHM) [15–18] or LO signal multiplication [19, 20]. Referring to [21] for a detailed comparison between two alternatives, the present contribution deeply investigates the former architecture, giving insight into the design procedure.

As known, SHM topology consists of different sub-circuits whose complexity strictly depends on the selected harmonic product, balancing order and other specific requirements as conversion gain and linearity. In the present case, a double-balanced architecture was chosen, so that the mixer core had to be provided with three distinct baluns (for LO,RF, and IF ports), each one implementing different functionalities (as matching, DC grounding/blocking and filtering), besides balancing the signal. Furthermore, a dedicated RF/IF decoupling network and a LO buffer amplifier were inserted in order to enhance ports isolation and circuit linearity respectively.

A schematic picture of the presented MMIC is reported in Fig. 1, showing the complete mixer block diagram. In the following section, distinct paragraphs are dedicated to the analysis of each block, providing, at the same time, a detailed description of the followed design technique.

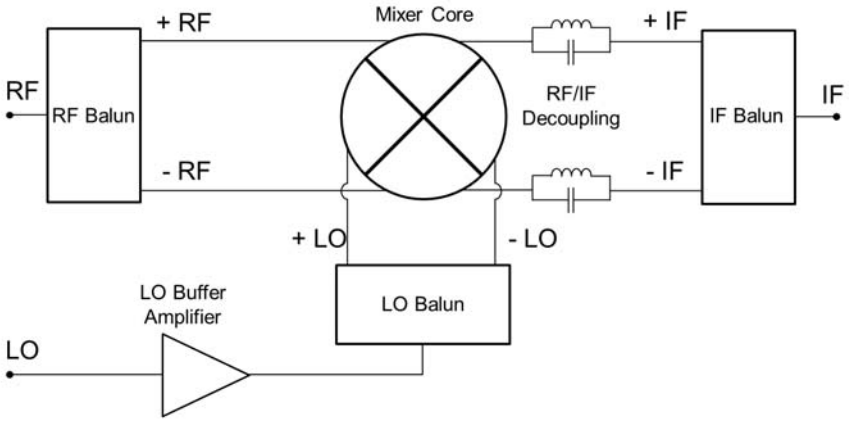

Figure 1. Mixer block diagram.

3. MMIC DESIGN

The presented SHM is intended to operate between the Q (43–50 GHz) band and X (7–8.5 GHz) band by means of a 18–21 GHz LO pump signal. Actually, the main challenge in MMIC design is to accommodate, within the same chip, several different structures, in a mixed lumped/distributed implementation depending on the respective frequency of operation. The circuit is realized in a pseudomorphic GaAs 250 nm gate length foundry process by UMS (PH25). Such an industrial-grade technology is based

on a GaAs-InGaAs-AlGaAs active layer, grown by molecular beam epitaxy on semi-insulating GaAs substrate. Active devices in typical class A bias are featured by 250 mW/mm of output power at 1 dB compression with 30% associated power added efficiency. Mixing diodes are designed for low junction capacitance as well as low series resistance and exhibit calculated cutoff frequencies as high as 330 GHz. In the remainder of the section, the design of different building blocks will be closely described, providing details about the mixing core architecture and chosen balancing/filtering/amplifying networks.

3.1. Mixer Core

The choice of the best mixing core arrangement is mandatory for obtaining desired circuit performance, as it mostly determines achievable figure of merit such as conversion gain, isolation and linearity. Sub-harmonic design starts from basic Anti-Parallel Diode Pair (APDP) cell that intrinsically provides RF signal beating with only even LO harmonics; cell symmetry is fundamental for odd harmonic internal circulation (suppression). Balancing order also plays a key role in targeting mixer requirements, as it mainly regulates ports isolation at the expense of increased circuit complexity. As a second order effect, it also improves mixer linearity, provided that enough LO power can drive a higher number of non-linear devices. Unfortunately, conversion gain will typically fade out with increasing the balancing order [22]: taking into consideration relative proximity between LO (18–21 GHz) and IF (7–8.5 GHz) bands, and between 2LO (36–42 GHz) and RF (43–50 GHz) bands. Double-balanced ring topology, as reported in Fig. 2, is the only feasible architecture for the present application.

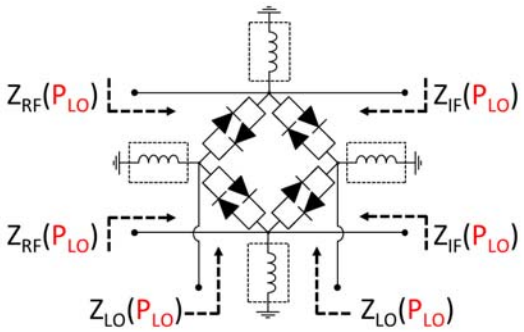

Figure 2. Double-balanced mixer core (ideal harmonic terminations).

As a second step, diodes periphery has to be carefully selected trading-off among conversion gain, bandwidth and linearity: accurate parametric simulations on different device peripheries allow choosing the best device geometry and required LO drive level. More in detail, RF port (differential) impedance in the circuit of Fig. 2 can be modelled as an RC parallel circuit featured by the Q factor:

$$Q = \omega_0 RC \tag{1}$$

As a consequence of diodes' non-linear behaviour, mixer core impedance strongly depends on LO drive level (see again Fig. 2): actual impedance value at each port can only be estimated by means of a Harmonic-Balance analysis, as the ratio between the fundamental-frequency voltage and current phasors. Such simulation also requires to impose proper harmonic impedance terminations of the circuit: in this case, an ideal short circuit has been imposed for the DC component while open circuits have been imposed for higher order harmonics (as the ideal inductances in Fig. 2 testify). Now, fixing device periphery and increasing the LO power, R component exponentially decreases while the C component roughly maintains the same value with an overall effect of Q factor reduction. On the other hand, by fixing LO power and varying device size, Q factor remains constant since R and C components respectively respond with a direct and inverse proportional law to periphery variation: Q factor can be assumed as an invariant only dependent on the technology and LO power level, as reported in left Y axis of Fig. 3. According to Bode-Fano limitation [23], the lowest is the Q factor, and the best is the achievable return loss on a fixed bandwidth. However, this analysis does not take into account of the real part of the load to be matched: again referring to Fig. 3 (right Y axis), the same LO power level leads to different conversion gains, at central frequency of the band, according to device size.

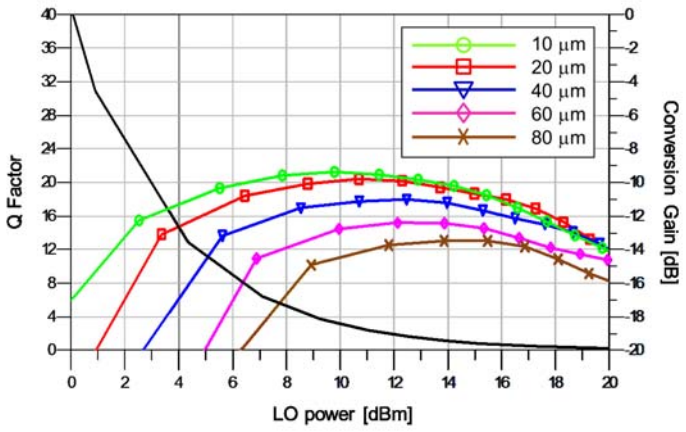

Figure 3. Q factor (left Y axis) and conversion Gain at band centre (right Y axis).

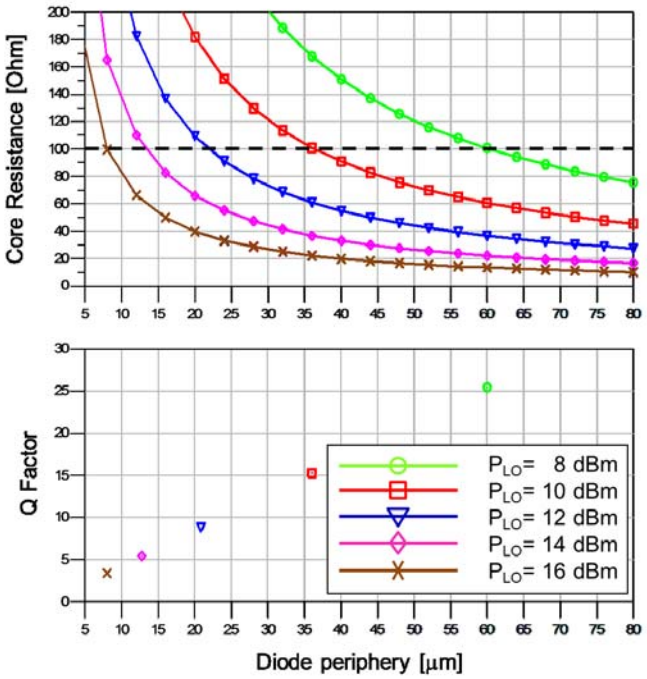

Figure 4. Mixer core differential resistance (upper Y axis) and Q factor (lower Y axis).

Above-described phenomenon can be explained looking at the graph in Fig. 4, where the real part of the load (R component) is plotted (on the upper Y axis) as a function of device periphery for different LO power levels. In the same graph, (lower Y axis) the correspondent value of Q factor is reported. Target value of 100 Ohm (differential) resistance can be reached by different LO power levels and device size arrangements; however, combination featured by the largest peripheries suffers from too high Q factor (poor matching and conversion gain) while combination featured by the smallest peripheries requires too much LO power and may result in poor linearity performance: in conclusion, a $4 \times 6\,\mu$m device, driven by at least 12 dBm of LO power, emerges as the best solution.

Large signal differential impedance simulation (the same Harmonic-Balance analysis described above) can be now performed, at each port, pumping the mixing core with the correct LO power level: this is a crucial design step since it determines the required LO, RF and IF balun impedance transformation ratio. Furthermore, characteristic impedance and electrical length of adduction lines

(connecting baluns to the mixer core) should be carefully optimized, in order not to worsen ports impedance quality factor but to partially compensate for its capacitive behaviour. In particular, large signal impedance, at LO side, is improved by means of a high-pass tee section, featuring short-circuited stubs.

3.2. RF/IF Decoupling Network

Even tough RF to IF isolation is partially guaranteed by the double-balanced topology, additional circuitry is necessary, in order to properly feed diodes non-linearity with the incoming RF excitation and to extract the converted IF signal. Unlike traditional double-balanced ring mixer (where IF port is located on the virtual ground for RF circuit), IF balun is directly connected to the RF balanced port, so that suitable RF/IF decoupling network turns out to be mandatory. Such a filtering structure should physically implement an open circuit for RF band, preventing incoming signal from flowing toward IF port, thus worsening conversion loss; at the same time, it should be completely transparent for IF signal.

The network described above ideally behaves as a parallel L-C resonator in series to the balanced IF port: taking into account RF relative bandwidth, the most convenient way to realize the decoupling network is connecting a quarter wavelength open-ended stub by a quarter wavelength distance from the RF balun insertion point (see Fig. 5).

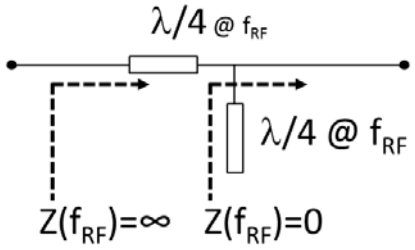

Figure 5. RF/IF decoupling network.

3.3. LO Section

LO circuitry has to be designed in order to ensure a matched, single-ended, external interface. More in detail, this section should provide four distinct functionalities:

1. Single-ended to balanced transformation
2. LO port impedance transformation
3. Mixing core ground reference
4. LO power amplification

Considering the moderately high frequency of LO signal (around 20 GHz), LO port interface is compatible with a distributed implementation of balun circuit. Furthermore, the small impedance transformation ratio allows using traditional Marchand balun topology in its conventional form [24], where $\lambda/4$ grounded ends serve as useful DC ground for APDP mixer core.

Finally, the insertion of a LO buffer stage can substantially improve mixer linearity performance. Moreover, local amplification of pump signal further simplifies LO reference delivery at system level. Referring to the analysis performed in 3.1, mixer core must be driven by at least 12 dBm of pump signal: the need for a robust, in-band equalized, LO reference suggests the implementation of a single stage feedback amplifier, providing more than 12 dBm of output power with 6 dB gain in an extremely linear operation. For this aim, a 6×50 μm active device is employed: amplifier, self biased for class A operation, minimizes routing complexity, featuring 250 mW power consumption. Besides, it is worthwhile to point out that part of the drain supply voltage drops across a dummy resistor inserted for testing purposes only on external (5V) DC supply: overall MMIC power consumption would be only 150 mW. Schematic representation of entire LO section is reported in Fig. 6.

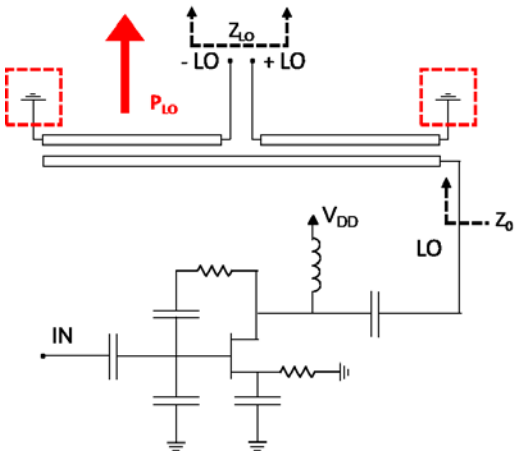

Figure 6. LO section (balun and buffer amplifier).

3.4. RF Section

Development of the RF section is undoubtedly the most challenging step in the design of the mixer; as a matter of fact, RF circuitry should provide three distinct functionalities:

1. Single-ended to balanced transformation
2. RF port impedance transformation
3. High dynamic impedance with respect to IF signal

Unlike LO port, RF port requires a high transformation ratio from the really low differential impedance, at mixer core level, toward the external 50 Ohm; such impedance matching is further complicated because of the high load quality factor at operation frequency (43–50 GHz). Moreover, the need for a high IF impedance prevents from using a conventional transformer with the secondary conductor connected to ground.

As known, traditional Marchand balun suffers from the poor coupling factor between coupled lines sections edges: such a restriction typically results in a narrow operating bandwidth and limited single ended to differential impedance transformation ratio. This is clearly demonstrated by the complete balun S matrix at bandwidth centre, as derived in [24], where Z_0 and Z_D represent input single-ended impedance and output differential impedance respectively:

$$S = \begin{bmatrix} \frac{1-C^2\left(\frac{Z_D}{Z_0}+1\right)}{1+C^2\left(\frac{Z_D}{Z_0}-1\right)} & j\frac{C\sqrt{2(1-C^2)}\sqrt{\frac{Z_D}{Z_0}}}{1+C^2\left(\frac{Z_D}{Z_0}-1\right)} & -j\frac{C\sqrt{2(1-C^2)}\sqrt{\frac{Z_D}{Z_0}}}{1+C^2\left(\frac{Z_D}{Z_0}-1\right)} \\ j\frac{C\sqrt{2(1-C^2)}\sqrt{\frac{Z_D}{Z_0}}}{1+C^2\left(\frac{Z_D}{Z_0}-1\right)} & \frac{1-C^2}{1+C^2\left(\frac{Z_D}{Z_0}-1\right)} & j\frac{\sqrt{2}C^2\sqrt{\frac{Z_D}{Z_0}}}{1+C^2\left(\frac{Z_D}{Z_0}-1\right)} \\ -j\frac{C\sqrt{2(1-C^2)}\sqrt{\frac{Z_D}{Z_0}}}{1+C^2\left(\frac{Z_D}{Z_0}-1\right)} & j\frac{\sqrt{2}C^2\sqrt{\frac{Z_D}{Z_0}}}{1+C^2\left(\frac{Z_D}{Z_0}-1\right)} & \frac{1-C^2}{1+C^2\left(\frac{Z_D}{Z_0}-1\right)} \end{bmatrix} \tag{2}$$

Once balun impedance transformation ratio Z_D/Z_0 is determined, S_{21} and S_{31} parameters can assume the maximum theoretical value for three-port passive networks (i.e., $1/\sqrt{2}$), provided that the optimum coupling factor C is chosen according to the following expression [24]:

$$C = \frac{1}{\sqrt{\frac{Z_D}{Z_0}+1}} \tag{3}$$

For this reason, different design techniques have been developed to increase the coupling factor: contributions can be found adopting a spiral shaping [13] or three-conductor approaches [25–27]. Reference [28] presents a generalized solution for multi-conductor Marchand-like baluns and illustrates how to reduce a multi-conductor symmetrical coupled line section to a single asymmetrical section.

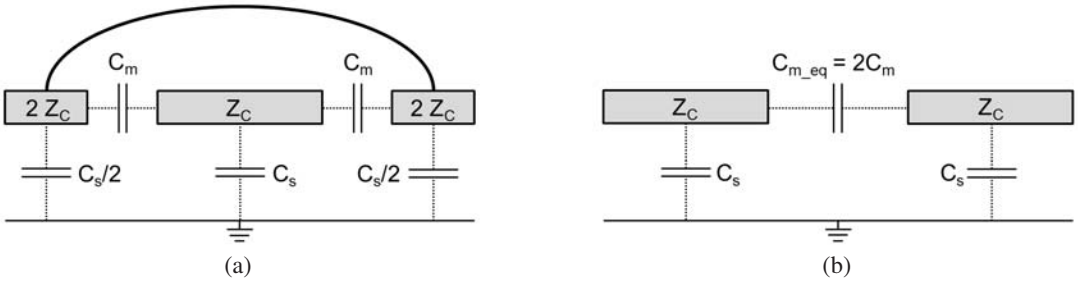

Figure 7. (a) Asymmetrical coupled line section and (b) equivalent symmetrical section.

In this contribution, a pretty different design strategy is adopted, based on a three-conductors asymmetrical coupled line section. More in detail, the characteristic impedance of external lines is chosen to be twice the impedance of the central line. Once the outer lines are properly connected (ideally short-circuited) at both ends of the lines, they become topologically equivalent to a single transmission line section, featured by halved characteristic impedance. The resulting structure is therefore completely identical to a symmetrical coupled line section with increased coupling factor, as clearly depicted in Fig. 7. This allows maintaining the same theoretical analysis as in [24].

From [29], the coupling coefficient of Fig. 7(b) can be written as a function of single lines ground capacitance and line-to-line mutual capacitance:

$$C = \frac{Cm_{eq}}{\sqrt{(C_S + Cm_{eq})\,(C_S + Cm_{eq})}} = \frac{2Cm}{C_S + 2Cm} \tag{4}$$

Substituting Eq. (3) into Eq. (2), the optimum value of mutual capacitance (determined, in the first approximation, by the distance between adjacent coupled lines) can be finally inferred:

$$C_m = \frac{C_s}{2\left(\sqrt{\frac{Z_D}{Z_0} + 1} - 1\right)} \tag{5}$$

The last step in balun design consists in replacing typical ground connections, on secondary conductors, by means of open-ended stubs which provide proper line termination at centre frequency, while preventing low-frequency IF signal, generated into the mixer core, to be loaded by the RF balun low impedance. Finally, a short circuited stub is inserted at the un-balanced port in order to compensate for micro-bonding inductance. Schematic depiction of the complete RF three-conductors balun can be found in Fig. 8, while reference [30] provides a more detailed balun analysis with measurements comparison on a dedicated test cell.

3.5. IF Section

As already explained in a earlier section, sub-harmonic ring mixer needs additional circuitry at IF section that has to simultaneously perform:

1. Single-ended to balanced transformation
2. IF port impedance transformation

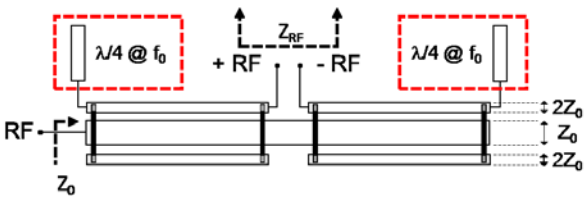

Figure 8. RF three-conductors balun.

3. Mixing core ground reference

Unlike LO and RF ports, IF interface cannot be implemented in a distributed manner, as a consequence of its lower operating band. In this case, a high pass/low pass filtering section is employed to produce the required 180° signal shift, according to the following design formulae:

$$\begin{aligned} L_1 &= \frac{Z_C \sin\left(\frac{\phi}{2}\right)}{\omega\left(1-\cos\left(\frac{\phi}{2}\right)\right)} \\ C_1 &= \frac{1}{\omega Z_C \sin\left(\frac{\phi}{2}\right)} \\ L_2 &= \frac{Z_C \sin\left(\frac{\phi}{2}\right)}{\omega} \\ C_2 &= \frac{1-\cos\left(\frac{\phi}{2}\right)}{\omega Z_C \sin\left(\frac{\phi}{2}\right)} \end{aligned} \tag{6}$$

High-pass and low-pass branches respectively synthesize +90 and −90 phase shifts, so that they can be easily exploited in order to perform a quarter wavelength transformation; more in detail, characteristic impedance Z_C in Equations (6) is chosen to match an external impedance twice Z_0 (100 Ohm): once two branches are joined at the un-balanced port, they finally perform the correct impedance transformation. Note that "pi" section arrangement is specifically selected in order to exploit high pass shunt inductors to provide 0 V bias reference to the mixer core, as clearly reported in Fig. 9.

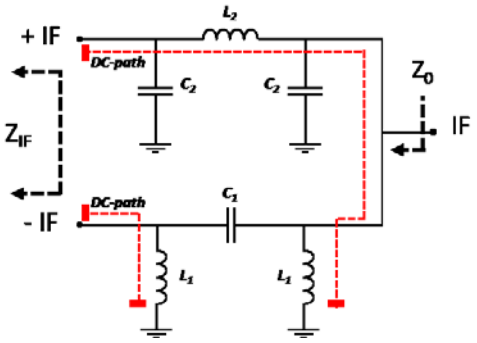

Figure 9. IF lumped balun.

4. EXPERIMENTAL RESULTS

Realized SHM results in a really integrated and compact MMIC, with an area occupation of only $2.4 \times 2.4\,\text{mm}^2$. A chip photograph is shown in Fig. 10, where LO, RF and IF ports are respectively visible on the lower, left and right borders of the chip. The remaining upper border was populated with DC bias pad for buffer DC supply. Looking at the figure below, mixer can be recognized on the upper portion of the die, the lower one being occupied by self biased feedback amplifier, acting as LO buffer stage.

The realized circuit was successfully tested in five operating bands: 43.5–44.5 GHz (LO=18 GHz), 44.5–46 GHz (LO=18.75 GHz), 46–47.5 GHz (LO=19.5 GHz), 47.5–49 GHz (LO=20.25 GHz), 49–50 GHz (LO=21 GHz). Circuit exhibits a typical conversion loss of 12 dB as reported in Fig. 11 showing, at the same time, good linearity performance, as the IIP3 plot, depicted in Fig. 12. Simulations show a pretty good agreement with experimental data excepted for the fifth RF band (LO=21 GHz) where some little mismatch in LO interface causes a slight increase in conversion loss.

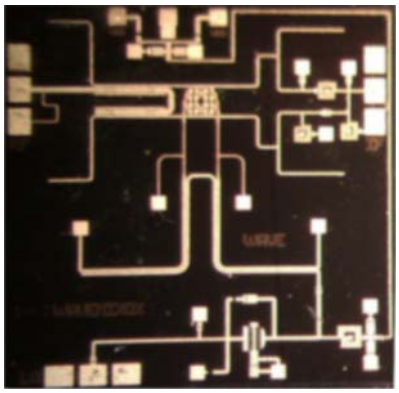

Figure 10. MMIC photograph.

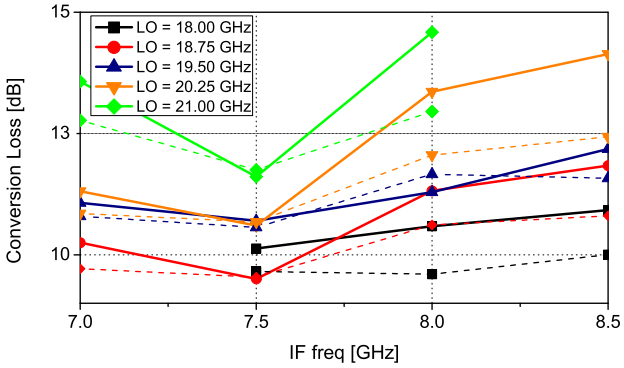

Figure 11. Mixer simulated (dashed lines) and measured (solid lines) conversion loss.

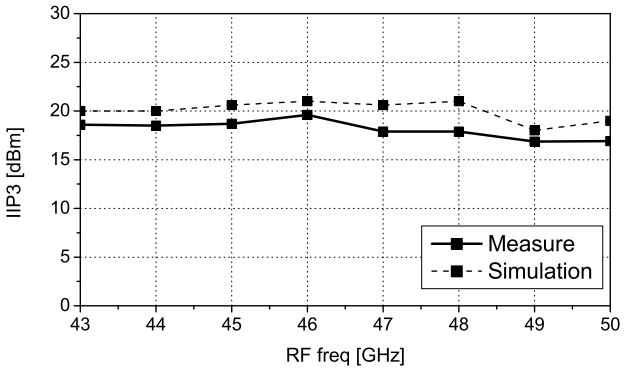

Figure 12. Mixer simulated (dashed line) and measured (solid line) IIP3.

The proposed SHM was designed to operate on a wire-bonded test jig but actually measured on wafer: this is the reason that RF port matching, reported in Fig. 13, suffers from some worsening with respect to ideal operating condition. On the other hand, IF port matching is not affected by the same phenomenon, as can be noted from Fig. 14, due to its lower operating frequency. Again simulation and measurement show a pretty good accordance, except for the extreme upper portion of the band where a little worsening is attributable to a not perfect simulation of the LO interface: such uncertainty causes a slight error in the prediction of mixer core differential impedances. The choice of a double-balanced mixer topology proved to be necessary to obtain high port isolation: LO to IF and RF to IF isolation

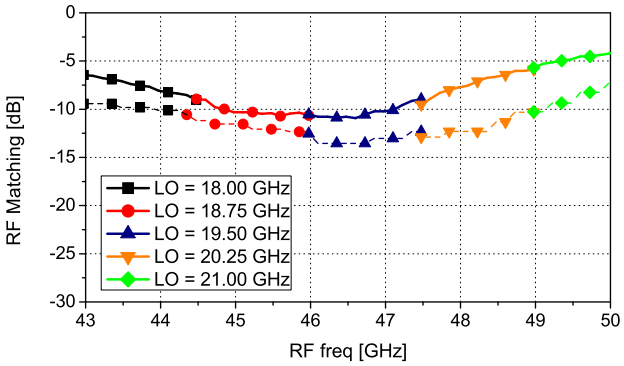

Figure 13. Mixer simulated (dashed lines) and measured (solid lines) RF port matching.

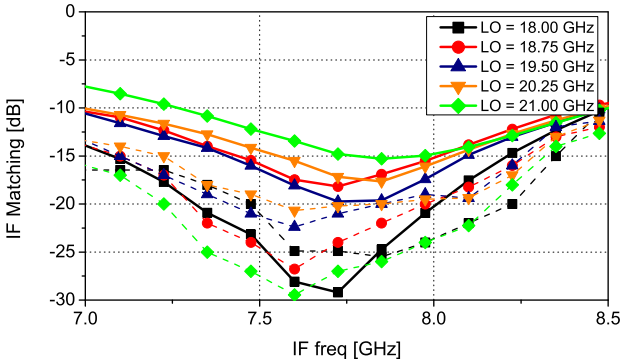

Figure 14. Mixer simulated (dashed lines) and measured (solid lines) IF port matching.

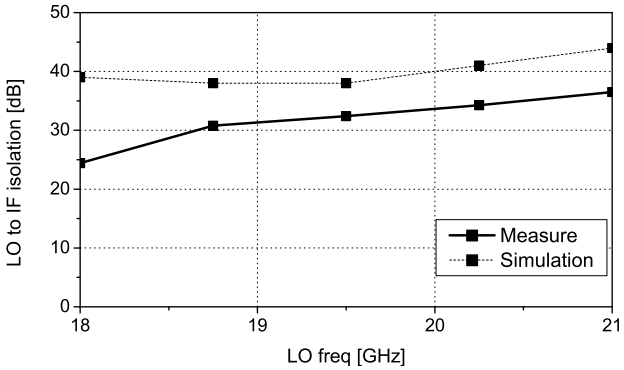

Figure 15. Mixer simulated (dashed line) and measured (solid line) LO to IF isolation.

are respectively higher than 25 dB and 30 dB (see Fig. 15 and 16). Also in this case, experimental data confirm circuit CAD prediction with a narrow confidence margin; for the RF to IF isolation, measurements are even better than simulations probably as effect of the reduced conversion gain at higher frequencies.

Effectiveness of the proposed design approach is further demonstrated by the summary Table 1, which compares the results of the present work with other recent SHM designs on similar bandwidths. As can be noted, the present circuit exhibits conversion gain and isolation results that are in line with other designs of similar technologies. Furthermore, implementation of the buffer amplifier guarantees the highest level of IIP3 together with the lowest value in terms of required pump power level. This is a fundamental achievement for a circuit designed to be featured by a low-frequency and low-power LO interface.

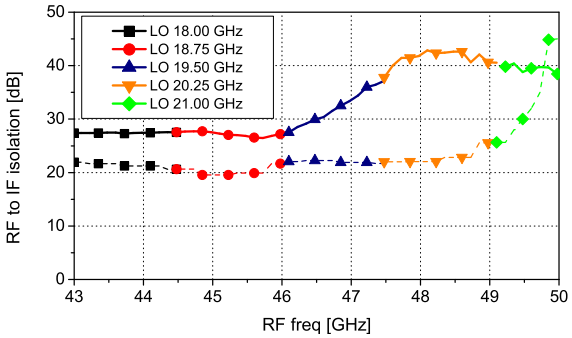

Figure 16. Mixer simulated (dashed lines) and measured (solid lines) RF to IF isolation.

Table 1. Comparison with previously published SHMs.

Reference	Technology	f_{RF} [GHz]	C.G. [dB]	P_{LO} [dBm]	LO/IF iso [dB]	RF/IF iso [dB]	IIP3 [dBm]	Size [mm^2]
12	CMOS 90 nm	33–103	−2.5	10	23	28	9	0.7×0.7
13	GaAs pHEMT 250 nm	47–50	−9	10	40	—	18	2.4×2.4
16	CMOS 90 nm	20–40	−11	10.5	20	35	9	0.9×1.0
17	GaAs pHEMT 150 nm	80–120	−13	10	—	—	—	1.4×1.4
18	GaAs mHEMT 130 nm	20–22	−9.4	7	35	—	—	2.3×1.7
26	GaAs pHEMT 150 nm	37–85	−12	10	35	30	13	0.8×0.8
27	GaAs mHEMT 130 nm	27–30	−9.5	10	48	—	—	2.3×1.7
This Work	GaAs pHEMT 250 nm	43–50	−12	7	25	28	18	2.4×2.4

5. CONCLUSION

Broadband satellite communications have become an attractive research topic, as a consequence of increasing number of the high data-rate digital services involved. As a key element in the realization of EHF receivers, millimeter wave mixers play a fundamental role in modern satellite links implementation. In the present contribution, the design flow of a EHF MMIC mixer, enabling the realization of compact and low-power consuming communication payloads, has been illustrated: the proposed architecture embeds a double balanced sub-harmonic mixing core, which allows for LO signal frequency halving, and a single stage LO buffer amplifier which guarantee low conversion loss and high linearity performance.

Although the proposed mixer moves from a traditional sub-harmonic strategy, manifold improvements have been implemented, in particular regarding the LO/RF/IF port definition; the design of the interfaces has been addressed in a methodical way thus avoiding any sub-optimal or redundant realization: the presented design technique actually provides the minimum set of passive networks realizing the mandatory biasing, matching and balancing functionalities. MMIC design flow has also been illustrated parametrically, in order to be practically adopted in the design of similar subsystems; furthermore, closed-form design expressions have been introduced, thus allowing easily prototyping an asymmetrical multiple conductor balun. Effectiveness of the new design approach has been proved experimentally: the fabricated mixer exhibits a really compact layout ($2.4 \times 2.4\,\text{mm}^2$), featuring 12 dB typical conversion loss and almost 20 dBm IIP3; double balanced ring topology ensures 25 dB worst case port isolation. Overall DC power consumption is about 250 mW but can be easily lowered to 150 mW.

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