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A 1.8–2.8 GHz Highly Linear Broadband Power Amplifier for LTE-A Application

Chun-Qing Chen, Ming-Li Hao, Zhi-Qiang Li, Ze-Bao Du, and Hao Yang*

Abstract—This paper proposes a fully integrated broadband power amplifier for LTE-A application using GaAs HBT process. To improve the linearity and broadband performance, RC feedback structures and dynamic bias circuits are employed and designed through optimization. With careful design of the broadband matching networks in the proposed 3-stage power amplifier topology, a power gain above 21.6 dB is achieved from 1.8 GHz to 2.8 GHz. Driven by an 80 MHz wideband LTE-A signal with PAPR of 7.5 dB, the designed RF power amplifier achieves an average output power about 22 dBm at ACLR = −30 dBc over the entire 1 GHz frequency band. Considering the broad bandwidth of the driven signal and wide frequency coverage bandwidth, the performance merits of the proposed design compare favorably with the state-of-the-art.

1. INTRODUCTION

LTE-advanced (LTE-A) has fulfilled the requirements of the 4G standards made by ITU with the help of Carrier Aggregation (CA) and high modulation density up to 64QAM. CA is one of the most important features of LTE-A, enabling an overall bandwidth of 100 MHz and a high data rate up to 1 GBit/s by aggregating up to five LTE carriers, each of 20 MHz bandwidth [1]. A power amplifier is one of the most important components, for its performance directly influences the overall system bandwidth, linearity, output power and efficiency. The increase of the signal bandwidth and peak-to-average power ratio (PAPR) in LTE-A demands a higher linearity in power amplifiers design.

In base stations, the final stage output power amplifier often employs GaN transistors together with a digital pre-distortion (DPD) system to achieve enough output power and linearity. Along with CA, the broad bandwidth and high PAPR of the modulated signals will force the components of the base-station to work in a back-off state to get enough linearity. Therefore an extra drive stage is often needed to pre-amplify the RF signals before sending them to the final output stage. For the drive stage power amplifier, a broadband and linear fully integrated chip is a good solution that offers enough power gain with low cost. Different from the final stage power amplifiers, the bandwidth and linearity requirements of the drive stage PA are more important than efficiency.

Recently, many fully integrated PA chips have been designed for the LTE-A application. CMOS process has a high level of integration and low cost, and some CMOS-based PAs have been reported for LTE-A [2–4]. However, CMOS suffers from low breakdown voltage and substrate loss, resulting into relatively low output power and poor linearity. So far, GaAs is still the most mature process for medium-power PAs with good linearity. Doherty structure is suitable for the back-off power application, and a broadband MMIC Doherty PA has been designed, covering the 1.6∼2.1 GHz frequency range [5]. Another MMIC PA is proposed in [6] which is designed in GaAs pHEMT process and operates from 2 to 6.5 GHz. In [7], a class-J PA is realized using GaAs HBTs and optimized for the LTE application

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* Corresponding author: Hao Yang (yanghao@ime.ac.cn).

The authors are with the Institute of Microelectronics of Chinese Academy of Sciences, Beijing Key Laboratory of Radio Frequency IC Technology for Next Generation Communications, Beijing 100029, China.

from 1.7 to 2.05 GHz. The aforementioned works have proven the advantages of the GaAs process over CMOS for the fully integrated PAs in LTE applications. However, none of them evaluated the influence of the broadband signals aggregated by several 20 MHz carriers.

In this paper, a fully integrated PA using GaAs HBT process is proposed and tested under an 80 MHz broadband signal aggregated by four 20 MHz wideband carriers from 1.8 GHz to 2.8 GHz. This design employs an equalizer in the input matching network to balance the power gain and several optimized dynamic bias circuits along with *R-C* feedback structures to improve the linearity. This paper is organized as follows. Section 2 describes the topology of the proposed PA and specific design considerations, including the linearity optimization of the bias circuits and the broadband design of the matching networks. The experimental results, including the measured results under small signals, continuous-wave and modulated signals, are reported in Section 3, followed by the conclusion in Section 4.

2. CIRCUIT DESIGN

High linearity and broadband frequency coverage are two main design goals in this paper. In order to meet the strict adjacent channel leakage ratio (ACLR) requirements of LTE-A, several efforts are made to achieve enough linearity . The general topology of the proposed broadband PA is shown in Figure 1. *R-C* feedback structures are inserted between the output and the input of the power stages to increase the linearity and relieve the stress of broadband matching over 1.8 GHz to 2.8 GHz. To compensate the gain loss caused by *R-C* feedback networks, a 3-stage cascade structure is used with emitter area ratio of $1 : 2 : 4$. This guarantees enough linear space for the first two drive stages, but with the sacrifice of low efficiency.

When the bandwidth of the signal increases using the carrier aggregation technique, the ACLR will also degenerate quickly. This is due to the fact that the third- and the fifth-order intermodulation components of the PA will affect the ACLR directly [8]. In the situation of n-subcarrier two tone test, the ACLR and third-order intermodulation distortion (IMD3) have a relation as [9]

$$\mathrm{ACLR}_n = \mathrm{IMD3} + C_n \tag{1}$$

where C_n is a correction factor relating to the number of sub-carriers. A low IMD3 value can still effectively reflect a good ACLR of the RF PA, even though the relationship would be much more complex for the CA operation. During the simulation in this design, IMD3 is one of the most important metrics to evaluate the linear performance of the power amplifier and to optimize the values of the components in bias circuits and matching networks.

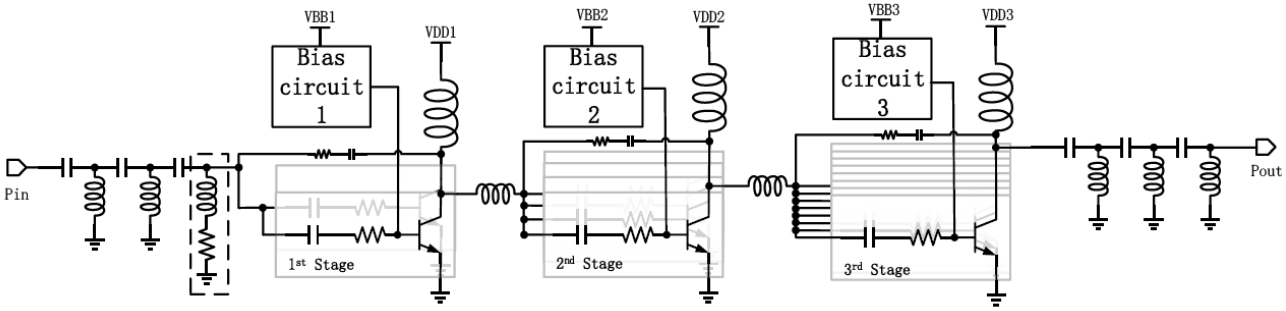
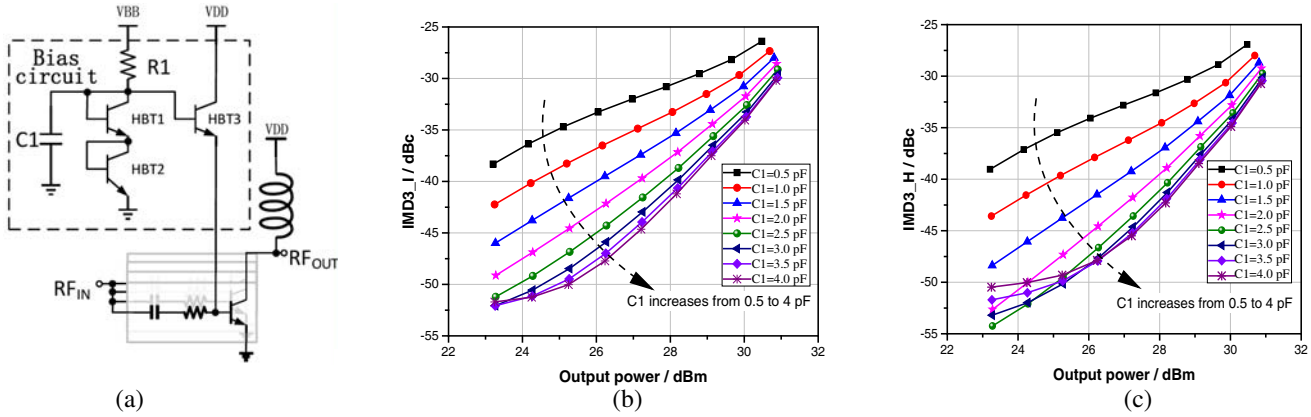


Figure 1. The structure of the proposed 3-stage broadband power amplifier.

The bias circuit should be designed first, because it determines the working state and the basic performance of the whole power amplifier. Dynamic biasing structures are preferred to enhance the linear performance of a HBT PA, for the base bias voltage of the PA will decrease along with the increase of the input power [10]. The employed bias circuit structure is shown in Figure 2(a). The diode-connected HBT1 and HBT2 offer the biasing voltage for the base of HBT3. C_1 is connected to the base of HBT3 and shorts the leaking RF signals. Therefore the voltage at the base of HBT3 will keep

stable when the increased input RF power leaks to the bias circuit. The rectified signal to bias circuit will also cause the voltage drop between the base and emitter of the HBT3, which will compensate the voltage drop of power stage under biasing. To get best linearity under the broadband LTE-A signals, the 1st and 2nd stage are biased near the class-A mode and the 3rd power stage is biased near the class-AB mode. Because this design is used as the drive stage power amplifier in the base station, the sacrifice of certain power efficiency for the higher linearity performance is acceptable.

During the optimization of bias circuits, the value of C_1 is found to affect the linearity of the whole PA. Figure 2 gives the simulated IMD3 of the whole 3-stage PA for different values of C_1. The two-tone test is taken with the tone spacing of 20 MHz centered at 2.3 GHz. When the value of C_1 increases from 0.5 pF to 2.5 pF, the improvement of both the lower and higher IMD3 is more than 10 dB for the output power below 28 dBm. However, when C_1 is bigger than 2.5 pF, the improvement in IMD3 is limited and the size of C_1 makes it a big component in the layout. Therefore, C_1 of the bias circuit is chosen as 2.5 pF, achieving a good balance between the linearity improvement and chip size consumption.



(a) (b) (c)

Figure 2. The structure of dynamic bias circuit (a) and simulated results of lower (b) and higher (c) value of IMD3 with two-tone test at 2.3 GHz under different C_1 values.

To fulfill the high linearity requirements over the entire frequency range of 1.8 GHz∼2.8 GHz, each stage should be carefully designed with both the dynamic bias circuits and *R-C* feedback networks connected. The power loss due to *R-C* feedback networks is determined by the value of the feedback resistor R_f [11], and the feedback capacitor C_f is mainly used to block the DC signals. To get enough drive gain, the R_f is set as 500 Ω with a C_f of 2.7 pF for each stage. Simulation results show that the power loss due to the *R-C* feedback is about 1dB. The *R-C* feedback structure in this work is found to be more effective in increasing the stability than increasing the bandwidth. To fulfill the high linearity requirements from 1.8 GHz to 2.8 GHz, matching networks play an important role. The main strategy in designing matching networks is to determine the optimal load impedance for each stage first, then optimize the matching network for each stage and then connect the three stages one by one to finish the whole design.

To find the optimal load impedance of each stage, three load-pull simulations have been carried out at 1.8 GHz, 2.3 GHz and 2.7 GHz, respectively. We first do the conjugate input matching for each stage, then sweep the load impedance and simulate the $P_{1\,\mathrm{dB}}$ point for every load impedance. Figure 3 shows the optimal load impedance region at different frequencies for the 3 stages when the $P_{1\,\mathrm{dB}}$ is good enough. As shown in Figure 3, when the frequency increases, the imaginary part of the optimal impedance decreases and real part shares a certain common region. The optimal load impedance of the 3rd stage is located in a narrower region, compared with the other two stages, as shown in Figure 3(c), which means the performance of the 3rd stage is more sensitive to the variation of the output matching network.

Knowing the optimal load impedance for each stage, the broadband matching network design is started from the 3rd power stage. To convert 50 Ω to the optimal impedance at 1.8 GHz, 2.3 GHz and

2.8 GHz simultaneously, three high pass sections are used as the output matching network, as shown in Figure 1. The determination of the values of the matching elements is done through optimization and thus is not detailed here. Then design the middle stage matching network to cover the optimal load impedance of the 2nd and 1st stage in turn. The middle stage matching network should be designed as simple as possible to reduce both the gain loss and layout consumption. As shown in Figure 1, the middle stage matching network is realized using a single inductor along with carefully designed choke inductors, which is realized by bonding wires and lump inductors off the chip. While the output and middle stage matching networks guarantee the best output performance of each stage, the design of input matching network should focus on enhancing the gain flatness over the design frequency range of 1.8∼2.8 GHz. By designing the matching networks in such a reverse order, each stage can cover its optimal load impedance. The optimization of the entire circuit's performance can be done quickly by adjusting the values of the lumped components in the matching networks in a small region.

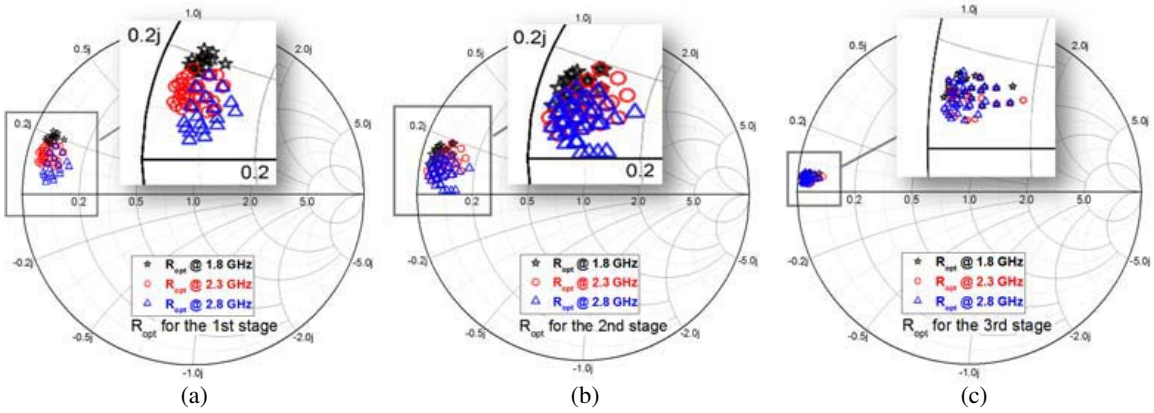


Figure 3. Simulated R_{opt} for each stage of PA.

To balance the gain in the design frequency range, an equalizer is necessary to suppress the gain in low frequency band. An L-R equalizer structure is employed in this design which is shown in a dashed rectangle in Figure 1. By tuning the values of L and R, the suppression can be adjusted for different frequency ranges and the simulated gain suppression is shown in Figure 4. The gain is suppressed by about 1.5 dB from 1.8 GHz to 2.5 GHz and less than 0.5 dB gain flatness improvement is observed.

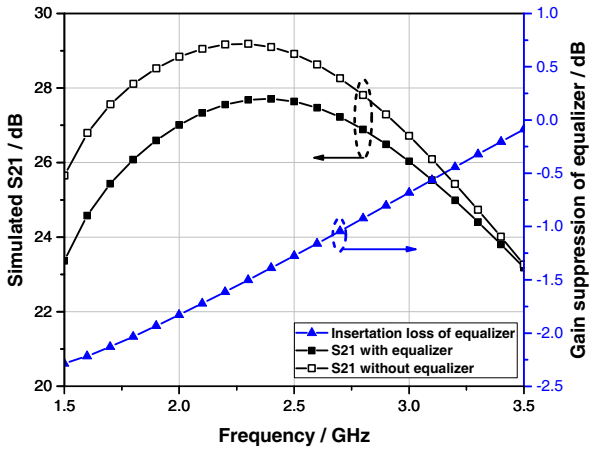


Figure 4. Simulated results for the equalizer of the input matching network.

3. EXPERIMENTAL RESULTS

The proposed PA is fabricated in a GaAs HBT process, within a chip size of 1.25 mm*1.25 mm including all the components. The chip photograph is illustrated in Figure 5 with all the matching networks integrated on chip. In measurement, the chip is glued on a Rogers substrate with supply voltage of VDD = 5 V and VBB = 2.7 V. To evaluate the performance of the designed broadband PA, the small signal test, single-tone test with continuous-wave (CW) signal, and modulated signals tests are performed respectively.

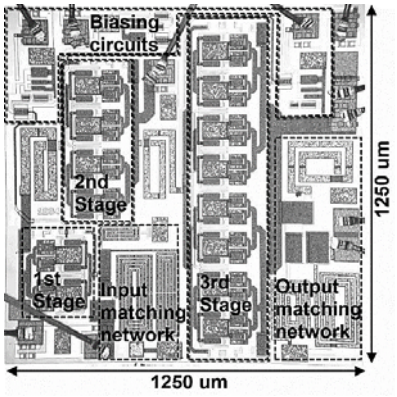


Figure 5. Die micro-photograph of the fabricated PA with a size of about 1.5 mm^2.

S-parameters are measured with an input power of −30 dBm and shown in Figure 6(a). The input and output are well matched with S_{11} and S_{22} near −10 dB from 1.8 GHz to 2.8 GHz. S_{21} is above 21.6 dB across the entire 1 GHz bandwidth. Compared with the simulated results (solid lines in Figure 6(a)), the gain degenerates obviously from 2.5 GHz to 2.8 GHz. The gain flatness can be further improved by tuning the values of the L-R equalizer. The measured Rollet's stability factor [12] (K-factor) is shown in Figure 6(b) with a value bigger than 3 from 0.5 GHz to 5 GHz which guarantees an unconditional stability of the design.

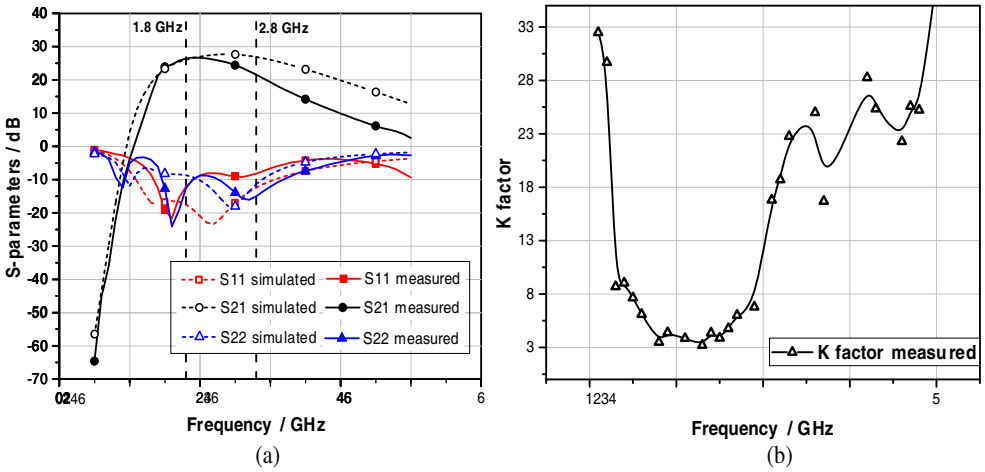


Figure 6. Measured S-parameters and K factor from 0.5 to 5 GHz.

Figure 7 shows the measured performance across 1.8∼2.8 GHz with the 80 MHz bandwidth 7.5 dB PAPR LTE-A signal. The PA delivers a PAE of 7.6%, a power gain of 25.6 dB and an ACPR of −26 dBc with an average output power of 25 dBm at a frequency of 2 GHz. To meet the linearity requirement with an 80 MHz bandwidth LTE-A signals, the careful design of RC feedback structure and output matching networks are far from enough. A large size power stage is chosen to offer enough power

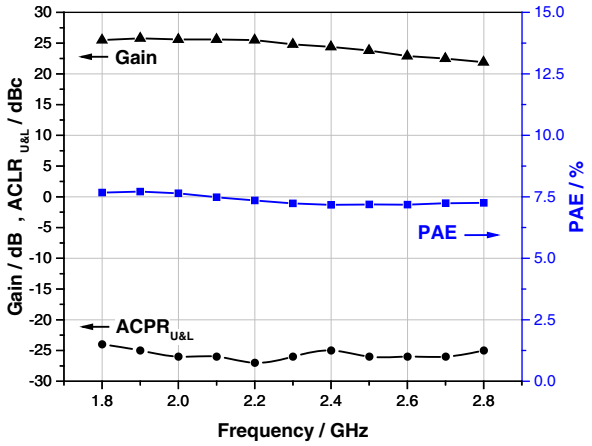


Figure 7. Measured PAE, power gain and ACPR at different frequencies when $P_{\text{out}} = 25\,\text{dBm}$.

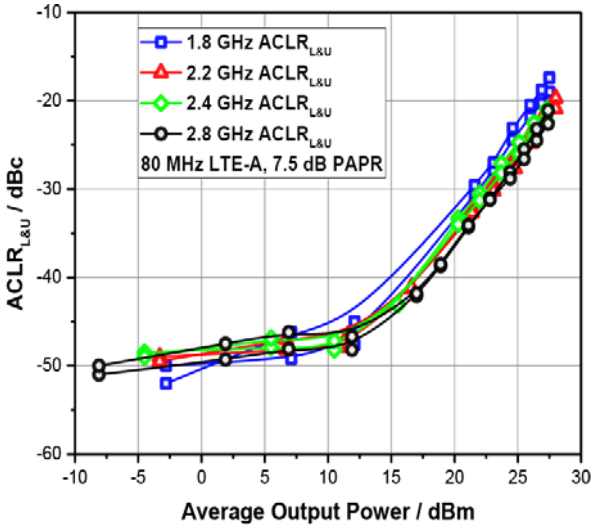


Figure 8. Measured ACLR at different frequencies with an 80 MHz wideband LTE-A signal.

back-off and all three stages of the PA are biased near the Class-A mode to improve the linearity in a traditional way. Consequently, the measured PAE will drop to 5.4%∼6.6% in 1.8∼2.8 GHz with an output power of 22 dBm when the ACPR is below −30 dBc. A best PAE of 13.3% is achieved when the output power is 27 dBm at 2 GHz.

To test the linearity performance of the designed fully integrated PA, an LTE-A signal composed of four 20 MHz LTE signals with a PAPR of 7.5 dB is applied to it, and the ACLR is measured at center frequencies of 1.8 GHz, 2.2 GHz, 2.4 GHz and 2.8 GHz respectively. Figure 8 shows the measured ACPR results versus average output power tested with 80 MHz BW 7.5 dB PAPR LTE-A signal. The lower and upper side ACPR of a certain frequency are plotted in the same color. As shown in Figure 8, even driven by an LTE-A signal with 80 MHz bandwidth, the output power is above 15 dBm when ACLR = −40 dBc and more than 22 dBm when ACLR = −30 dBc. Besides, the linearity performance is quite stable over the entire frequency range of 1.8 GHz to 2.8 GHz.

According to the best of the authors' knowledge, few fully integrated LTE power amplifiers have been reported that are tested under broadband signals up to 80 MHz using the CA technology that cover such a wide frequency range. Table 1 shows the performance of the proposed design, compared with the state-of-the-art fully integrated PAs for LTE applications. Considering the broadband input signal and the wideband frequency coverage, the proposed LTE-A PA achieves a favorable linearity performance.

Table 1. State-of-the-art fully integrated LTE PA.

Ref.	**[5] MTT 2011**	**[7] MTT 2015**	**[4] MTT 2015**	**[6] MWCL 2016**	**This Work**
Frequency/GHz	1.6–2.1	1.7–2.05	2.5	2–6.5	1.8–2.8
Psat/dBm	-	32	28.1	31–32.5	28
Signal	LTE	LTE	LTE-A	LTE	LTE-A
BW	10 MHz	20 MHz	60 MHz	20 MHz	80 MHz
PAPR/dB	7.5	7.6	10.26	8.66	7.5
Pavg/dBm	27.5	28	17.6	26	22
ACLR	−32	−30	−30	−30	−30
PAE/%	30∼36.3	40.5∼55.8	13.7	NC*	5.4∼6.1
Supply/V	4.5	3.3	2.5	5	5
Area/mm^2	1.96	0.86	1.8	9.6	1.56
Topology	Doherty	Class-J	Harm. Trap	-	-
Technology	GaAs HBT	GaAs HBT	SOI 180 nm	GaAs pHEMT	GaAs HBT

* Only the PAE for P_{sat} is mention in the paper.

4. CONCLUSION

This paper proposes a fully integrated LTE-A PA for wideband drive stage power amplifiers used in LTE-A base stations. Realized in GaAs HBT process, the designed PA achieves a power gain above 21.6 dB and saturate output power above 28 dBm in the entire frequency range of 1.8∼2.8 GHz. With carefully designed dynamic bias circuits and RC feedback structures, high linearity is achieved over a broad frequency range. The linearity performance is measured with an 80 MHz wideband input signal composed of four 20 MHz LTE signals. The average output power is above 22 dBm when ACLR = −30 dBc over the entire frequency range. The proposed broadband PA in this paper offers a positive example for the design of fully integrated power amplifiers for broadband LTE-A communication.

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