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Bandwidth Tuning in Transistor Embedded Metamaterials Using Variable Resistance

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Abstract—Metamaterials have been previously loaded with diodes and other types of passive circuit elements. Transistors offer an alternative to these established loading elements to expand the possible capabilities of metamaterials. With embedded transistors, additional degrees of freedom are achieved and lay out the architecture for more complex electromagnetic metamaterial design. A mathematical analysis of transistor loaded SRR unit cells is described in which the transistor acts as a variable resistor. From the mathematical analysis, we calculate transmission coefficients for a single unit cell. We then experimentally measure two SRRs with tunable quality factors and thus tunable bandwidth based upon modulating the effective loading circuit resistance to confirm the calculations. From the agreement between the calculated and measured transmission coefficients, we expand the analysis to show that a slab of more densely packed unit cells can achieve negative permeability with varying degrees of dispersion.

1. INTRODUCTION

Metamaterials have introduced a new method of creating effective artificial materials with various novel properties. Examples of these properties are negative permeability [1, 2], negative permittivity [3], and negative index of refraction [4, 5]. Correctly engineering and controlling these properties has yielded advances in cloaking [6], lensing [7, 8], and antenna design [9–11]. However, for all of these properties to be expressed in the manner required for the aforementioned applications, metamaterials need to be composed of resonant inclusions.

Resonant structures are inherently bandwidth and loss limited. To overcome the narrow bandwidth limitation, tunable RF metamaterials have been created by embedding diodes [12, 13], MEMS switches [14], and ferromagnetic elements [15, 16]. These are all passive components and are used to tune the value of the resonant frequency, with varying degrees of continuity. Tuning the resonant frequency value is only one type of tunability for a resonant structure. The resonance quality factor, which is determined from the bandwidth and loss of the resonator, can also be tuned to affect the frequency response of a metamaterial [17].

Transistors are three or four terminal devices (as opposed to the passive two-terminal devices such as diodes and capacitors) that have found applications in many aspects of circuits and systems as well as providing an alternative to the previously mentioned embedded devices. At the circuit level, transistors are used for amplication, oscillation generation, and switching, providing several crucial active functions in electronic circuits. However, transistors have only recently been embedded in metamaterials through simple circuits and applications [18–21].

The extra terminals provide more control over the characteristics of the unit cell, providing the additional possibility for tuning the bandwidth. This work will highlight the physics of using a metal-oxide-semiconductor field effect transistor (MOSFET) for tuning both the resonant frequency

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and resonance bandwidth, helping set the foundation for future applications of transistor embedded metamaterials. Design of metamaterials with a tunable quality factor allows for the creation of a metamaterial that can be configured through bandwidth modulation as well as resonant frequency modulation.

This work demonstrates how to create a metamaterial with a tunable bandwidth that utilizes a transistor as a variable linear resistor. Section 2 will review the important physics of passive elements and transistors that will allow for the constructing such a metamaterial. Section 3 will apply the developed physical models to describe a metamaterial with a variable bandwidth followed by experimental characterization. The final section will explain how to modify the transistor's configuration within the SRR in order to achieve minimal resonant frequency change while tuning the bandwidth by utilizing a different tunable element within the structure of the transistor.

2. METHOD OF QUALITY FACTOR TUNING

To design and quantify a resonant circuit, a mathematical quantity must be derived that accurately describes the bandwidth (shape) of the resonance. An important figure of merit for any passive or resonant element is its quality factor (Q). Q is numerically defined as the ratio of stored energy to dissipated energy (Eq. (1)) [22, 23].

$$Q = \omega \frac{W_{\text{stored}}}{P_{\text{dissipated}}} \tag{1}$$

For large values of Q, the element acts more like an ideal energy storage element and for small values of Q, the element is effectively an attenuator (or resistor). High Q elements and resonators are not always the best types of inclusions for every application, but being able to quantify the ideality of passive components is important for the characterization of a system.

A simple passive SRR can be reduced to a series RLC circuit for the purposes of metamaterial design [1]. Based upon the effective circuit parameters of such a SRR, the values of Q for the circuit equivalent series inductor and capacitor are calculated using Eqs. (2) and (3).

$$Q_c = \frac{1}{\omega C R} \tag{2}$$

$$Q_l = \frac{\omega L}{R} \tag{3}$$

The Q of the series RLC circuit at the resonant frequency is then determined by substituting ω_0 in place of ω and solving for either Q_l or Q_c.

$$Q = \frac{\omega_0 L}{R} = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{4}$$

From Eq. (4), the simplest method to vary Q while maintaining constant ω_0 is to tune the loop series resistance R (both L and C can also be used to tune Q but the LC product must remain constant). The structure of a transistor includes several different tunable elements, including a tunable resistor located between the drain and source terminals. This is the element that will be exploited to create a metamaterial with a tunable quality factor.

MOSFETs have 3 regions of operation: cutoff (or subthreshold), linear, and saturation. All regions of operation provide a tunable resistance, but the mechanism and range of resistance values is slightly different in each region. To define the operating regions, the threshold voltage (V_T) must be defined. In this work, V_T is defined as the bias required to attract enough electrons to create the inverted channel (the concentration of electrons in the channel is equal to the concentration of holes in the bulk away from the gate oxide). In cutoff, the gate to source voltage (V_{GS}) is less than the threshold voltage ($V_{GS} < V_T$). Under this bias condition, the conducting channel is not fully present but there is a small current can still flow from drain to source if another voltage is applied across those two terminals.

The I_{DS} current equation in the cutoff region is as follows in Eq. (5) [24] (the primary parameters to focus on are V_{GS}, V_T, and V_{DS} as the rest are constants determined from the physical semiconductor).

$$I_{DS} = k' \frac{W}{L}(m-1)\left(\frac{k_B T}{q}\right)^2 e^{q(V_{GS}-V_T)/mk_BT}(1 - e^{-qV_{DS}/k_BT}) \tag{5}$$

I_{DS} is not solely dependent on a single voltage, unlike current flowing a diode, but rather two voltages. V_{DS} dictates the current in a reverse bias diode-like equation while the application of V_{GS} pulls extra conducting electrons to the surface in the bulk, partially forming a conducting channel.

The second bias region for a MOSFET is the linear region. When V_{GS} is raised to voltages greater than V_T, the conducting channel is fully formed and allows for significant current flow from drain to source in the device. The current generated from the reverse biased junction becomes negligible compared with the current that flows through the channel and changes the current-voltage characteristic (Eq. (6) [25–27]).

$$I_{DS} = k' \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{6}$$

I_{DS} in this region becomes linearly related to V_{GS} and quadratically related to V_{DS}, a stark contrast compared with the exponential relationships from the current equation for the cutoff region (Eq. (5)). If V_{DS} is kept small, there is an increase in linearity between the current and voltage. The control of I_{DS} with V_{GS} in the cutoff and linear regions with respect to creating a tunable resistance will be looked at in Section 3.

If V_{DS} is increased to $V_{GS} - V_T$, the conducting channel becomes "pinched-off." When the channel is pinched-off, the MOSFET reaches the saturation operating region. The current-voltage characteristic changes from Eq. (6) to Eq. (7) [25–27] (again, V_{GS}, V_T, and V_{DS} are the primary parameters to focus on to understand the transistor behavior).

$$I_{DS} = \frac{k'}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \tag{7}$$

Once a MOSFET is in saturation, the current flow becomes nearly constant with increasing V_{DS} since pinching off the conducting channel restricts the concentration of carriers. I_{DS} does increase with V_{DS} due to the channel length modulation effect, but the rate of change is much smaller than in the linear region.

A transistor biased in such a way to isolate the drain, source, and gate terminals appears as several linear elements (Fig. 1). For this application, the transistor will be embedded in the SRR such that the RF current will flow between the drain and source. This configuration will result in the transistor effectively becoming a parallel combination of a resistor and capacitor. The total drain-to-source capacitance (C_{ds}) is a combination of the structure capacitances (Eq. (8)) and will not appreciably change as V_{GS} is tuned.

$$C_{ds} = C_{db} + \frac{C_{gd} C_{gs}}{C_{gd} + C_{gs}} \approx C_{db} \tag{8}$$

Most commercial transistors are asymmetric, typically resulting in $C_{gs} \gg C_{gd}$. Assuming this relationship of the transistor asymmetry, the series combination of C_{gs} and C_{gd} is dominated by C_{gd}. In most FETs, $C_{ds} \gg C_{gd}$ effectively rendering the combination C_{gs} and C_{gd} negligible, leaving the total effective capacitance approximately equal to C_{ds}.

The other primary current pathway between the drain and source is the parallel combination of g_{ds} and voltage controlled current source (VCCS). If V_{GS} is solely a DC voltage, the VCCS current is zero resulting in g_{ds} as the only other current path. Increasing g_{ds} will shunt current away the capacitor,

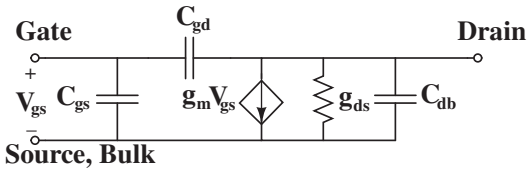

Figure 1. Simplified small signal equivalent circuit of a MOSFET. This model assumes that the bulk and source are tied together while the drain, gate, and source resistances and inductances will have a negligible effect to the eventual total resistance and inductance of the circuit (the SRR loop plus effective transistor g_{ds}).

changing the quality factor of C_{ds}. Taking the partial derivative of Eq. (5) with respect to V_{DS}, the effective g_{ds} for the transistor under subthreshold conditions is obtained.

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = k' \frac{W}{L}(m-1)\left(\frac{k_B T}{q}\right) e^{\frac{q(V_{GS}-V_T-mV_{DS})}{mk_B T}} \tag{9}$$

An important feature within Eq. (9) is that the change in conductance becomes very rapid. When V_{GS} is increased to near V_T, the conducting channel between is nearly formed and the Q of the effective capacitor is very small compared to a physical lumped capacitor. At the bias point $V_{GS} \geq V_T$, the conducting channel between the drain and source is fully present and the embedded transistor's effective operating region switches from subthreshold to linear.

In the linear region, the transconductance term g_m still remains near zero meaning the g_{ds} element will still be the primary resistive current carrying element. In the linear region, if V_{DS} is small, the quadratic term in Eq. (6) becomes negligible (Eq. (10)).

$$I_{DS} = k' \frac{W}{L}(V_{GS} - V_T)V_{DS} \tag{10}$$

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = k' \frac{W}{L}(V_{GS} - V_T) \tag{11}$$

Eq. (10) demonstrates a current characteristic similar to that of a resistor since I_{DS} and V_{DS} are linearly proportional. By increasing V_{GS}, nearly all the RF current will be shunted away from the capacitor, reducing the effect that C_{ds} will have on the circuit. However, at a certain voltage, the insulating oxide will begin to break down due to the large electric field across the gate oxide, destroying the variable resistor effect. As the oxide will no longer be isolating the gate and bulk, there will not be a potential difference between the gate and bulk, thus eliminating the electric field generated from the gate to the bulk and physically destroying the transistor.

V_{DS} can be made non-zero to bias the transistor in the saturation region but will make g_{ds} very small.

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{1}{2}\lambda k' \frac{W}{L}(V_{GS} - V_T)^2 \tag{12}$$

Even with the square dependence on $V_{GS} - V_T$, the current does not appreciably change with V_{DS}. With the slope of the current nearly flat, the effective conductance reduces to something similiar in magnitude to the cutoff/subthreshold conductance where most of the small signal current flows through the capacitor. The VCCS then becomes the tunable element of interest, but is only tunable if the gate-to-source voltage is a small signal RF voltage and not only a DC voltage. Using the VCCS as a tunable element embedded in a metamaterial is discussed in Section 4.

With the current-voltage relationships known and that the necessary equations to calculate effective conductances having been derived, the effective conductance (and therefore resistance) of the transistor can be extracted from the $I_{DS} - V_{DS}$ curves. Using a BSS83 n-channel transistor, $I_{DS} - V_{DS}$ curves were measured (Fig. 2). Examining near the origin, the curves become linear and the slopes can be calculated. The slope is the effective conductance, which is inverted to obtain the RF drain-to-source resistance

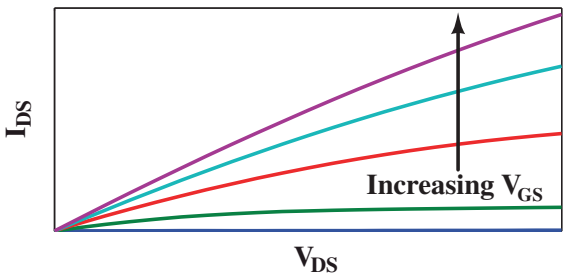

Figure 2. $I_{DS} - V_{DS}$ characteristics for a n-channel transistor.

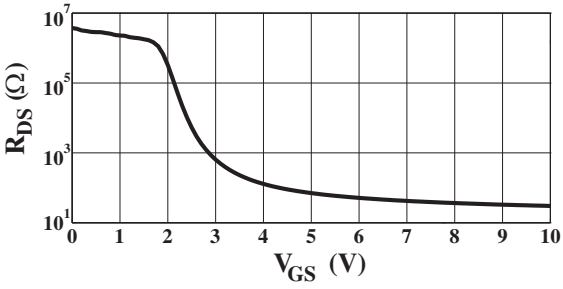

Figure 3. Extracted R_{DS} measurements for a BSS83 transistor configured as in Fig. 4.

(Fig. 3). The gate was directly connected to a DC control voltage while the source is connected to DC ground, creating the necessary V_{GS} to control the conductance of the channel between the drain and source. The drain is connected to the source by a resistor, which limits the minimum effective conductance (therefore determining the minimum loss of the capacitive structure) and sets the V_{DS} to zero. As expected, the resistance decreases exponentially in the cutoff region (consistent with Eq. (9)) and decreases much more gradually in the linear region (consistent with Eq. (11)).

3. ANALYSIS, SIMULATION, AND MEASUREMENT OF A SRR WITH TUNABLE *Q*

Starting with the equivalent circuit model of the transistor-embedded SRR, the analysis from Section 2 can be employed to determine the exact mathematical relationship between the circuit parameters and the quality factor. Eq. (4) can also be determined from the fact that the energy stored in the capacitor and inductor are equal at the resonant frequency [22]. Revisiting the initial definition of Q (Eq. (1)), the Q of the SRR equivalent circuit is determined through the summation of the stored energy in the capacitors and inductors (Eq. (13)) and the power dissipation caused by the resistors (Eq. (14)).

$$W_{\text{st}} = W_M + W_E = \frac{1}{4}|I_{L_M}|^2 L_M + \frac{1}{4}C_M|V_{C_M}|^2 + \frac{1}{4}C_t|V_{C_t}|^2 \tag{13}$$

$$P_{\text{dis}} = \frac{1}{2}|I_{R_M}|^2 R_M + \frac{1}{2}|I_{R_t}|^2 R_t \tag{14}$$

The voltage across transistor capacitance (V_{C_t}) is related to the current (I_{R_t}) flowing through the resistive path of the transistor (Eq. (15)) while the current through the resistor is related to the impedance of the capacitance and resistance (Eq. (16)).

$$V_{C_t} = I_{R_t} R_t \tag{15}$$

$$I_{R_t} = \frac{I_{L_M}}{j\omega C_t R_t + 1} \tag{16}$$

Using the fact that the stored electric and magnetic energy are equal at resonance [22] and $I_{R_M} = I_{L_M}$, Eq. (16) can be substituted into Eq. (14) to determine the Q of the transistor-embedded SRR equivalent circuit at resonance (Eq. (17)).

$$Q = \omega_0 \frac{2W_M}{P_{\text{dissipated}}} = \omega_0 \frac{\frac{1}{2}|I_{L_M}|^2 L}{\frac{1}{2}|I_{L_M}|^2 R_M + \frac{1}{2}|I_{L_M}|^2 R_t \frac{1}{|j\omega_0 C_t R_t|^2}} \tag{17}$$

Eq. (17) simplifies further to Eq. (18).

$$Q = \frac{\omega_0 L_M}{R_M + \dfrac{R_{ds}}{(\omega_0 C_{ds} R_{ds})^2 + 1}} \tag{18}$$

At the extreme positive values of the transistor resistance, the equation to derive Q simplifies to a form consistent with that of a normal passive SRR (Eq. (4)). Eq. (18) also allows for the analysis of the transistor-embedded SRR in bias regions such that the transistor resistance isn't either very large or very small.

The analysis of the equivalent circuit model is still not finished. Due to the dynamics of the incremental R_t, there will be a change in the resonant frequency. The above analysis used to derive an expression for Q did not explicitly require that ω_0 be already known. For the resonant system to be fully characterized, an expression relating ω_0 and the equivalent circuit parameters must be derived.

Using the basic definition of a resonance, the total reactance of the transistor-embedded equivalent circuit will sum to zero at ω_0. The total equivalent circuit impedance is calculated in Eq. (19).

$$Z = R_M + j\omega L_M - \frac{j}{\omega C_M} + \frac{R_t}{1 + j\omega C_t R_t} \tag{19}$$

The impedance calculation also simplifies to the basic series RLC impedance equation at the extreme values of R_t, yielding the maximum and minimum limits of the resonant frequency. The reactance calculation can be further simplified to Eq. (20).

$$X = \mathrm{Im}\{Z\} = \frac{\omega^4 L_M C_M C_{ds}^2 R_{ds}^2 + \omega^2 (L_M C_M - (C_{ds} R_{ds})^2 - C_M C_{ds} R_{ds}^2) - 1}{\omega C (1 + \omega^2 C_{ds}^2 R_{ds}^2)} \tag{20}$$

The reactance has poles at the zero frequency and two conjugate imaginary frequencies so the calculation of the reactance zeros can be done without running into higher order poles and zeros. Setting the numerator equal to zero and using a dummy variable to reduce the order of polynomial (set $x = \omega^2$), the resonant frequency is calculated from the effective circuit parameters using the quadratic formula (Eq. (21)).

$$x = \frac{(C_{ds} R_{ds})^2 + C_M (C_{ds} R_{ds}^2 - L_M)}{2 L_M C_M C_{ds}^2 R_{ds}^2} \pm \frac{\sqrt{[C_M (L_M - C_{ds} R_{ds}^2) - (C_{ds} R_{ds})^2]^2 + 4 L_M C_M C_{ds}^2 R_{ds}^2}}{2 L_M C_M C_{ds}^2 R_{ds}^2} \tag{21}$$

Taking the square root of x yields four possible solutions for the resonant frequency. Because all the effective circuit parameters are real valued and positive, only a single solution for ω is real and positive yielding a single valued resonant frequency.

Based upon Eqs. (18) and (19), a transistor-embedded SRR as configured in Fig. 4 can be fully analyzed mathematically. It is important to emphasize that the gate voltage is a DC quantity and that gate is effective isolated from the drain, source, and bulk to confirm that the system is passive and will not have issues typically associated active transistor circuits. Using the extracted effective circuit parameters of the transistor and SRR loop, the analytical dependence of the resonant frequency and resonance quality on the gate voltage can be plotted (Fig. 5).

When R_{ds} is very high (significantly greater than the transistor capacitance impedance), the resonance Q is higher than in other bias regions. Under the high resistance condition, most of the induced RF current flows through the transistor like an effective low-loss capacitor which adds near-zero resistive loss to loop. When the drain-to-source resistance is very low (significantly lower than the

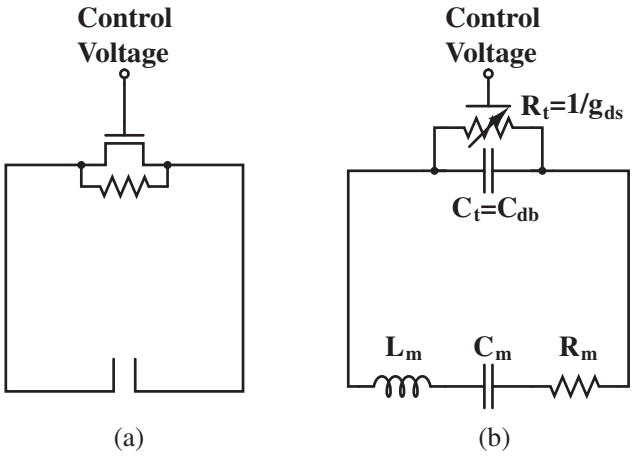

Figure 4. Diagram (a) and effective circuit equivalent (b) of a transistor embedded SRR. The transistor is embedded such that the gate is solely DC biased and RF current effectively only ows from drain to source. The FET bulk is tied to the source to avoid changes to the threshold voltage with a large-valued resistor connected across the source and drain to avoid hysteretic effects from the back-to-back junctions (DC bias network not shown).

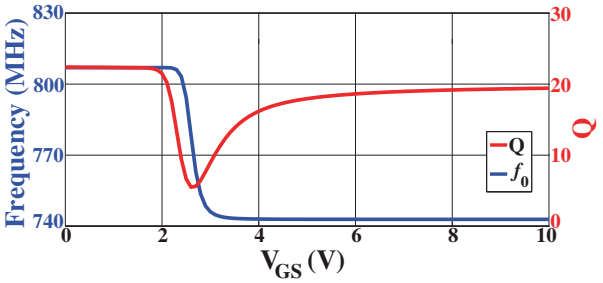

Figure 5. Calculated Q and f_0 for transistor-embedded SRR using estimated effective circuit parameters for the loop and transistor.

transistor capacitance impedance), the resonance quality starts to increase with an increase in V_{GS}. At this bias condition, the transistor resistance decreases, increasing Q (as expected from Eq. (4)). In the bias region when the drain-to-source resistance is roughly equivalent to the transistor capacitance impedance, the RF current is split approximately equally through the resistive and capacitive paths. Due to the large impedance across both paths (C_{DS} of the BSS83N is close to 1.5 pF, which yields an impedance magnitude of around 150 Ω at 750 MHz), the generated current is limited, decreasing the resonance quality and reducing the polarizability of the SRR.

Once the quality factor and resonant frequency of the effective circuit have been calculated, the effective permeability can then be determined [28] using Eq. (22) (F is defined as a geometry/fill factor related to the unit cell density).

$$\mu_r \approx 1 + \chi_m \approx 1 + \frac{F\omega^2}{\omega_0^2 - \omega^2 + \dfrac{j\omega\omega_0}{Q_{\text{circuit}}}} \tag{22}$$

$$F = \frac{\mu_0 A_{\text{loop}}^2}{V_{\text{cell}} L_{\text{loop}}} \tag{23}$$

From the effective μ_r calculation, the effective index of refraction ($n = \sqrt{\mu_r \epsilon_r}$), normalized impedance ($z = \sqrt{\mu_r/\epsilon_r}$), and transmission ($S_{21}$) and reflection ($S_{11}$) parameters can then be calculated (Fig. 7 and Eqs. (24) and (25)) [29] (since the SRR is a magnetic particle, ϵ_r is assumed to be 1).

$$S_{21}^{-1} = \left[\cos(nkd) - \frac{j}{2}\left(z + \frac{1}{z}\right)\sin(nkd)\right] e^{jkd} \tag{24}$$

$$S_{11} = -\frac{1}{2} j \left(z - \frac{1}{z}\right)\sin(nkd) S_{21} e^{jkd} \tag{25}$$

To experimentally confirm the calculated values derived from the effective circuit quality factor and other geometric factors, the transistor-embedded metamaterial unit cell was created and fabricated (Fig. 6) using the aforementioned BSS83 transistor (one of the few commercial transistors that have a physical bulk contact rather than an internal connection between the bulk and the source). The SRR was placed in a TEM waveguide and S_{21} was measured (Fig. 7(c)).

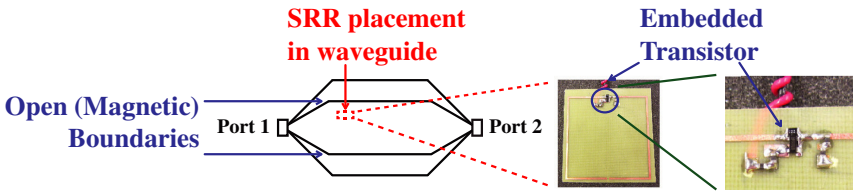

Figure 6. Fabricated FET-embedded unit cell (also seen in [21]). The SRR conducting loop connects the drain and source of the transistor with bias wires heading to the source (ground) and gate (V_{GS}). The waveguide is comprised by two conducting plates 6 cm apart with open boundaries which allow for the bias wires to travel to the unit cell with the bias circuitry being located within the unit cell. The unit cell was fixed in the waveguide such that the loop was parallel to the magnetic field component of the incident wave.

Comparing the experimentally measured data with the simulation data, the measured S_{21} curves demonstrate the expected behavior, agreeing reasonably well in both resonant frequency and magnitude. There is a shift in the SRR resonant frequency corresponding to the low resistance and high resistance values from Fig. 3, as well as a bias range in which the resonance quality is reduced to a minimum (corresponding to the resistance range around 1 kΩ).

With the experimental measurements confirming the validity of the mathematical analysis, the results can be extended to predict the effective material parameters if a slab of such unit cells is created. In the previous analytic calculations, the F factor in Eq. (22) was derived using effective

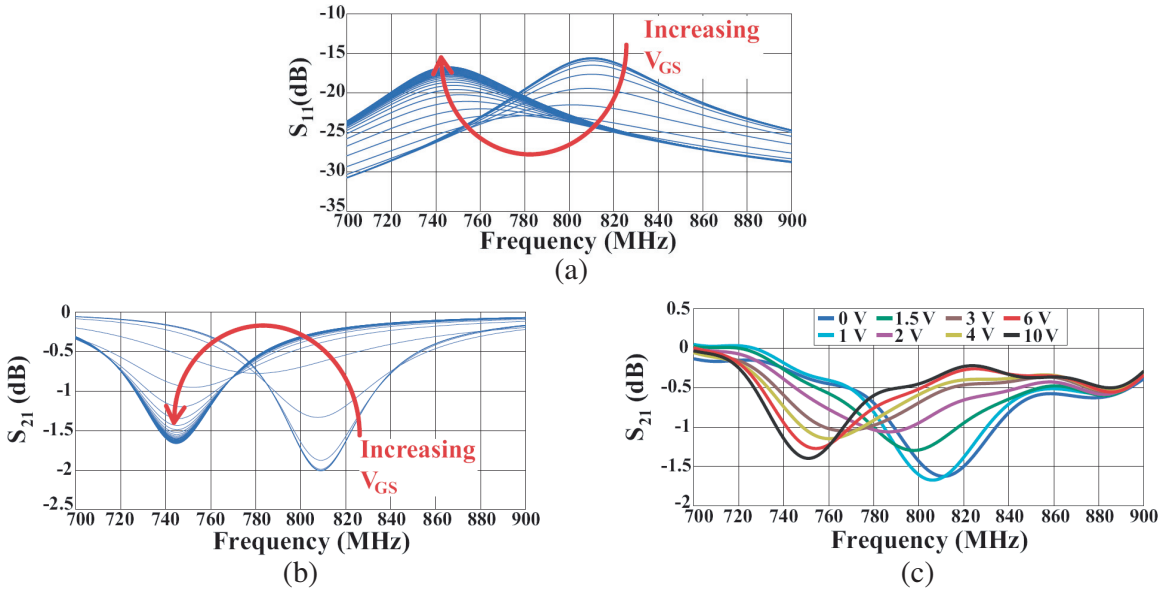

Figure 7. (a) Calculated S_{11}, (b) calculated S_{21}, and (c) measured S_{21} of a single transistor-embedded unit cell as described in Fig. 4 using the setup described in Fig. 6.

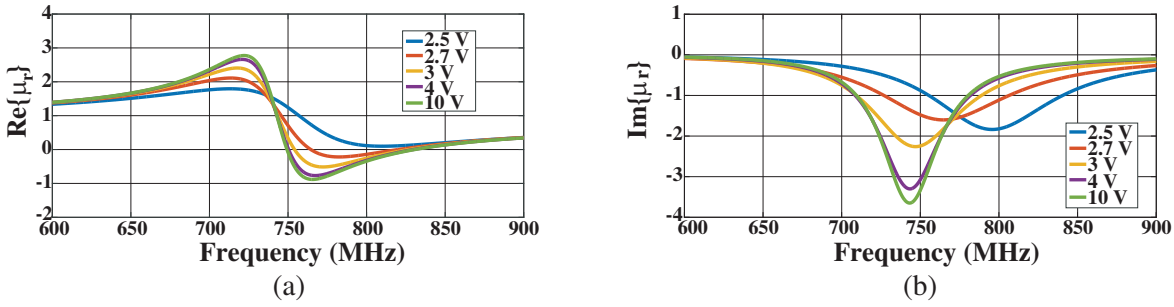

Figure 8. Calculated (a) Re$\{\mu_r\}$ and (b) Im$\{\mu_r\}$ of a metamaterial slab comprised by transistor-embedded SRRs such that the unit cell size was 60 mm × 60 mm × 60 mm. The SRRs configured as shown in Fig. 4 based upon the Q values in Fig. 5.

unit cell dimensions of 60 mm × 60 mm × 500 mm (based on the approximate dimensions of the measurement waveguide). If we assume that the slab would be comprised by unit cells with dimensions 60 mm × 60 mm × 60 mm, the F value increases while keeping the other values from Eq. (22) constant. Based on this theoretical increase in unit cell density, meaningful effective material parameters can be calculated (Fig. 8).

From the relative permeability curves, it is clear that such a metamaterial would potentially be able to still realize a region with negative permeability and that the bandwidth of such a region could be controlled. There are also curves at bias voltages of 2.5 and 2.7 V in Fig. 8(a) that predict that such a slab of metamaterial could create a nearly dispersionless frequency region. Looking at the corresponding data dipicted in Fig. 8(b) shows that this behavior is also associated with the bias condition required for minimum loss magnitude. This metamaterial state corresponds to the circuit bias in which the effective circuit Q reaches a minimum. This potentially reveals a way to passively create a relatively dispersionless material with μ_r near zero.

There is a region around the transistor threshold voltage (around 2 V) in which the resonant frequency and bandwidth changes rapidly, which is ideal for mixing [21]. Once the bias voltage is greater than the threshold voltage, the resonant frequency changes less drastically with changes in voltage, but the resonance quality steadily increases as the voltage continues to increase. The resonant

frequency still changes appreciably, however, which is undesirable in some applications. To minimize the frequency shift, a modification to the transistor circuitry must be made.

4. IMPROVED BANDWIDTH TUNING

The previous section looked at the nMOSFET under cutoff and linear biasing with only a mention of the saturation operating region. This is due to the large differential resistance (g_{ds}) between the source and drain that occurs under this biasing condition if the gate voltage is a purely DC voltage. As mentioned in the previous section, this would diminish the gate voltage's effect on the quality factor. To exploit the effective VCCS element in the small signal model, g_m and V_{gs} must both be non-negligible.

If the drain and gate are connected together, a two terminal element is created and the transistor is said to be diode connected. This changes the small signal model in Fig. 1 to the model in Fig. 9. In this configuration, there are 4 RF current pathways, C_{gs}, C_{ds}, g_{ds}, and the $g_m V_{gs}$ VCCS. The g_{ds} conductor is still governed by Eq. (12), but, as mentioned earlier, does not act as an effective RF shunt for the capacitor.

The VCCS is the primary tunable object in the diode-connected configuration. The drain to source current through this circuit element is controlled by V_{gs}, but since $V_{gs} = V_{ds}$, the current through the VCCS can be rewritten as Eq. (26).

$$I_{DS,VCCS} = g_m V_{gs} = g_m V_{ds} \tag{26}$$

The transconductance product reduces to Ohm's Law since the current is linearly dependent on the voltage across the element (the conductance of the effective resistive element becoming g_m). Using this equivalency, the total drain to source conductance and capacitance is written as:

$$g_t = \frac{1}{R_t} = g_m + g_{ds} \approx g_m \tag{27}$$

$$C_t = C_{db} + C_{gs} \tag{28}$$

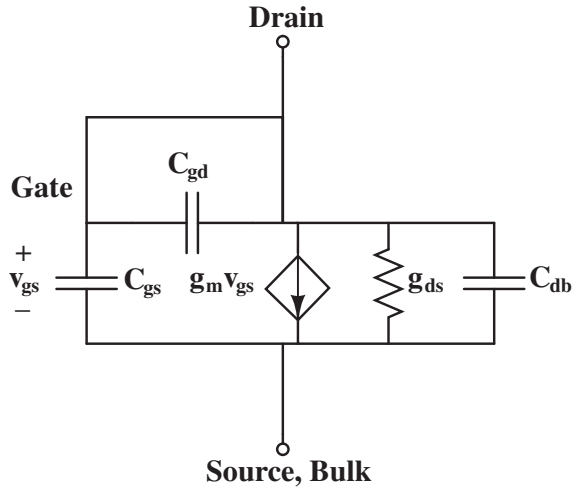

Figure 9. Equivalent small signal model of a diode connected transistor. Note that $v_{gs} = v_{ds}$ in this configuration, turning the VCCS into an effective resistor (Eq. (26)).

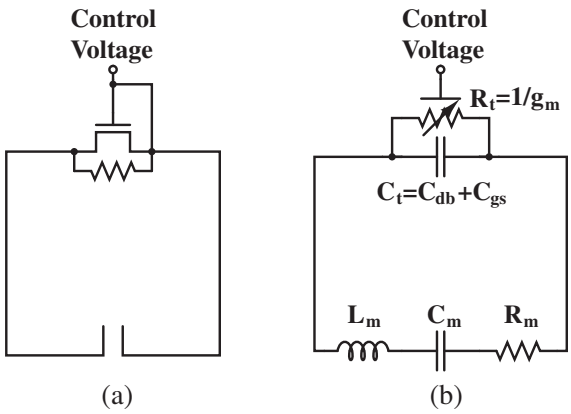

Figure 10. Schematic and diagram of a diode connected transistor embedded SRR. The transistor is embedded such that the gate and drain are tied together. The FET bulk is tied to the source to avoid changes to the threshold voltage with a large-valued resistor connected across the source and drain to avoid hystersis effects from the back to back junctions (DC bias network not shown).

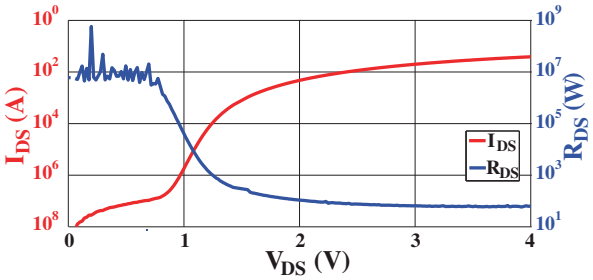

Figure 11. Measured I_{DS} and R_{DS} of the diode-connected BSS83 transistor. Due to measurement error ($I_{DS} < 100\,\text{nA}$ is pushing the accuracy limits of the digital ammeter), the measured deep subthreshold R_{DS} is very noisy but also greater than $1\,\text{M}\Omega$.

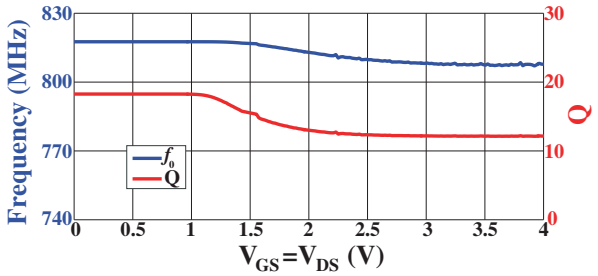

Figure 12. Analytically calculated resonant frequency and Q based upon effective equivalent circuit parameters.

Compared with the capacitance seen in the first configuration (Eq. (8)), the effective capacitance of the element embedded in the SRR loop is increased. This reduces the effect that the transistor capacitance will have on the overall loop capacitance, minimizing the change in resonant frequency caused by the change in voltage across the element.

A diode-connected transistor is embedded within an SRR loop as shown in Fig. 10. As with the previous configuration, the source and bulk are tied together (preventing the threshold voltage changing due to the body effect). A large valued resistor is, again, placed in parallel to the drain and source to ensure that there are no hysteresis effects within the transistor structure (again, this limits the maximum element resistance and therefore the maximum Q of the resonating unit cell).

Unlike the first configuration, a significant amount of DC power is required to bias the transistor in saturation. In order for the saturation condition to be reached, the electric field from the drain to the gate to counteract the vertical field generated by the gate when $V_{GS} > V_T$. Under this condition, the conducting channel between the drain and source is fully formed and a voltage difference between the drain and source must exist. There will be a significant current flowing from the drain to the source, hence a larger amount of DC power will be required for biasing. However, the bias voltages are still DC quantities and if the induced signal power in the unit cell is assumed to be small, the system becomes effectively passive, even though the active transconductance element is the primary tunable element.

Again using a BSS83 nMOSFET, a current-voltage curve was measured and the effective drain to source resistance was extracted (Fig. 11). Due to the maximum power limit of the transistor, the voltage range of interest is also reduced. Comparing Fig. 11 with Fig. 3, the subthreshold region still exhibits the large change in resistance that is expected from the exponential current-voltage relationship, but the element resistance does not decrease to the levels of the resistance at higher voltages as seen in the configuration detailed in Section 3. This means that the second resonant dip (the greater V_{GS} values in Fig. 7) may not be observed in the diode connected configuration, but the resistance change is large enough that a wide range of resonance quality factors should be observed.

Following the same procedure outlined in Section 3, S_{11} (Fig. 13(a)) and S_{21} (Fig. 13(b)) for the modified transistor-embedded SRR were calculated based upon the quality factor of the effective circuit (Fig. 12). Similar to the parameters calculated from the configuration detailed in Fig. 4, as the resistance decreases, the resonance quality should decrease. There is a slight decrease in resonant frequency when the bias voltage increases above the threshold voltage, but this is still a much smaller change as compared to the resonant frequency changes seen in Fig. 7.

To confirm the analytic results, another unit cell based upon the loop geometry seen in Fig. 6 was fabricated with the drain and gate connected with a wire (and to drive the transistor into saturation when the bias voltage was above the threshold voltage). S_{21} measurements were similarly obtained in an open TEM waveguide (Fig. 13(c)) confirming that once the transistor operating characteristics are such that the transistor operates in saturation, the resonant frequency practically ceases changing ($< 2\%$) as the voltage increases.

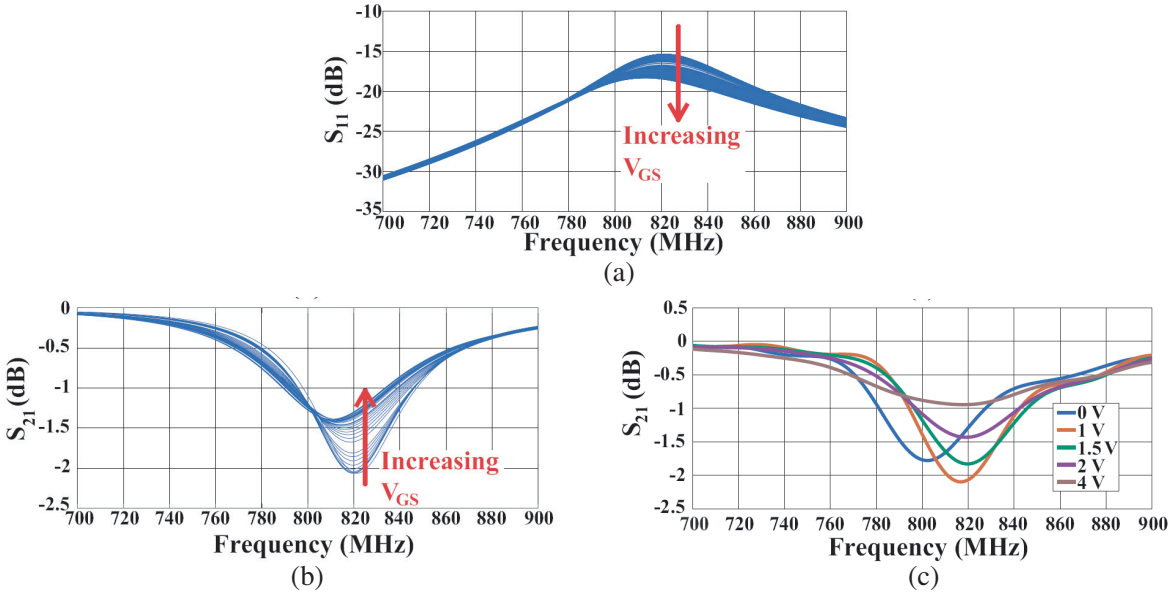

Figure 13. (a) Calculated S_{11}, (b) calculated S_{21}, and (c) measured S_{21} from unit cell embedded with a diode-connected BSS83 transistor.

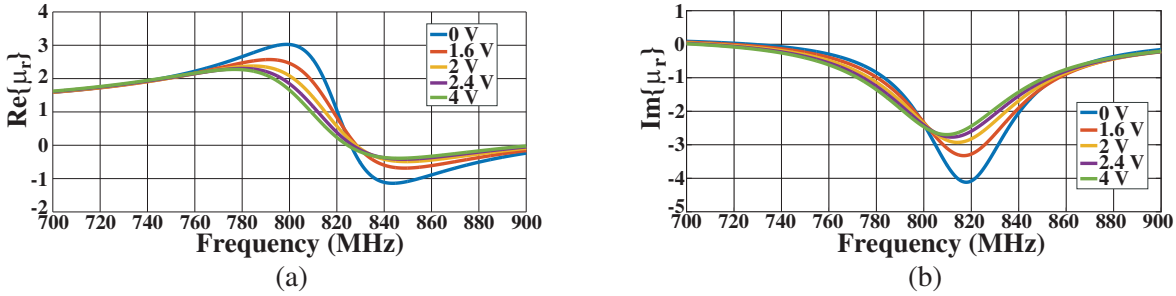

Figure 14. Calculated (a) Re$\{\mu_r\}$ and (b) Im$\{\mu_r\}$ of a metamaterial slab comprised by diode-connected-transistor-embedded SRRs such that the unit cell size was 60 mm × 60 mm × 60 mm. The SRRs configured as shown in Fig. 10 based upon the Q values in Fig. 12.

In contrast to the simulation data in Fig. 13(b), the measured resonance demonstrates that the bandwidth and resonant frequency increase in the subthreshold operating region. This is explained by the structure capacitances changing because of varying bias (this was previously ignored in the analysis in Section 3 as C_{ds} was assumed to remain nearly constant with varying V_{GS} and C_{gs} wasn't relevant in determining the resonant frequency in that configuration). When the voltage was increased to near the threshold voltage, the resonance depth reached a maximum and the resonant frequency became nearly constant with voltage, in agreement with the simulations. Comparing the S_{21} measurements from the two configurations, the resonance quality changes much more smoothly and slowly using the diode connected configuration. This shows that using a diode connected transistor can offer a significant range of resonance quality tuning without modifying the resistance significantly.

To again show the effects that such a tunable metamaterial would have as an effective material, the circuit quality factors were again used to extend the analysis, similarly to Section 3. The F value was changed in the exact same way (modifying one of the unit cell dimensions from 500 mm to 60 mm) and the relative permeability was calculated (Fig. 14). From this extension, a slight shift in the Lorentzian shape is observed and, again, the bandwidth in which the permeability is negative is shown to be tunable. Once again, as the circuit bias modifies the effective circuit Q to its minimum, the relative permeability

curves again predict frequency regions in which the metamaterial exhibits μ near zero behavior while being minimally dispersive with reduced loss compared with the other unit cell configurations with narrower bandwidth.

5. CONCLUSION

The ability for a transistor to be embedded within a metamaterial unit cell for the purposes of frequency tuning and resonance quality tuning has been theoretically developed, analyzed, and experimentally confirmed. This work also demonstrates and exploits the versatility of the transistor structure by using a few of the individual tunable elements derived from the transistor model. The ability to dynamically control the bandwidth and frequency of resonant structures is instrumental in the further development and use of metamaterials and other types of RF structures. Additionally, by controlling both the unit cell density and transistor biasing, a potential design procedure has been developed in which the dispersion can also be controlled without introducing large, prohibitive loss. Future work in this area would include increasing the quality factor tuning range, further minimizing the resonant frequency change, and apply one of these types of unit cells to previously studied small antennas (such as the work previously described in [9–11]).

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