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An Asymmetrical Bulk CMOS Switch for 2.4 GHz Application

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Abstract—A novel asymmetrical single-pole double-throw (SPDT) switch for 2.4 GHz application with high power handle ability is developed. The novel asymmetrical topology is discussed. To increase the power capacity, ac-floating and dc-bias techniques are used. Using these techniques, a switch achieves a measured P1 dB of 20.5 dBm, an insertion loss (IL) of 1.16 dB and an isolation loss of 20.8 dB in TX mode; an insertion loss of 1.57 dB and isolation of 21.6 dB in RX mode. The circuit is fabricated using 3.3-V 0.35-µm DNW NMOS transistors in 0.18-µm bulk CMOS process.

1. INTRODUCTION

Today, many RF circuits such as low noise amplifier (LNA) and voltage control oscillator (VCO) are implemented in CMOS processes. But most RF switches are still fabricated in GaAs or SOI CMOS technology [1], which makes RF switches costly and difficult to integrate with other CMOS RF circuits. If RF switches can be implemented in CMOS process, it should be possible to integrate with other CMOS RF circuits into one chip. This will bring down the cost and improve the ease of use. But in CMOS processes, the low electron mobility, low breakdown voltage and low substrate resistance of nMOS make a high-power capacity, low-loss RF switch difficult to design [2]. Also issues such as parasitic diodes limit the linearity [3, 4]. To improve the linearity of SPDT, many methods are developed. External [5] and on-chip [6] LC matching networks are used in RF switches. But this will increase the cost. A switch with P1 dB of 28.5 dBm and IL of 1.5 dB have been achieved at 2.4 GHz [7] using a parallel LC tank to connect the bulk. Another method to improve the linearity of RF switch is using stacked transistors [8]; however, this will deteriorate the insertion loss.

This paper proposes a novel asymmetrical 2.4 GHz CMOS SPDT using ac-floating and dc-bias techniques [9]. This SPDT is fabricated in 0.18 µm bulk CMOS process using 3.3-V 0.35-µm DNW NMOS transistors. This SPDT achieves a measured P1 dB of 20.5 dBm, IL of 1.57 dB at RX, 1.16 dB at TX and isolation of 21.6 dB at RX, 20.8 dB at TX. This CMOS switch can be integrated into other CMOS circuits. Section 2 covers circuit design, and Section 3 presents the simulation and measurements. Conclusion is given in Section 4.

2. CIRCUIT DESIGN

2.1. Asymmetrical SPDT Circuit Structure

Figure 1(a) is the topological structure of the general SPDT circuit, which contains the TX switch and RX switch. When the SPDT is in the TX mode, the signal flow is as shown in Fig. 1(b). The TX switch is turned on and the RX switch turned off, transmitting signal from the TX port to the antenna port. As it is power signal, it is required that IL of TX switch should be small. Also large signal will appear

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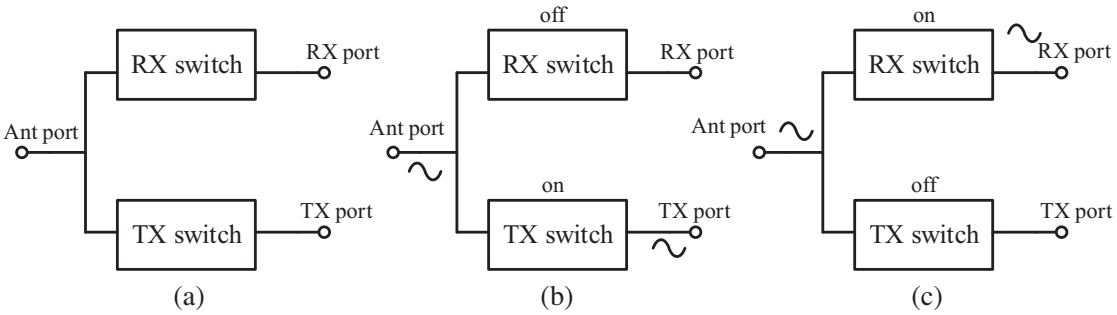

Figure 1. (a) General topology of SPDT. (b) SPDT in TX mode. (c) SPDT in RX mode.

at the TX port and antenna port. Therefore, the RX switch should avoid interference from the large signal and make the TX switch relatively independent. When the SPDT is in RX mode, the signal flow is as shown in Fig. 1(c). The TX switch is shut down and the RX switch turned on to receive the weak signal from the antenna port to the RX port. At this point, it requires that the IL of RX switch should be as small as possible. Besides, the TX switch contributes to IL of SPDT in RX mode. The above requirements can be summarized as follows. The linearity of SPDT requires that TX switch should send power signal as high as possible and that RX switch should not leak signal when power signal appears at antenna port. The IL of SPDT demands that both ILs of TX switch and RX switch should be small. The isolation between RX port and TX port depends upon the closure of RX switch and TX switch.

Figure 2 shows the proposed asymmetrical SPDT circuit structure. Resistances Rg, Rb, Rd, transistors M1 and inductance Ld form the TX switch. Resistances Rg, Rb, Rd, transistors M2, M3, and capacitances C1, C2 form the RX switch. CNT and CNT_NOT is a group of reverse control signals. When CNT is high, and CNT_NOT is low, M1 and M3 are turned on, and M2 is turned off; TX switch is open, and RX switch is closed, so the SPDT is in TX mode. When the CNT is low, and CNT_NOT is high, M1, M3 are turned off, and the parasitic capacitances such as Cgs, Cgd of M1 and Ld form a parallel LC tank, making the TX switch high-impedance at design frequency, thus the TX switch is shut down; M2 is turned on so that the signal flows from antenna port to RX port.

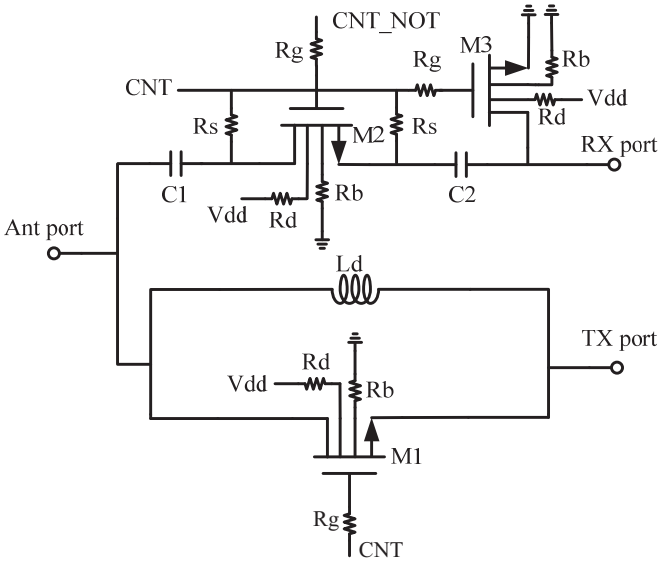

Figure 2. Proposed asymmetrical SPDT circuit structure.

2.2. TX Switch Design

In CMOS process, junction diodes between drain/source and bulk make CMOS transistor difficult to transmit high-power signals. To solve this problem, many techniques have been proposed: 1) ac-floating

technology for DNW NMOS [9]; 2) LC tank body end bias [7]. The common characteristic of these techniques is to improve the substrate impedance, thereby reducing the loss and increasing the linearity of transistor. With the development of CMOS technology, the cost of DNW NMOS is greatly decreased. In some circuits, DNW transistors are widely used to increase noise performance. So the SPDT designed using DNW NMOS can be integrated into other CMOS chips.

Figure 3(a) shows the circuit structure of a TX switch. Fig. 3(b) shows the structure of a DNW MOS transistor. Fig. 3(c) is the equivalent circuit of a TX switch. In Fig. 3(a), when control voltage CNT is high, M1 is turned on; signal flows through M1; the power transmission ability of M1 and the loss of M1 determine the P1dB and IL of TX switch, respectively. When the CNT is low, M1 is turned off, and the high impedance of parallel LC tank isolates TX port and RX port. From Fig. 3(b), when the signal is transmitted from the drain to source, if the signal amplitude is large enough, the parasitic diodes between drain/source and P-well will be turned on during the negative cycle of the signal. Also if the gate of the transistor is connected to the control voltage CNT directly, V_{gs} and V_{gd} will not be a constant and greatly affect the on resistance of M1. So the transmission loss will increase, and linearity will decrease. Ac-floating technique can effectively solve this problem [9]. In Fig. 3(c), R_{on} is about 2 ohms and L_d about 7 nH. So when TX switch is turned on, most current flows through R_{on}, and the voltages of drain and source are almost equal. The capacitances C_{gd}, C_{gs} and the large resistance Rg make the ac voltage of the gate almost the same as that of drain and source. Therefore, voltage V_{gs} and V_{gd} will be a constant. The P-well of DNW NMOS is connected to voltage VPwell through a large resistance Rb, and generally VPwell is ground voltage. The large resistance Rb and parasitic capacitances C_{db} and C_{sb} make the ac voltage of the bulk almost the same as that of drain and source. So the effect of parasitic diodes between drain/source and P-well can be eliminated. Although the ac-floating technique makes ac voltage of gate, drain, source and bulk of M1 approximately equal, the ac voltage amplitude of the gate and bulk is still smaller than that of drain and source. As the transmission power increases, this voltage difference will turn on during negative circle and affect the transistor conduction. Therefore, the power transmission capacity of the transistor is still limited. In Fig. 3(c), deep n-well is connected to voltage VDnwell through a large resistor Rd to shut down the parasitic diode between deep n-well and p-well, and generally VDnwell is VDD. In order to reduce IL and inductance, the W/L of M1 should be larger. In this design, the W/L of M1 is 800u/350n, and all resistors are 20 kΩ.

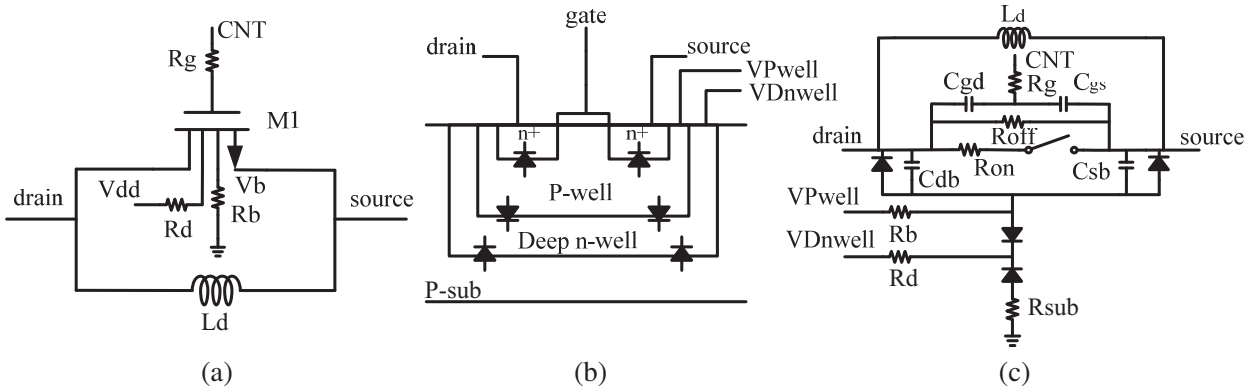

Figure 3. TX Switch (a) structure of TX switch, (b) structure of DNW MOS transistor, (c) equivalent circuit of the TX switch.

2.3. RX Switch Design

Figure 4(a) is the circuit structure of traditional RX switch. In Fig. 4(a), ac-floating technique is used on the transistors M2, M3 to decrease IL. When the CNT is high and the CNT_NOT low, the transistor M2 is turned off to prevent signal leakage, and M3 is turned on to connect RX port to ground. Thus the RX port does not affect other circuits, and the isolation is improved. According to the above analysis, when this SPDT is in TX mode, RX switch is closed, and there will be power signal at antenna port. If the power signal is strong enough, the voltage V_{gd} of M2 will be bigger than V_{th} of M2 due to the

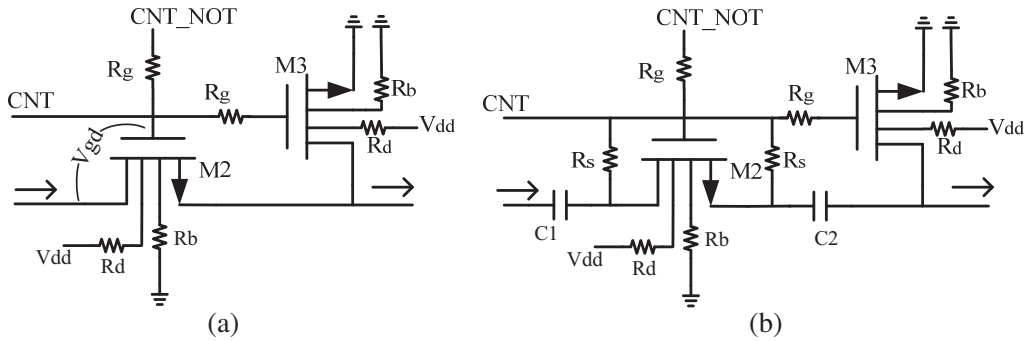

Figure 4. Traditional and proposed RX switch. (a) Traditional RX switch. (b) Proposed RX switch.

negative half cycle of the power signal. Thus M2 will be turned on and leak power signal to RX switch periodically, and the linearity of SPDT will decrease. In order to solve this problem, a new RX switch is proposed in Fig. 4(b). The drain and source of M2 are biased to the control voltage CNT through resistances Rs to get a DC bias. When M2 is shut down, a positive DC voltage will be added to the signal at the drain and source of M2 to prevent M2 from being opened periodically by the power signal. At the same time, DC blocking capacitances are added at the drain and source of M2 to eliminate the impact of DC voltage on the other circuits. When CNT is low and CNT_NOT high, M2 is turned on to receive signal, and M3 is closed to prevent signal from leaking to the ground. The rational size of blocking capacitances will reduce the signal loss in the capacitances.

Based on the above discussion, it can be found that the IL of SPDT in TX mode is related to IL of TX switch and the leakage of RX switch, and that IL of SPDT in RX mode is related to IL of RX switch and the leakage of TX switch. The isolation of SPDT between TX port and RX port depends on the closure of RX and TX switches. The linearity or P1 dB of SPDT is determined by the smaller between the P1 dB of TX switch and the maximum power that the RX switch can keep closed.

3. SIMULATION AND MEASUREMENTS

This SPDT is implemented using 3.3-V 0.35-μm DNW NMOS transistors in 0.18-μm bulk CMOS process. Fig. 5 shows a chip photograph of SPDT. The power supply and control voltages are 3.3 V. The size of SPDT is 356 μm × 740 μm including the ESD protection for control I/O and power supply.

Figure 6 shows the simulation and measurements of this SPDT in TX mode. It can be seen from Fig. 6(a) and Fig. 6(b) that the simulated and measured ILs at 2.4 GHz are 0.86 dB and 1.16 dB, respectively. And the simulated and measured isolations between RX port and TX port are 25 dB and 20.8 dB, indicating that the isolation between RX port and TX port is good. The simulation and

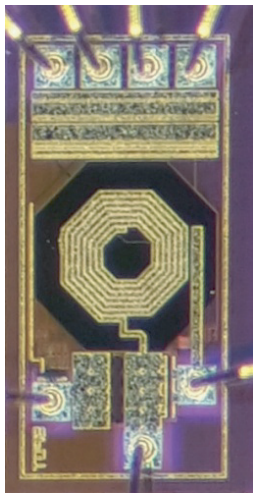

Figure 5. Chip micrograph.

measurement results of SPDT in RX mode are shown in Fig. 7. The simulated and measured ILs are 0.95 dB and 1.57 dB according to Figs. 7(a) and (b). This SPDT has a low IL in RX mode. The isolation is 36 dB for simulation and 21.6 dB for measurement. The result shows that when the SPDT is in RX mode, the RX and TX ports are well isolated. The simulated and measured P1 dB of SPDT are shown in Fig. 8. The simulated P1 dB of SPDT is 33 dBm in Fig. 8(a) and the measured the P1 dB of SPDT is 20.5 dBm in Fig. 8(b), which indicates that this SPDT has a good linearity. Table 1 shows the performance comparison of this design and other works. From the comparison, it can be seen that this design has an advantage on IL and chip area.

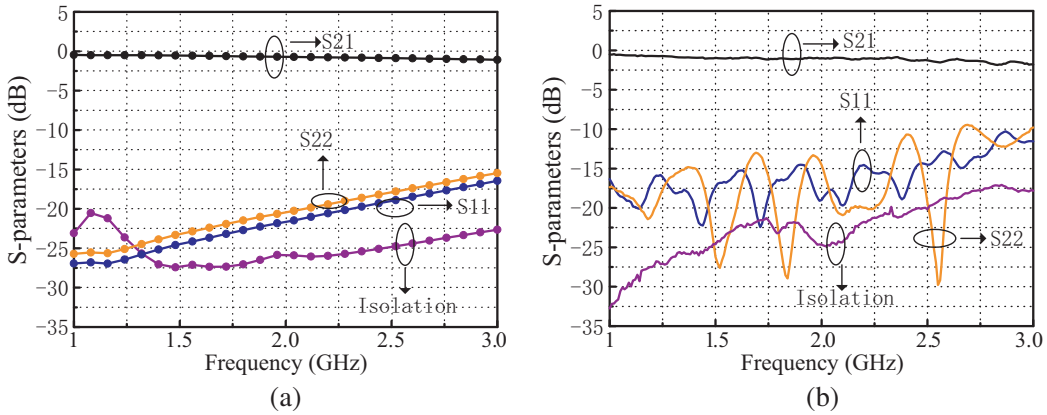

Figure 6. Simulation and measurements in TX mode. (a) Simulation. (b) Measurements.

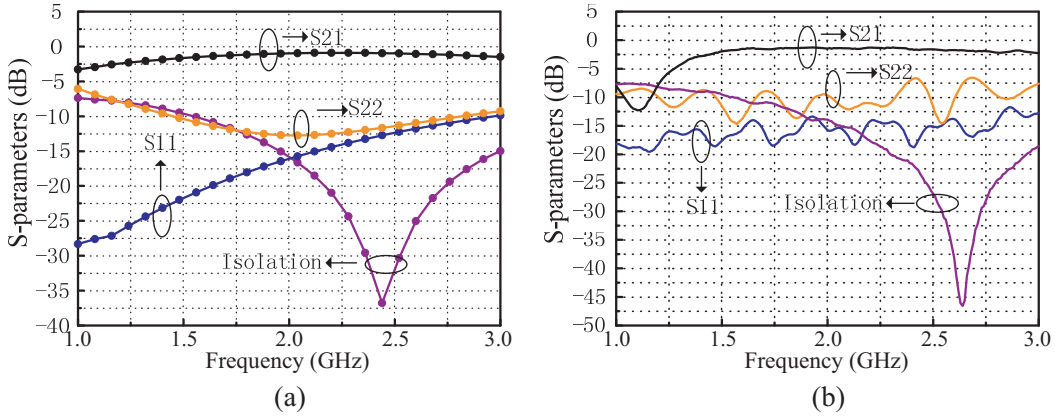

Figure 7. Simulation and measurements in RX mode. (a) Simulation. (b) Measurements.

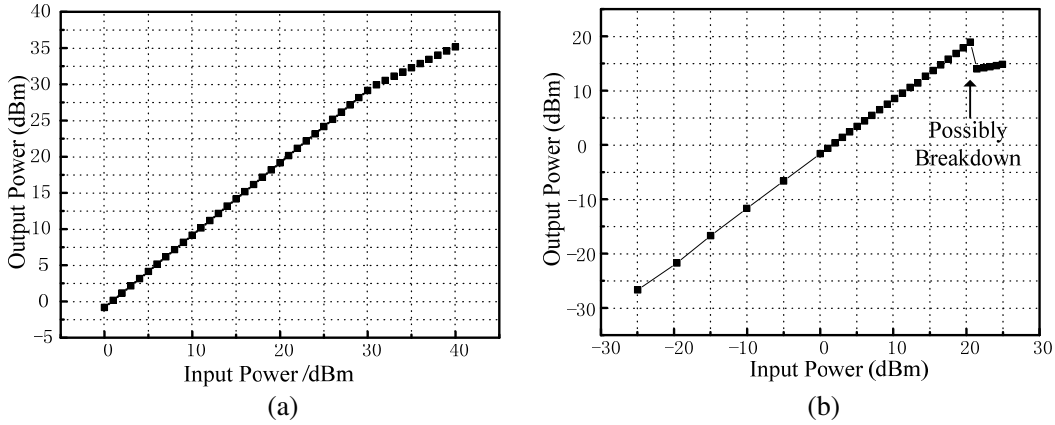

Figure 8. Simulation and measurement of P1 dB. (a) Simulation. (b) Measurement.

Table 1. Performance comparison.

T/R switch	Freq. (GHz)	IL (dB)		Isolation (dB)		IP1 dB for TX (dBm)	Chip Area (mm^2)	CMOS Technology
		TX	RX	TX	RX			
This work	2.4	1.16	1.57	20.8	21.6	20.5	0.26	0.18 µm
[7]	2.4	1.5	1.6	32	17	28.5	0.56	0.18 µm
[10]	5	1.1	2	42.7	-	21.0*	0.6×0.75	0.18 µm

*0.3 dB compression point.

4. CONCLUSION

A novel asymmetric SPDT structure is proposed and discussed in detail. The SPDT is fabricated using 0.18 µm CMOS process. At the design frequency (2.4 GHz), the IL of this design is 1.16 dB in TX mode and 1.57 dB in RX mode. This design achieves a measured P1 dB of 20.5 dBm in TX mode. The isolation between the TX and RX ports is 20.8 dB in TX mode and 21.6 dB in RX mode. This SPDT achieves balance among linearity, insertion loss, and isolation and can be integrated into other CMOS circuits easily.

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