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An X-Band 100 W GaN HEMT Power Amplifier Using a Hybrid Switching Method for Fast Pulse Switching

Hyo-Jong Kim, Woo-Jin Cho, Jun-Hyung Kwon, and Jong-Wook Lee*

Abstract—This paper presents a new hybrid switching technique for enhanced pulsemode solid-state power amplifiers (SSPAs). In the proposed technique, pulse timing for bias stabilization is effectively decoupled from pulse amplification. The decoupling allows fast pulse switching by reducing the pulse width and increasing the pulse repetition frequency (PRF). The new switching method is applied to an X-band SSPA using GaN HEMT. The advantage of the proposed method is demonstrated by its excellent pulse characteristic. The proposed technique achieves a fast PRF of 100 kHz and a narrow pulse width of 1 µsec. The measured rise/fall time(RFT) is 12.5/11.1 nsec, which is more than four times less than that of previous works. In addition, an excellent pulse droop of 0.43 dB is achieved with an output power of 51.3 dBm at 9.9 GHz. The fabricated SSPA shows a maximum output power of 135 W, a small signal gain of 47 dB, and power added efficiency (PAE) of 28.2% at 9.9 GHz. These results show that the proposed pulse switching technique provides a promising solution for SSPAs using a high-power GaN HEMT.

1. INTRODUCTION

Radars are used in a wide range of applications, including weather observation, air traffic control, air surveillance, and target tracking. A power amplifier (PA) with highpower, linearity,and efficiency is a key component in radar systems [1–6]. In the past, the power available from individual solid-state devices has been limited when compared with vacuum tube devices. Recently, significant progress has been made on GaN high-electron-mobility transistors (HEMT) for highpower solid-state power amplifiers (SSPAs) [7–17]. Using pulse compression techniques, radar systems using SSPAs show similar performance to that of vacuum tubes [7]. The GaN HEMT amplifier in [12] produces a 400 W output power in Class-AB pulse mode for a 3.5 GHz WiMAX base station. The work in [14] presents an X-band 100 W pulse mode GaN amplifier for radar systems. The work in [17] presents a GaN HEMT generating 870 W in the S-band (2.9–3.3 GHz).

To relieve the cooling requirement, high-power amplifiers usually operate in pulse mode. Pulse mode operation in time division duplex (TDD) radar systems reduces loss and noise [18]. In pulse mode operation, switching time and pulse flatness are important parameters in TDD radar systems. Sharp pulse edges and narrow pulse width are required to increase radar range resolution. Previous studies have examined the effect of these parameters in pulse mode radar systems [12–15]. The work in [12] used the Class-AB pulse mode, which exhibited slow switching time via time sequential operation. The work in [13] investigated the effect of pulse width on the drain current of GaN HEMT. The authors in [15] conducted a comparative study on various bias modulation methods for a pulse mode SSPA. As shown in [13] and [15], the output pulse characteristic is heavily affected by bias switching, and switching time increases with the output power level. This is because the charging time of the capacitive elements

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present in the bias switching network increases with power. Given the trade-off between pulse distortion and output power in the conventional method, it is difficult to obtain a narrow pulse width under high power operation.

In this paper, we propose a new pulse switching method to solve the trade-off problem. In the proposed method, we add a pulse modulation switch at the input of the amplifier, and the switch is operated in a synchronous manner with the bias modulation. In this way, the pulse timing for bias modulation is effectively decoupled from the pulse amplification. The de-coupling effectively removes the output pulse distortion due to the fast pulse switching, allowing for pulse mode operation with a narrow pulse under high power operation. Using the proposed technique, we fabricate a pulse mode SSPA delivering over 100 W in the X-band. Comparisons of measured data with previous works demonstrate enhancement in such parameters as rise/fall time (RFT), pulse width, pulse droop, and pulse repetition frequency (PRF).

2. SWITCHING TIME ANALYSIS

Figure 1 shows conventional methods for pulse mode SSPA; the input pulse modulation method is shown in Fig. 1(a). In this method, pulse modulation is performed outside an SSPA using an external switch, and the SSPA subsequently amplifies the modulated signal. The RFT of the output pulse is determined via the characteristics of the external switch. This method has an advantage in that the amplifier design can be tailored to optimize the output pulse characteristics, and high linearity can be achieved. The drawback is that the amplifier operates continuously even when there is no input signal resulting in low efficiency. The bias pulse modulation method is shown in Fig. 1(b). In this method, a continuous wave (CW) signal is supplied to the input of an SSPA. For pulse modulation, the power supply is switched on and off by a bias switching driver (BSD) [7, 13, 15]. This method provides relatively simple implementation compared to input pulse modulation. In addition, this method can achieve high efficiency because the bias is applied only when there is an input signal. The disadvantage is that the output pulse shape is easily affected by the BSD. When a fast bias transient is applied to the BSD, it adversely affects the output pulse shape resulting in overshoot and ringing. Thus, there exists a tight coupling between the pulse modulation and bias switching. Using these conventional methods, it is difficult to achieve both high power and fast pulse switching.

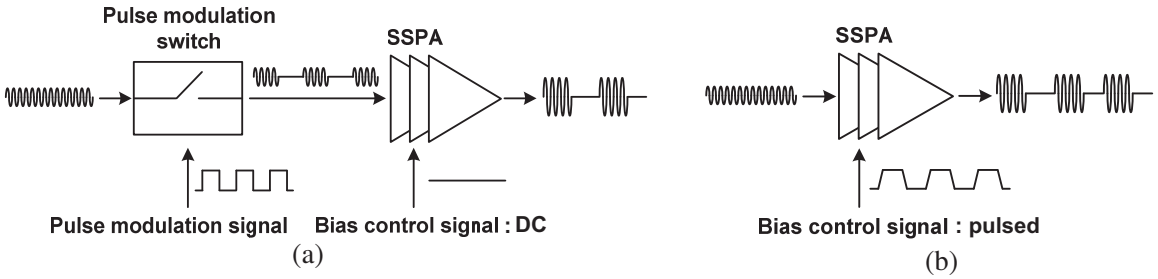


Figure 1. Conventional pulse mode operation. (a) Input pulse modulation, (b) bias pulse modulation methods.

2.1. Switching Time Analysis of Power Transistor

RFT is an important parameter in pulse mode operation, and determines the minimum pulse width and the maximum PRF. The RFT is determined via the delay in both the power transistor and BSD. First, we analyze the switching time of the power transistor. Figure 2 shows a schematic of the switching time analysis;the transistor parameters include a series gate resistance R_g, gate-to-source capacitance C_{gs}, gate-to-drain capacitance C_{gd}, transconductance g_{fs}, source inductance L_s, and drain inductance L_d. To simplify the analysis, we neglect small source and drain resistances. Using a voltage step $V_G u(t)$, the gate is pulsed from $V_{GS0} = -5\,\mathrm{V}$, which is smaller than the threshold voltage V_T. A fixed bias voltage

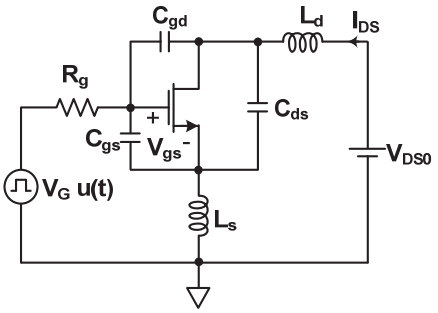


Figure 2. Transistor schematic.

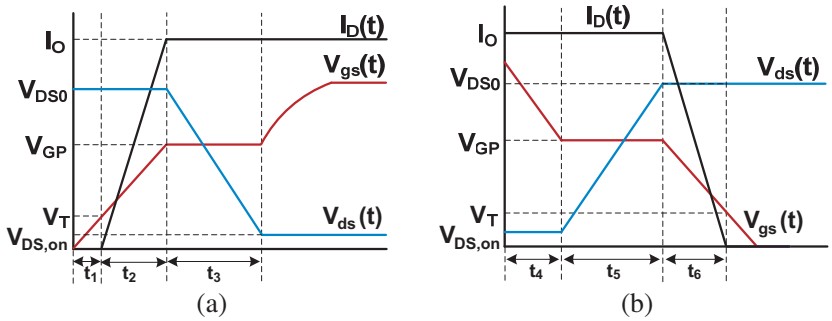


Figure 3. Voltage and current waveforms. (a) Turn-on (b) turn-off.

V_{DS} is applied at the drain. Figure 3(a) shows voltage and current waveforms during the turn-on transient. The transient is divided into three time intervals [19].

1) Time interval t_1: In this time interval, the gate-source voltage $V_{gs}(t)$ is smaller than V_T, and there is no drain current $I_D(t)$ or voltage drop across L_s. The transient is determined via the charging time of C_{gs} and C_{gd} as

$$V_{gs}(t) = V_G(1 - e^{\frac{-t}{R_g(C_{gs}+C_{gd})}}) \tag{1}$$

The time interval ends when $V_{gs}(t_1) = V_T$. By solving Eq. (1), we obtain

$$t_1 = R_g(C_{gs} + C_{gd}) \ln\left(\frac{1}{1 - (V_T/V_G)}\right). \tag{2}$$

2) Time intervalt_2: In this time interval, $I_D(t)$ rises linearly in proportion to $V_{gs}(t)$. In a packaged device, inductances can have a significant effect on the time delay. L_s in particular significantly increases the switching time due to its negative feedback operation. Considering the effect of L_s and L_d [20], $V_{gs}(t)$ is obtained by solving

$$K_1\frac{d^2V_{gs}(t)}{dt^2} + K_2\frac{dV_{gs}(t)}{dt} + V_{gs}(t) = V_G, \tag{3}$$

where $K_1 = R_gC_{gd}g_{fs}(L_s + L_d)$ and $K_2 = R_g(C_{gs} + C_{gd}) + L_sg_{fs}$.

Depending on the relative magnitudes of K_1 and K_2, Eq. (3) gives either sinusoidal or exponential solutions. In the case of $(K_2)^2 - 4K_1 \leq 0$, we obtain sinusoidal solutions as

$$V_{gs}(t) = V_G - (V_G - V_T)e^{-\frac{K_2}{2K_1}t}\left[\cos\left(\frac{\sqrt{4K_1 - K_2^2}}{2K_1}t\right) + \frac{K_2}{\sqrt{4K_1 - K_2^2}}\sin\left(\frac{\sqrt{4K_1 - K_2^2}}{2K_1}t\right)\right]. \tag{4}$$

In the case of $(K_2)^2 - 4K_1 > 0$, we obtain exponential solutions as

$$V_{gs}(t) = V_G - \frac{V_T - V_G}{\tau_2 - \tau_1}\left(\tau_1e^{-t/\tau_1} - \tau_2e^{-t/\tau_2}\right). \tag{5}$$

Using a linear transconductance approximation, $I_D(t)$ can be expressed as

$$I_D(t) = g_{fs}\left(V_{gs}(t) - V_T\right). \tag{6}$$

The time interval t_2 ends when $I_D(t)$ reaches the full load current I_O. In the case of $(K_2)^2 - 4K_1 \leq 0$, time interval t_2 is obtained by solving Eqs. (4) and (6) as

$$I_D(t_2) = g_{fs}\left[V_G - (V_G - V_T)e^{-\frac{K_2}{2K_1}t_2}\left[\cos\left(\frac{\sqrt{4K_1 - K_2^2}}{2K_1}t_2\right) + \frac{K_2}{\sqrt{4K_1 - K_2^2}}\sin\left(\frac{\sqrt{4K_1 - K_2^2}}{2K_1}t_2\right)\right] - V_T\right] = I_O. \tag{7}$$

In the case of $(K_2)^2 - 4K_1 > 0$, the time interval t_2 is obtained by solving Eqs. (5) and (6) as

$$I_D(t_2) = g_{fs}\left[V_G - \frac{V_T - V_G}{\tau_2 - \tau_1}\left(\tau_1 e^{-t_2/\tau_1} - \tau_2 e^{-t_2/\tau_2}\right) - V_T\right] = I_O, \tag{8}$$

where $\tau_1 = 2K_1/(K_2 - \sqrt{K_2^2 - 4K_1})$ and $\tau_2 = 2K_1/(K_2 + \sqrt{K_2^2 - 4K_1})$.

3) Time interval t_3: Because $I_D(t) = I_O$ is constant in this interval, $V_{gs}(t)$ is kept at a fixed gate voltage V_{GP} as

$$V_{gs}(t) = V_T + I_O/g_{fs} = V_{GP}. \tag{9}$$

When $V_{gs}(t) = V_{GP}$, the gate current I_G charges only C_{gd}. Therefore, the change in V_{gd} is the same as $-V_{ds}(t)$, where $dV_{gd}/dt = -dV_{ds}/dt = I_G/C_{gd} = [(V_G - V_{GP})/R_g]/C_{gd}$. Using the initial condition of $V_{ds}0$, $V_{ds}(t)$ can be expressed as

$$V_{ds}(t) = V_{DS0} - \frac{V_G - (V_T + I_O/g_{fs})}{R_g C_{gd}}t = V_{DS0} - \frac{V_G - V_{GP}}{R_g C_{gd}}t. \tag{10}$$

At the end of time interval t_3, $V_{ds}(t)$ reaches the on state voltage $V_{DS,on}$. Using Eq. (1), t_3 is expressed as

$$t_3 = \frac{(V_{DS0} - V_{DS,on})R_g C_{gd}}{V_G - (V_T + I_O/g_{fs})}. \tag{11}$$

Figure 3(b) shows the current and voltage waveforms that occur during turn-off transient. The analysis is similar to the case of turn-on transient.

4) Time interval t_4: In this time interval, $V_{gs}(t)$ falls at a rate determined by the time constant $R_g(C_{gs} + C_{gd})$. There is no change in $I_D(t)$ until $V_{gs}(t)$ falls to V_{GP}. During this period, $V_{gs}(t)$ can be expressed as

$$V_{gs}(t) = V_G e^{\frac{-t}{R_g(C_{gs}+C_{gd})}}. \tag{12}$$

This interval ends at time t_4 when $V_{gs}(t)$ falls to V_{GP}. Using Eqs. (9) and (12), we obtain t_4 as

$$t_4 = R_g(C_{gs} + C_{gd}) \ln\left(\frac{V_G}{V_T + (I_O/g_{fs})}\right). \tag{13}$$

5) Time interval t_5: In this time interval, $V_{ds}(t)$ rises to V_{DS} while both $I_D(t)$ and $V_{gs}(t)$ remains constant. The I_G is discharged through C_{gd}. Using the initial condition of $V_{DS,on}$, $V_{ds}(t)$ can be expressed as

$$V_{ds}(t) = \frac{1}{R_g C_{gd}}\left(V_T + \frac{I_O}{g_{fs}}\right)t + V_{DS,on}. \tag{14}$$

This interval ends at time t_5 when $V_{ds}(t)$ rises to V_{DS} and we obtain

$$t_5 = \frac{R_g C_{gd}(V_{DS0} - V_{DS,on})}{V_T + (I_O/g_{fs})}. \tag{15}$$

6) Time interval t_6: In this time interval, both $I_D(t)$ and $V_{gs}(t)$ change. During this time interval, $I_D(t)$ falls from I_O to zero. This time interval ends at time t_6 when $V_{gs}(t)$ falls to V_T. A change in $I_D(t)$ produces a change in the voltage across L_s and L_d. This current flow restrains the $V_{gs}(t)$ rate of decrease. A similar analysis may be performed during time interval t_2. In the case of $(K_2)^2 - 4K_1 \leq 0$, time interval t_6 is obtained by solving

$$I_D(t_6) = g_{fs}\left[(V_T + I_O/g_{fs})\, e^{-\frac{K_2}{2K_1}t_6}\left[\cos\left(\frac{\sqrt{4K_1 - K_2^2}}{2K_1}\right)t_6 + \frac{K_2}{\sqrt{4K_1 - K_2^2}}\sin\left(\frac{\sqrt{4K_1 - K_2^2}}{2K_1}\right)t_6\right] - V_T\right] = 0. \tag{16}$$

In the case of $(K_2)^2 - 4K_1 > 0$, t_6 is obtained by solving

$$I_D(t_6) = g_{fs}\left[-\frac{V_T + I_O/g_{fs}}{\tau_2 - \tau_1}\left(\tau_1 e^{-t_6/\tau_1} - \tau_2 e^{-t_6/\tau_2}\right) - V_T\right] = 0. \tag{17}$$

Table 1 shows transistor parameters of a 50 W GaN HEMT which includes two die chips (See Fig. 1) [21]. The parameters are extracted using the method presented in [22]. R_{gs} represents the gate-to-source resistance and R_{ds} the drain-to-source resistance DC parameters are given in the data sheet as $V_T = -4\,\text{V}$, $I_O = 5\,\text{A}$, $V_{GP} = 1.8\,\text{V}$, and $g_{fs} = 4.5\,\text{S}$. The GaN HEMT is biased at $V_{DS0} = 24\,\text{V}$ and $V_{GS0} = -5\,\text{V}$. Table 2 shows the calculated time intervals. Using Eqs. (2), (8), and (11), we obtain the risetime as $t_1 + t_2 + t_3 = 17\,\text{nsec}$. For the fall time, we obtain $t_4 + t_5 + t_6 = 0.8\,\text{nsec}$ using Eqs. (13), (15) and (17). The results show that the GaN HEMT can be switched with a fast RFT that is on the order of a nanosecond.

Table 1. Transistor parameters for a 50 W GaN HEMT.

Parameter	Value	Parameter	Value	Parameter	Value
$L_g\,(\text{nH})$	0.64	$L_d\,(\text{nH})$	0.45	$L_s\,(\text{nH})$	0.21
$R_g\,(\Omega)$	9.1	$R_d\,(\Omega)$	7.78	$R_s\,(\Omega)$	0.86
$R_{gs}\,(\Omega)$	40.3	$R_{ds}\,(\Omega)$	12.7	$g_{fs}\,(\text{S})$	4.5
$C_{gs}\,(\text{pF})$	8.8	$C_{ds}\,(\text{pF})$	0.2	$C_{gd}\,(\text{pF})$	0.43

Table 2. Calculated time intervals for a 50 W GaN HEMT.

Time delay	t_1	t_2	t_3	t_4	t_5	t_6
Time (nsec)	0.04	1.38	0.24	0.01	0.04	0.77

2.2. Switching Time Analysis of Bias Switching Driver

Figure 4(a) shows a schematic of the BSD for gate switching (GS). A simplified equivalent circuit for the switching time analysis is shown in Fig. 4(b). The voltage divider (R_1 and R_2) generates a gate switching pulse $V_{P,GS}(t)$. When a power MOSFET Q_1 is turned on, it provides a low resistance path to the ground. The delay in Q_1 is determined by a gate resistor R_{gQ1} and two input capacitors, C_{gsQ1} and C_{gdQ1}. Because of the abrupt switching action of Q_1, we consider the total delay as the sum of the delay in Q_1 and the voltage divider. When Q_1 turns on, $V_{P,GS}(t)$ rises from V_{GS} to $(V_{GS}R_2)/(R_1 + R_2)$ and can be expressed as

$$V_{P,GS}(t) = \frac{V_{GS0}}{R_1 + R_2}\left(R_2 + R_1 e^{\frac{-t}{\tau_{GS1}}}\right), \tag{18}$$

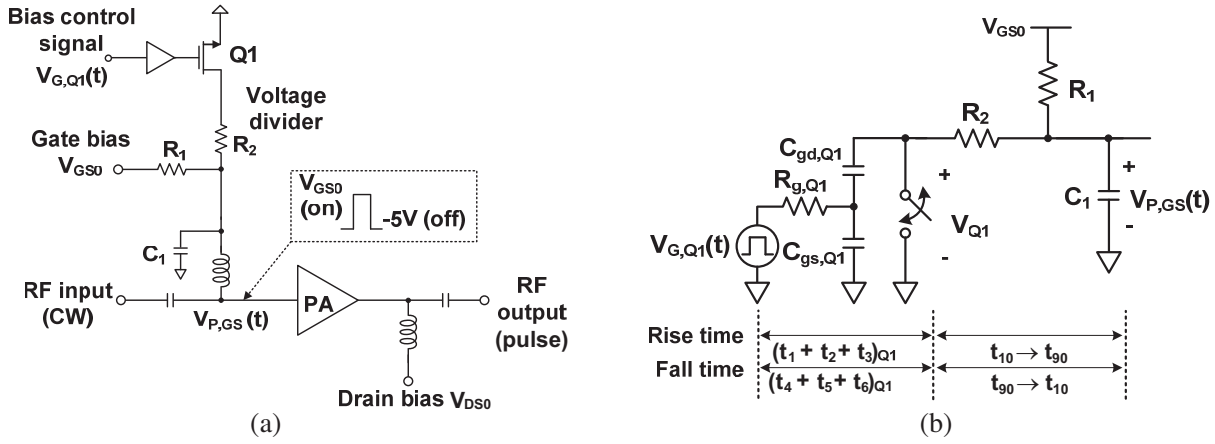


Figure 4. (a) Schematic of BSD for gate switching, (b) simplified circuit for switching time analysis.

where $\tau_{GS1} = (R_1 \| R_2)C_1$. Rise time is defined as the time it takes for a signal to increase from 10 to 90% of its final value. Then, the time t_{10} for the 10% value is obtained by solving

$$V_{P,GS}(t_{10}) = \frac{V_{GS0}}{R_1 + R_2}\left(R_2 + R_1 e^{\frac{-t_{10}}{\tau_{GS1}}}\right) = V_{GS0} + \frac{1}{10}\left(\frac{R_2}{R_1 + R_2}V_{GS0} - V_{GS0}\right). \tag{19}$$

The time t_{90} for the 90% value is obtained in a similar manner. Then, the rise time t^G_{rise} can be expressed as

$$t^G_{rise} = t_{90} - t_{10} = \tau_{GS1}\ln\left(\frac{10}{1}\right) - \tau_{GS1}\ln\left(\frac{10}{9}\right) = \tau_{GS1}\ln(9). \tag{20}$$

When Q_1 turns off, $V_{P,GS}$ falls from $(V_{GS}R_2)/(R_1 + R_2)$ to V_{GS0}, and it can be expressed as

$$V_{P,GS}(t) = V_{GS0} + V_{GS0}\left(\frac{R_2}{R_1 + R_2} - 1\right)e^{\frac{-t}{\tau_{GS2}}}, \tag{21}$$

where $\tau_{GS2} = R_1C_1$. In a similar manner, the fall time t^G_{fall} can be expressed as

$$t^G_{fall} = \tau_{GS2}\ln(9). \tag{22}$$

Including the time delay in Q_1, the RFT of gates witching is obtained using

$$t_{rise,GS} \cong (t_1 + t_2 + t_3)_{Q_1} + t^G_{rise} \tag{23}$$

$$t_{fall,GS} \cong (t_4 + t_5 + t_6)_{Q_1} + t^G_{fall} \tag{24}$$

The overall amplifier chain in this work consists of three stages, where each stage delivers 4, 15, and 50 W. GaAs FETs are used for both 4 and 15 W power stages, which are biased at $V_{DS} = 10$ V. For the 50 W stage, the GaN HEMT is biased at $V_{DS} = 24$ V. As shown in Eqs. (23) and (24), the RFT is determined by the delays of Q_1 and the voltage divider. The V_{GS0} required by the amplifier are dependent on the power level. Considering the trade-off between the RFT and reliability, we choose $R_1 = 800$ and $400\,\Omega$ for 4 and 15 W GaAs FETs, respectively. For 50 W GaN HEMT, we choose $R_1 = 100\,\Omega$. $R_2 = 100\,\Omega$. Fig. 5 shows gate switching waveforms for three power stages delivering 4, 15, and 50 W. The amplifier is operated at 9.9 GHz. The results show good agreement between measured and simulated data. Table 3 shows the calculated, simulated, and measured RFT depending on P_{OUT}. The result shows that the fall time dominates the overall RFT. Because a larger R_1 is required for the amplifier with a higher P_{OUT}, the RFT decreases with P_{OUT}.

Figure 6(a) shows a schematic of the BSD for drain switching (DS). A simplified equivalent circuit for switching time analysis is shown in Fig. 6(b). With the bias control signal, Q_3 abruptly switches the voltage at the gate terminal of Q_2. Fast bias switching at the gate terminal of Q_2 can cause overshoot. The overshoot is reduced using a pulse shaping circuit (R_F and C_F) at the gate of Q_2. Capacitor banks at the source terminal of Q_2 provide an instant supply of high current during pulse operation; therefore,

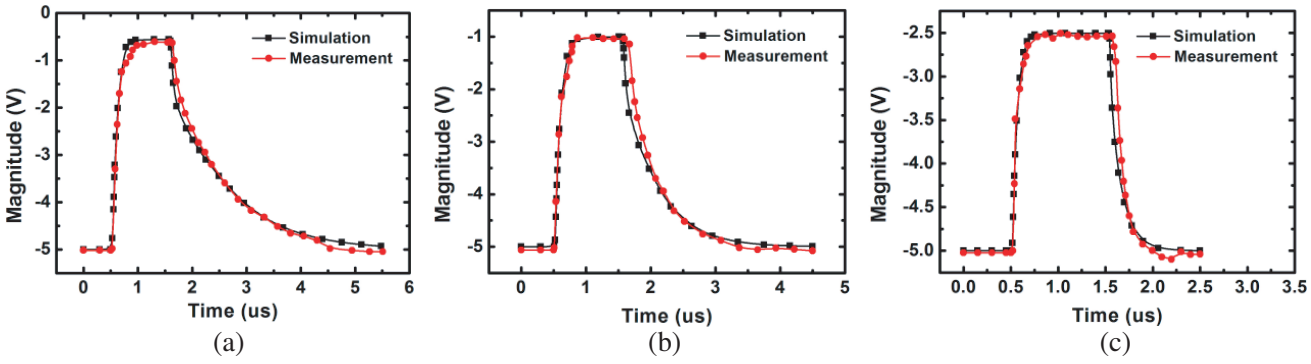


Figure 5. Measured and simulated waveforms of gate switching for stages delivering. (a) 4 W, (b) 15 W, (c) 50 W.

Table 3. Comparison of RFT for different output power using gate switching.

Output power	Calculation (nsec)		Simulation (nsec)		Measurement (nsec)	
	Risetime	Falltime	Risetime	Falltime	Risetime	Falltime
4 W	213	1842	193	2096	208	1972
15 W	194	963	182	1029	189	984
50 W	127	260	119	245	119	251

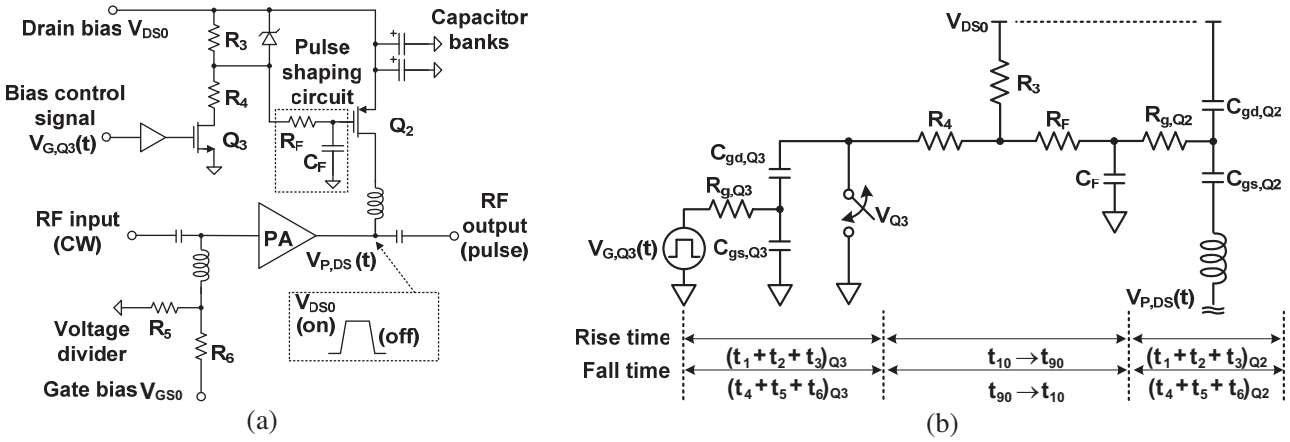


Figure 6. (a) Schematic of the BSD for drain switching, (b) simplified circuit for switching time analysis.

its capacity is designed to be sufficiently large to prevent pulse droop. Switching time analysis for the drain switching is similar to that of the gate switching. The rise time t^D_{rise} can be expressed as

$$t^D_{rise} = t_{10} - t_{90} = \tau_{DS1} \ln(9), \tag{25}$$

where $\tau_{DS1} = C_F\ (R_F + R_3 \| R_4)$. The fall time t^D_{fall} can be similarly expressed as

$$t^D_{fall} = t_{90} - t_{10} = \tau_{DS2} \ln(9), \tag{26}$$

where $\tau_{DS2} = C_F\ (R_F + R_3)$. Including the time delay of Q_2 and Q_3, we obtain the RFT of drain switching using

$$t_{rise,DS} \cong (t_1 + t_2 + t_3)_{Q_2} + t^D_{rise} + (t_1 + t_2 + t_3)_{Q_3} \tag{27}$$

$$t_{fall,DS} \cong (t_4 + t_5 + t_6)_{Q_2} + t^D_{fall} + (t_4 + t_5 + t_6)_{Q_3}. \tag{28}$$

Considering the trade-off between the RFT and reliability, we choose $R_3 = 40\,\Omega$ and $R_4 = 50\,\Omega$ for 4 and 15 W GaAs FETs, respectively. For 50 W GaN HEMT, we choose $R_3 = 75\,\Omega$ and $R_4 = 25\,\Omega$. Fig. 7 shows waveforms of drain switching for three power stages delivering 4, 15, and 50 W. The results show good agreement between measured and simulated data. The fall time dominates the overall RFT. In addition, the RFT of the drain switching is on the order of hundreds of nanoseconds, which is smaller than that of the gate switching. Table 4 shows the calculated, simulated, and measured RFT depending on P_{OUT}. Although GaN HEMT can switch rapidly over a few nsec, the analysis shows that the overall RFT is limited by the delay in BSD. The longer switching time is caused by the tight coupling between the pulse amplification and bias switching. To solve this problem, we propose a hybrid pulse switching method, as explained in the next section.

3. HYBRID PULSE SWITCHING METHOD

Figure 8(a) shows the proposed hybrid pulse switching method. In this method, we add a pulse modulation switch at the input of the SSPA. The switch is operated in synchronous with the bias

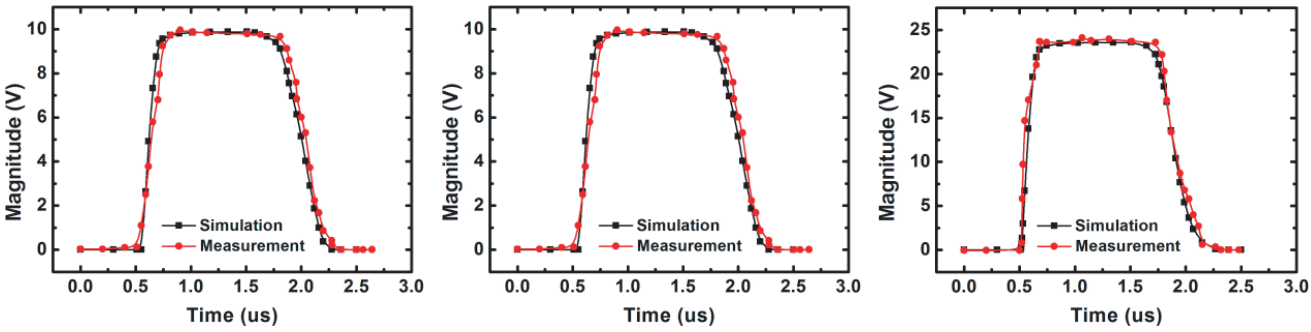


Figure 7. Measured and simulated waveforms of drain switching for stages delivering. (a) 4 W, (b) 15 W, (c) 50 W.

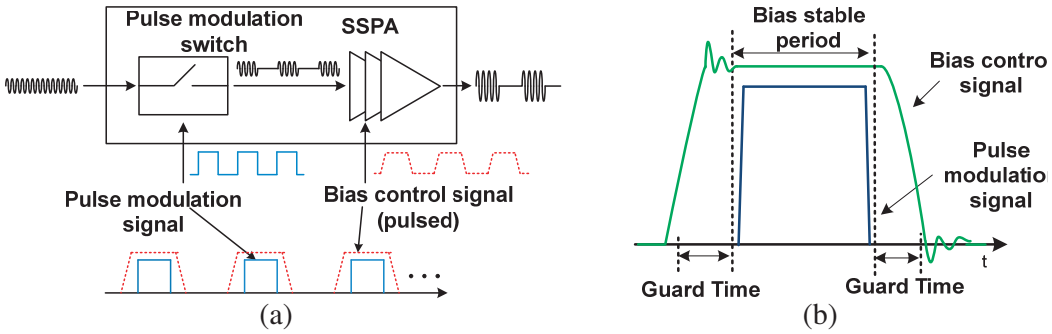


Figure 8. (a) Hybrid pulse switching method using synchronous bias control and pulse modulation signals. (b) Timing sequence in the hybrid pulse switching method.

Table 4. Comparison of RFT for different output power using drain switching.

Output power	Calculation(nsec)		Simulation(nsec)		Measurement(nsec)	
	Risetime	Falltime	Risetime	Falltime	Risetime	Falltime
4 W	127	363	126	339	113	325
15 W	127	363	126	339	113	325
50 W	134	286	114	316	105	310

control signal. The RF pulse signal is amplified after the DC bias is stabilized. Thus, the overshoot and ringing in the bias control signal have negligible effects on the output pulse shape. In this way, the operation of bias modulation is effectively decoupled from pulse amplification and the RFT is determined by the input pulse modulation switch.A key advantage of this approach is that the amplifier design can be optimized for both efficiency and output pulse characteristics. Fig. 8(b) shows the timing sequence in the hybrid pulse switching method. There are two pulse signals, bias control and pulse modulation signals, which are time synchronized. Because the bias control signal carries a high current pulse, we observe overshoot and ringing during pulse switching. Therefore, we allocate guard time before and after the pulse modulation signal. In this way, the transient in the bias control signal does not affect the output pulse shape. Considering the trade-off between timing margin and efficiency, we choose 20 nsec for the guard time.

Figure 9(a) shows a system block diagram of the X-band pulse mode SSPA. The system consists of a pulse modulation switch, a driver amplifier, a main amplifier, and two pulse modulators.For the pulse modulation switch, a GaAs single-pole-double-throw (SPDT) switch is used. The switch has an insertion

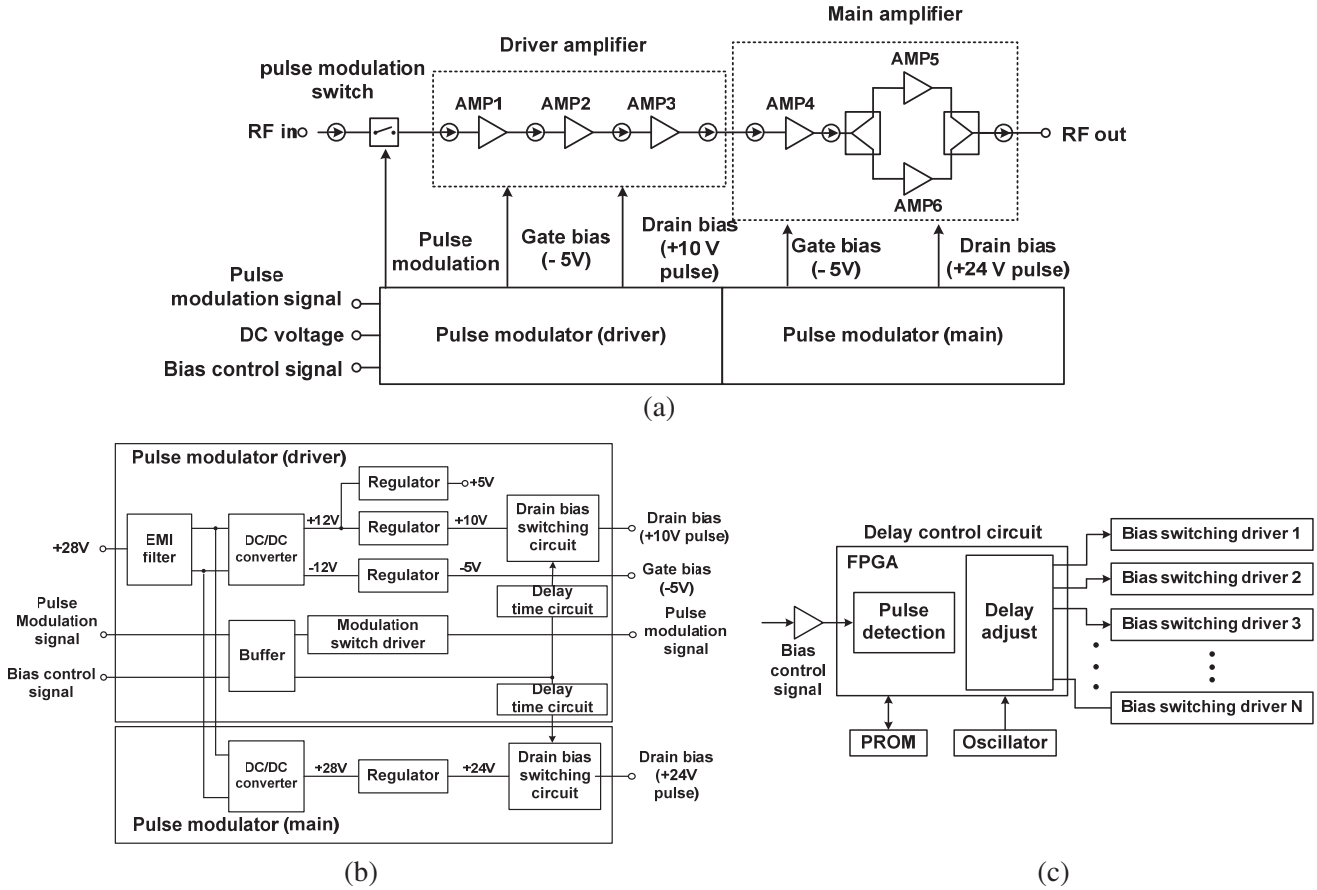


Figure 9. Block diagram of (a) X-band pulse mode SSPA, (b) pulse modulators, (c) delay control circuit.

loss of 2.7 dB and an isolation level of 42 dB. To achieve the timing synchronization, we design the pulse modulators for the driver and main amplifiers, as shown in Fig. 9(b). The pulse modulator includes an EMI filter, DC/DC converters, regulators, a modulation switch driver, bias switching drivers, and delay control circuits. To prevent electromagnetic interference via high bias current switching, the EMI filter is used at the input of the DC/DC converter [23]. The output of the converter is the input to the regulators to supply the gate and drain bias voltages. Several GaN HEMTs are needed to achieve a high power at the X-band, demanding multiple BSDs.Because of component mismatches, the time delays in the BSD can vary. To remove the mismatch, we synchronize the turn-on time of multiple BSDs using a delay control circuit, as shown in Fig. 9(c) After characterizing the maximum delay time among the BSD, we tune the delay time for each driver.

Figure 10 shows a schematic of the main amplifier. To deliver an output power of 100 W, we combine two GaN HEMTs using branch line couplers. The bias circuit is carefully designed to deliver 6 A for each stage with a small loss. To achieve a broad bandwidth of 1 GHz, a radial stub is used for the bias network.The GaN HEMT provided by a vendor is internally matched to 50 Ω in the frequency range of 8.5–9.6 GHz. To extend the bandwidth for the target frequency band of 9.5–10.5 GHz, we design broadband matching networks, as shown in Fig. 11. The measured input reflection coefficients are $\Gamma_{IN} = 0.394\angle 62.8°$, $0.341\angle -31.5°$, and $0.3\angle -115.7°$ at 9.5, 10.0, and 10.5 GHz, respectively, and the measured output reflection coefficients are $\Gamma_{OUT} = 0.488\angle 153.2°$, $0.585\angle 99.7°$, and $0.548\angle 40.17°$, respectively. Using the reflection coefficients, we design multistage impedance matching elements to achieve the desired frequency response. The input matching is designed in steps from Γ_{IN}^* to 50 Ω, as shown in Fig. 11(a). A similar approach is adopted for the output matching, as shown in Fig. 11(b). The fabricated input and output matching circuits have been tuned iteratively through measurements.

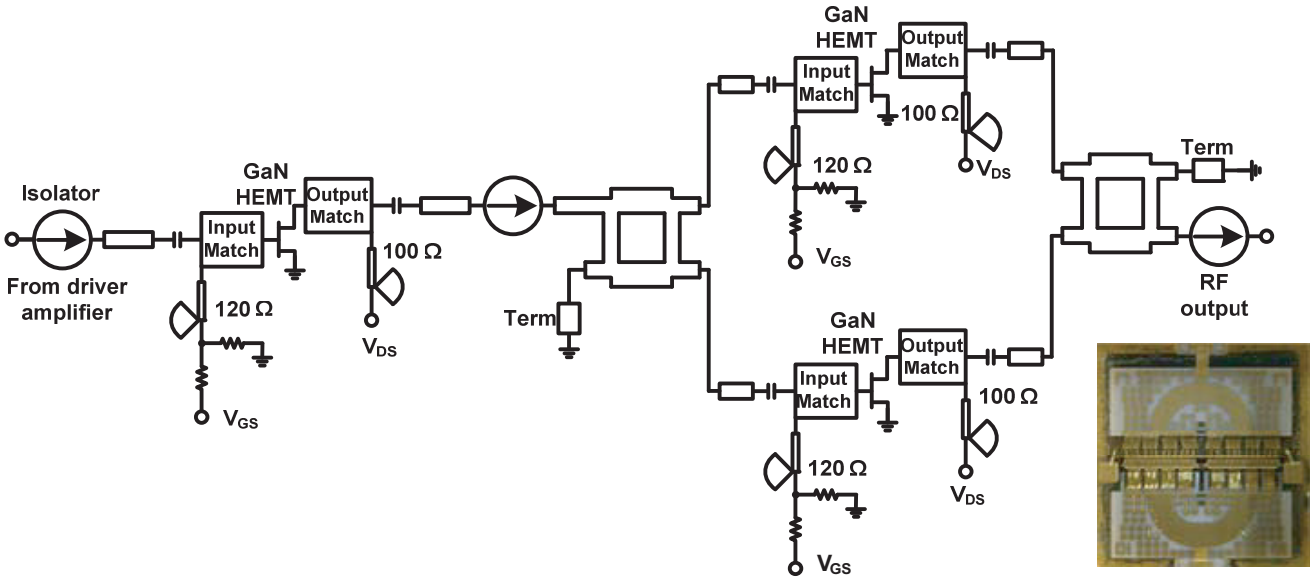


Figure 10. Schematic of the main amplifier.Photo of 50 W GaN HEMT die is shown in the inset.

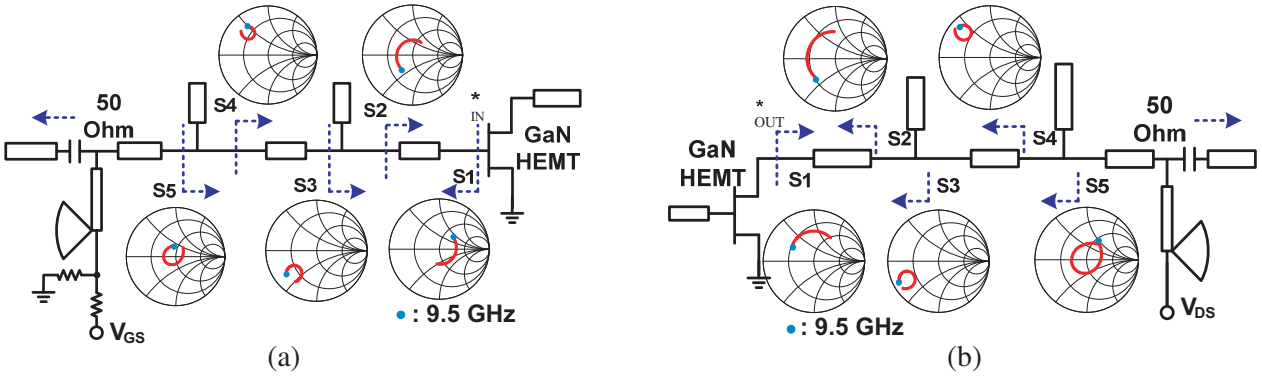
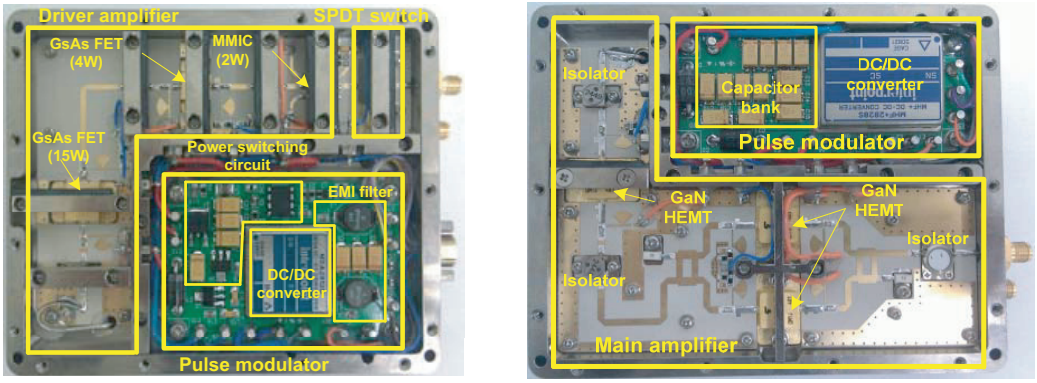


Figure 11. Design of broadband matching networks for (a) input matching, (b) output matching.

4. EXPERIMENT RESULTS

Figure 12 shows a photograph of the fabricated SSPA with a size of $130 \times 105 \times 31\,\text{mm}^3$. The amplifier module is designed considering efficient heat sinking, isolation, and power handling capability. Fig. 13 shows the measured power sweep of the SSPA in pulse mode. The small-signal gain is 47 dB. A maximum P_{OUT} is 51.3 dBm with a peak PAE of 28.2%. Fig. 14 shows an RFT comparison of different pulse switching methods. The switching time between 10 to 90% pulse transitions has been measured using an oscilloscope. Using drain switching (DS), the average RFT over 9.5–10.6 GHz is 119.3/339.8 nsec for rise and fall times, respectively. Using the gate switching (GS), the average RFT is 220.1/1000.4 nsec. In comparison, the average RFT is 12.4/11.1 nsec using hybrid switching. These results demonstrate that fast pulse switching is achieved using the proposed hybrid switching. The measured RFT of the modulation switch (SPDT + switch driver) is 12.5/10.9 nsec, which is in agreement with the average RFT of the amplifier. The result indicates that the RFT is determined by the speed of the input modulation switch, and there is little distortion or time delay added by the amplifier itself. In addition to the RFT, the pulse droop is one of the key characteristics in pulse mode SSPA.

Figure 15 shows the measured pulse droop. The result shows that both drain and hybrid switching deliver similar average P_{OUT}. When compared to drain switching, hybrid switching reduces the pulse



(a) (b)

Figure 12. Photograph of the fabricated pulse mode SSPA. (a) Driver amplifier, (b) main amplifier modules.

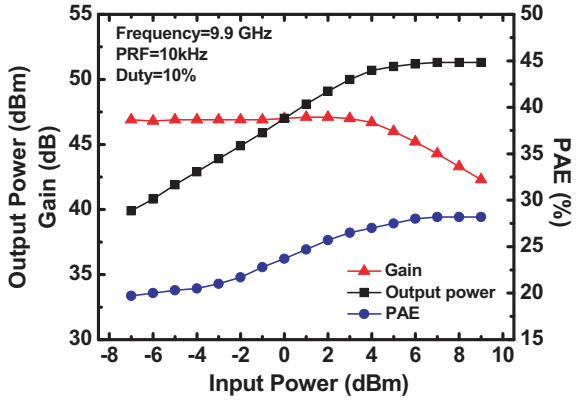


Figure 13. Measured power sweep of the SSPA.

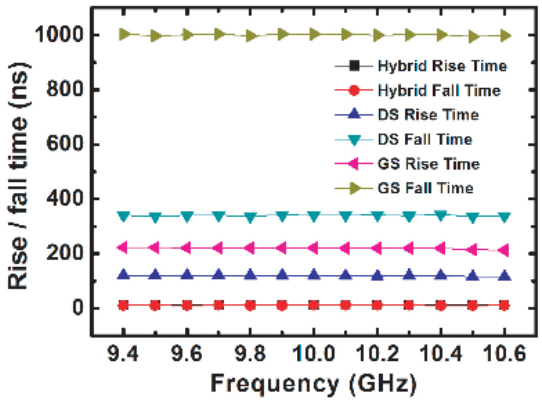


Figure 14. Comparison of measured RFT.

(a) (b)

Figure 15. Measured pulse droop characteristics obtained using (a) hybrid switching, (b) drain switching.

droop from 1.93 to 0.43 dB. Fig. 16 shows the measured P_{OUT} for various PRF over the frequency. With a 10% duty cycle and 10 kHz PRF, $P_{OUT} > 50$ dBm is achieved over a 900 MHz bandwidth of 9.5–10.4 GHz. Figure 17 shows the measured RFT of the SSPA based on the input power P_{IN}. When the P_{IN} changes from -5 to $+5$ dBm, the RFT ranging from 10.3 to 13.1 nsec does not change significantly;

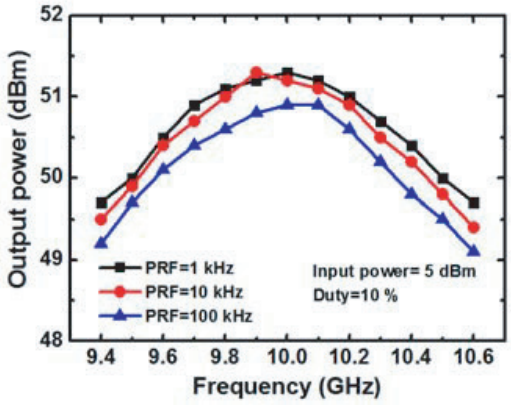


Figure 16. Measured output power versus pulse repetition frequency.

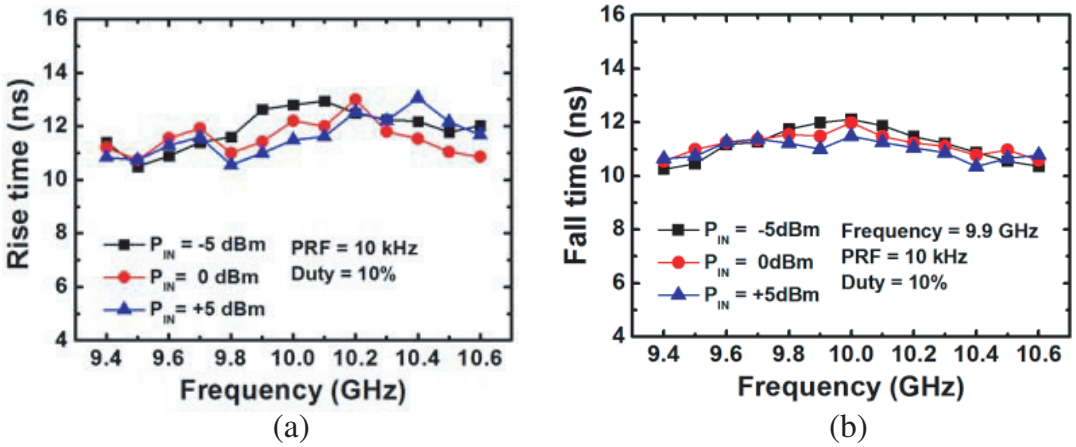


Figure 17. Measured RFT as a function of input frequency for various input power. (a) Rise time, (b) fall time.

thus, the proposed method maintains a relatively constant RFT even when the P_{IN} is varied. This behavior is desirable for an operation requiring variable P_{OUT}. This is in contrast to the previous result [13], where the RFT ranging from 20 to 120 nsec is heavily affected by the P_{IN}.

Table 5 shows a performance comparison with the previously reported SSPAs. With a relatively low operating frequency, the works in [13, 15, 17] use gate switching. When compared with Reference [13], our work shows more desirable pulse characteristics; RFT is not sensitive to the P_{IN} change. Reference [15] shows a performance comparison obtained using the drain and gate switching, where the two methods achieve similar P_{OUT} and drain switching achieves faster RFTs; these results are consistent with our results. The work in [17] uses GaN HEMT for S-band pulse mode operation. Because of the slow transient response caused by gate switching, PRF is limited to 0.5 kHz. Among the pulse mode SSPA in the X-band, both [7] and [14] use drain switching. The work in [7] achieves a high $P_{OUT} > 250$ W, however, the result is measured using a relatively low PRF of 1.1 kHz. Finally, the pulse width is fixed to 64 μsec while it can be varied from 1 to 100 μsec in the present work. Reference [14] shows a P_{OUT} similar to that in this study. The PAE shown is superior to ours; however, the result is measured at a single tuned frequency. The hybrid switching technique proposed in this work achieves a high PRF ($\sim$ 100 kHz) and the smallest pulse width ($\sim$ 1 μsec). In addition, both the pulse width (from 1 to 100 μsec) and the PRF (from 1 to 100 kHz) can be varied, allowing a flexible and adaptive pulse mode operation. And the RFTis not affected significantly by the P_{IN} level. Overall, the proposed hybrid switching method achieves the fastest RFT among the previous works.

Table 5. Performance comparison with previous works.

Parameter	This work		[7]	[13]	[14]	[15]		[17]
Frequency (GHz)	9.5–10.4		9.1–9.6	3.5	9.8	5.3–5.4		2.9–3.3
Pulsing Method	Hybrid	Drain	Drain	Gate	Drain	Gate	Drain	Gate
Rise/fall time (nsec)	12.5/11.1	53.7/53.9	N.A.	> 120	N.A.	538/470	116/103	N.A.
Device	GaN HEMT + GaAs FET	GaN HEMT + GaAs FET	GaN HEMT + GaAs MMIC	GaAs FET	GaN HEMT	GaAs FET	GaAs FET	GaN HEMT
P_{OUT} (W)	100	100	250	10	100	13.5	13.9	870
Gain (dB)	47	47	38.2	14	10	45	45	13.8
PAE (%)	28.2	28.2	24.5	N.A.	53	13.9	14.9	52.7
Pulse width (μsec)	1–100	10	64	N.A.	10	20.9	21.7	200
Pulse rep. freq. (kHz)	1–100	10	1.1	100–400	10	3.8	3.8	0.5

5. CONCLUSION

This paper proposes a new hybrid pulse switching technique to enhance the pulse mode operation of a high-power GaN HEMT. Using the proposed technique, we successfully fabricate an SSPA delivering over 100 W in the X-band. The fabricated SSPA shows a maximum output power of 135 W, a small-signal gain of 47 dB, and a PAE of 28.2% at 9.9 GHz. The SSPA achieves a fast PRF of 100 kHz, a narrow pulse width of 1 μsec, and a pulse width of 1 μsec. An average RFT of 12.5/11.1 nsec is achieved over 9.5–10.4 GHz, which is more than four times smaller than the value obtained with conventional pulse switching methods. Furthermore, the RFT is not sensitive to changes in the input power level. In addition to enhanced switching speed, the proposed method exhibits excellent pulse flatness. Overall, the proposed hybrid switching method is promising for the advanced pulse mode operation of high-power GaN HEMT SSPA.

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