Progress In Electromagnetics Research C, Vol. 74, 31–40, 2017

4-Bit Ka Band SiGe BiCMOS Digital Step Attenuator

Muhammad Masood Sarfraz[1, 2], Yu Liu[1, 2, *], Farman Ullah[1, 2], Minghua Wang[1, 2], Zhiqiang Li[1, 2], and Haiying Zhang[1, 2]

Abstract—This paper presents a Ka-band 4-bit BiCMOS digital step attenuator with maximum attenuation of 7.5 dB (16 states). The proposed attenuator design is based on switched T-bridge network including phase correction network and is fabricated in 0.13 µm SiGe BiCMOS technology. Attenuator with phase correction structure shows root mean square (RMS) amplitude errors < 0.8 dB at 31 to 33 GHz and the RMS insertion phase varying from 2.8° to 5.8° over 31–33 GHz. The measured insertion loss is 19 dB and total chip size including pad is $1.92 \times 0.4\,\text{mm}^2$.

1. INTRODUCTION

Signal amplitude control circuits such as variable gain amplifiers (VGA) and signal attenuators are widely used in contemporary wireless communication systems, phase array radar and temperature compensation of power amplifiers [1–3]. In phased-array antennas, a constant transmission phase and amplitude control is required to avoid tracking errors. In order to get the constant phase and required amplitude, each signal phase and amplitude must be precisely and accurately set. Typically, this is done by the core blocks of RF transceivers such as phase shifter and attenuator. In addition, low phase variation and precise amplitude control are the essential parameters for the phased-array systems where several transmit/receive modules are integrated to control multiple circuits [1, 4].

Variable Gain Amplifier has been a traditional approach to produce variable gain output, but it has the limitations of high power dissipation and also not suitable for mm-wave applications. Attenuators are superior to VGA for achieving the same function with better outcomes because of their high power handling capability and high linearity which are extremely important for wideband applications such as vehicular radar, mobile communication and test equipment. Furthermore, the advancement in CMOS and SiGe BiCMOS technology provides faster devices with improved characteristics which are suitable for mm-wave applications [5, 6].

Linearity, bandwidth and attenuation range are distinctive factors in an attenuator design. Several designs of digital step attenuator using different topologies such as switched path attenuators [7], switched Pi/T attenuators [1] and distributed step attenuators [8, 9] have been reported previously for mm-wave band applications. The switched-path attenuators are constructed from two SPDT switches with two paths in between, and each path has a different attenuation. This topology provides low phase variation over attenuation states but high insertion loss at reference state due to cumulative losses of SPDT switches for multibit design. In addition, it occupies larger chip area. The distributed step attenuators applications are limited due to its larger chip area and cost even though these attenuators are benefited with low insertion loss and good source and load matching. The switched Pi/T attenuators are the combination of series and shunt resistive network and use switches for attenuation. However, it is hard to get optimum attenuation and bandwidth at mm-wave frequencies [1, 10].

Received 8 March 2017, Accepted 27 April 2017, Scheduled 9 May 2017

* Corresponding author: Yu Liu (liuyu5@ime.ac.cn).

[1] Institute of Microelectronics, Chinese Academy of Sciences, Beijing Key Laboratory of Radio Frequency IC Technology for Next Generation Communications, Beijing 100029, China. [2] University of Chinese Academy of Sciences, 19A Yuquan Rd., Shijingshan District, Beijing 100049, China.

In the present work, we demonstrate a 4-bit digital step attenuator designed in 0.13 µm SiGe BiCMOS technology for Ka-band applications using 2nd order capacitive phase correction network. We chose T-bridge digital step attenuator topology for its simplicity and high linearity response for lower bit attenuators, i.e., 0.5 dB, 1 dB, 2 dB and 4 dB and also have fewer components and good RF performance than π-type network [1, 6]. Using the proposed design for the attenuator, we achieved high linearity and low phase variation in wide band. In Section 2, we introduce the technique of the proposed design and explain how the previous design limitations have been overcome by the proposed method. The obtained results are stated in Section 3. In Section 4, we compare the proposed method with various other published attenuators. Finally, the work is summarized in Section 5.

2. CIRCUIT DESIGN

The conventional switched T-type attenuators are composed of series/shunt switches and resistors. A nMOS transistor as the series/shunt switches is a key component of digital step attenuators. An nMOS device is usually used as a switch due to its low on-resistance and off-capacitance. When nMOS switch is on, it acts as a resistor, and its R_on can be calculated as in Eq. (1) [11]. Equivalent circuit model of nMOS switch with R_on resistance and C_off capacitance are shown in Fig. 1

$$\text{R\_on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \tag{1}$$

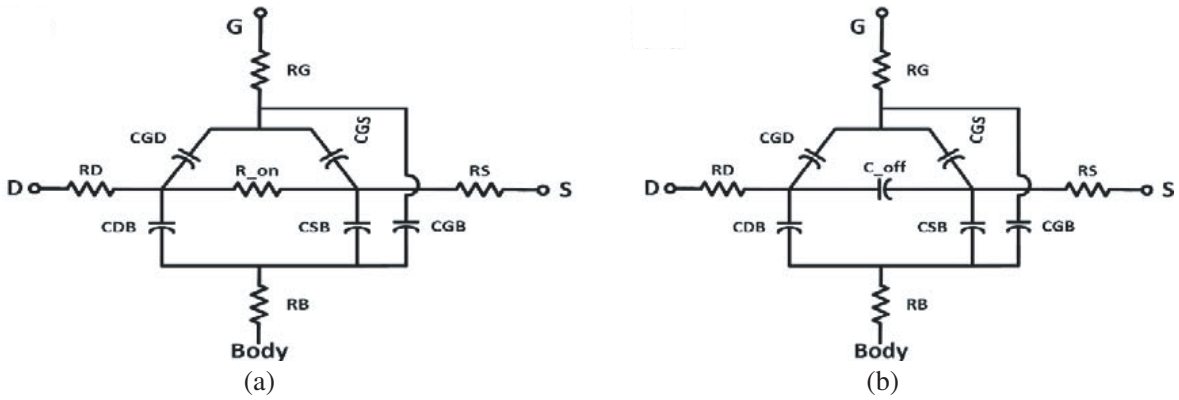

Figure 1. Equivalent circuit model of nMOS switch (a) at R_on State, (b) at C_off State.

In switch-on state, the on-resistance of nMOS switch will cause attenuation of the signal amplitude when the signal is passing through it. For large gate width, the on-resistance is small and acts as a short path for the signal from input to output. However, in switch-off state, the switch acts as capacitive path as shown in Fig. 1(b) and provides a leakage path for the signal and hence the large phase difference is observed since the capacitance has the phase lead characteristic. Also, the parasitic capacitances including gate-source and gate-drain capacitance (CGS, CGD) form a forward path to the signal that causes phase lead. While the junction capacitances (CDB and CSB) provide leakage paths to the body.

In switch-off state as shown in Fig. 1(b), the gate and junction capacitances (CGS, CGD, CSB and CDB) make the series configuration and provide signal path. These capacitances also cause insertion phase when these devices are used as switches in series branch. Alongside, the junction capacitances contribute to the input/output matching networks that may alter the matching of the system and thus causes insertion loss. These paths decrease the signal power transmitted from the input of an nMOS switch to its output, which increases the insertion loss of attenuators. Therefore, a large resistor R_G is connected to the gate of nMOS switch in order to prevent the signal leakage from the gate. Furthermore, an appropriate gate width needs to be decided by the tradeoff between insertion loss and phase.

The amplitude of an attenuator can be switched between the maximum attenuation state and minimum attenuation state with insertion of switches in series and shunt branches, respectively. The

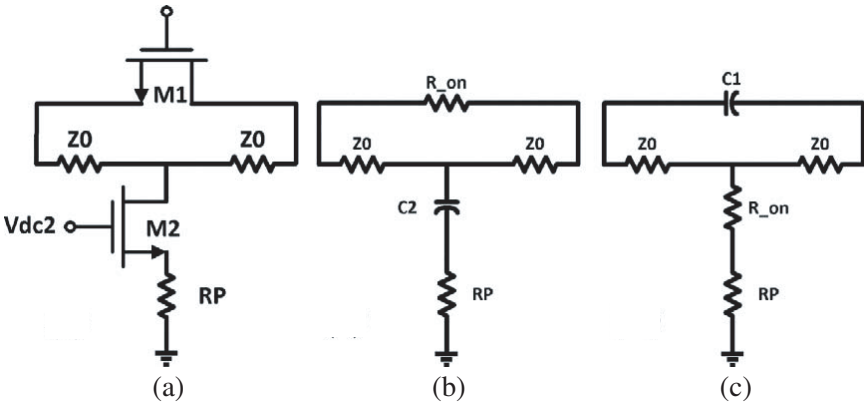

Figure 2. (a) Conventional structure of T bridge-type attenuator. (b) Reference and (c) attenuation state.

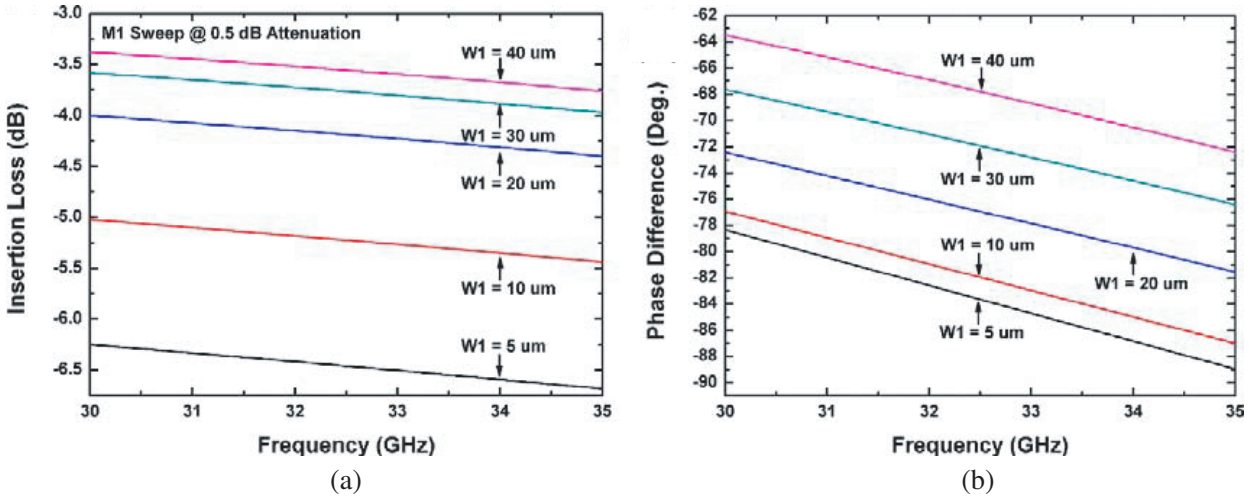

Figure 3. Simulation result of (a) insertion loss and (b) phase difference of 0.5 dB conventional T-Bridge attenuator.

maximum attenuation value depends on the series and shunt resistor values of the attenuator circuit. Resistor values of the attenuator circuits can be calculated by two-port network analysis [12].

Conventional switched T-bridge attenuator with reference and attenuation state is shown in Fig. 2 and consists of series and shunt transistors. When gate width of M1 transistor of the conventional switched T-bridge attenuator is increased, on-resistance is decreased as depicted in Eq. (1). Also, its performance is changed with the change in gate width of transistor M1. It is demonstrated in Fig. 3, where the insertion phase and insertion loss are deviated with change in gate width of M1 of the 0.5 dB conventional attenuator. It can be seen that as the gate width is varied from 5 µm to 40 µm, the insertion loss is decreased. At the same time, the insertion phase is also increased. Hence, it can be concluded that the conventional topology cannot have both low insertion loss and small phase difference simultaneously.

In order to have no transmission phase difference, it is important to satisfy the following condition [1, 12]

$$\Delta\emptyset = \emptyset_A - \emptyset_R = 0 \tag{2}$$

To have zero phase difference, the switch-off capacitances C1 and C2 of series and shunt transistors respectively shown in Fig. 2 must ideally be zero. However, at high frequencies, i.e., Ka band, these capacitances in conventional topology do not contribute zero value, and thus a large phase difference can be observed in Fig. 4.

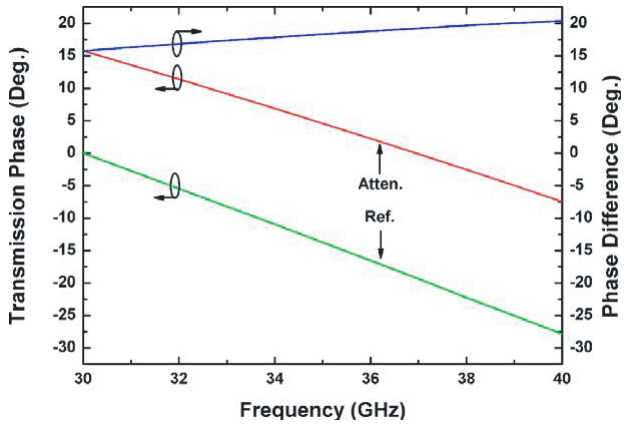

Figure 4. Simulation result of transmission phase and phase difference for 0.5 dB conventional T-Bridge attenuator.

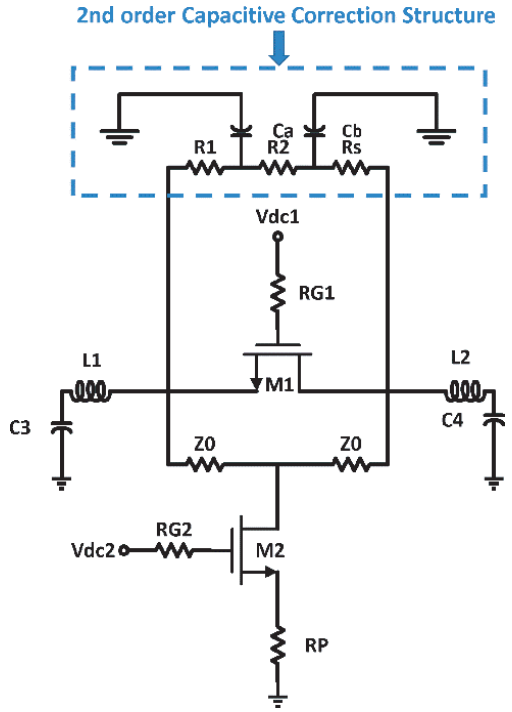

Figure 5. Proposed structure of T bridge-type attenuator.

In order to minimize the transmission phase difference, a low pass filter for its phase lag characteristics can be used to reduce the phase difference at mm-wave band frequencies [1, 13, 16]. By employing the proposed 2nd order capacitive correction structure shown in Fig. 5 with appropriate component values and optimizing the series/shunt switches, not only it serves a phase correction network, but also the required attenuation level is achieved at desired frequency.

The phase difference is observed to be mainly affected by the series capacitor values Ca and Cb of the phase correction structure. And it is observed that as Ca and Cb are changed from 0 to 100 fF for 0.5 dB, the difference is increased as demonstrated in Fig. 6(a). However, by selecting optimum component values of the capacitive phase correction network as well as transistor gate widths, we get the minimal phase difference at the required frequency. This is proved by the simulation result of 0.5 dB attenuator as shown in Fig. 6(b), where the phase difference between reference and attenuation is almost zero.

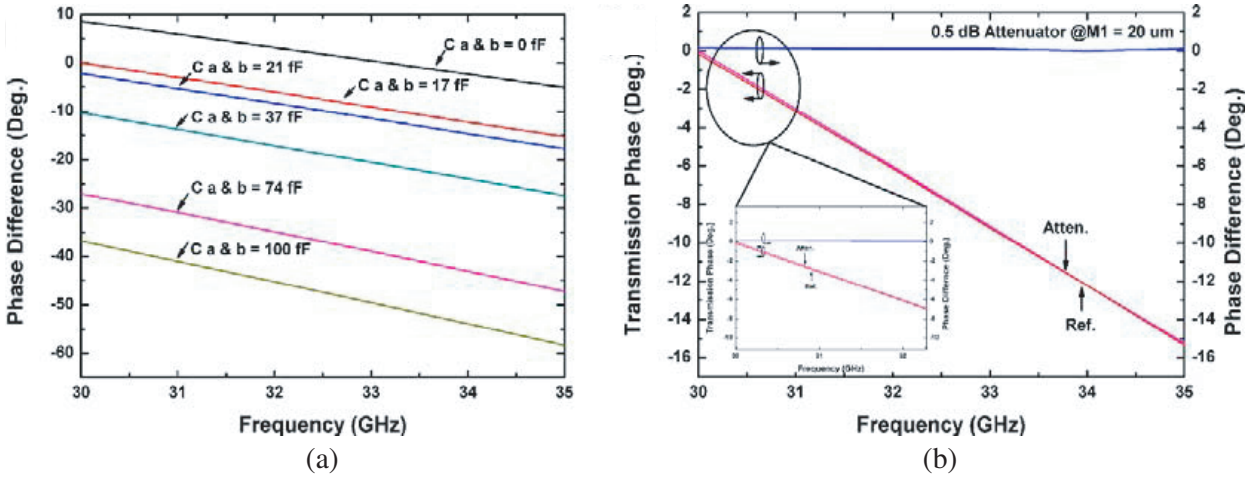

Figure 6. (a) Simulation result of the proposed 0.5 dB T-bridge attenuator. (b) Phase difference of proposed structure under various values of Ca & Cb. Transmission phase and phase difference.

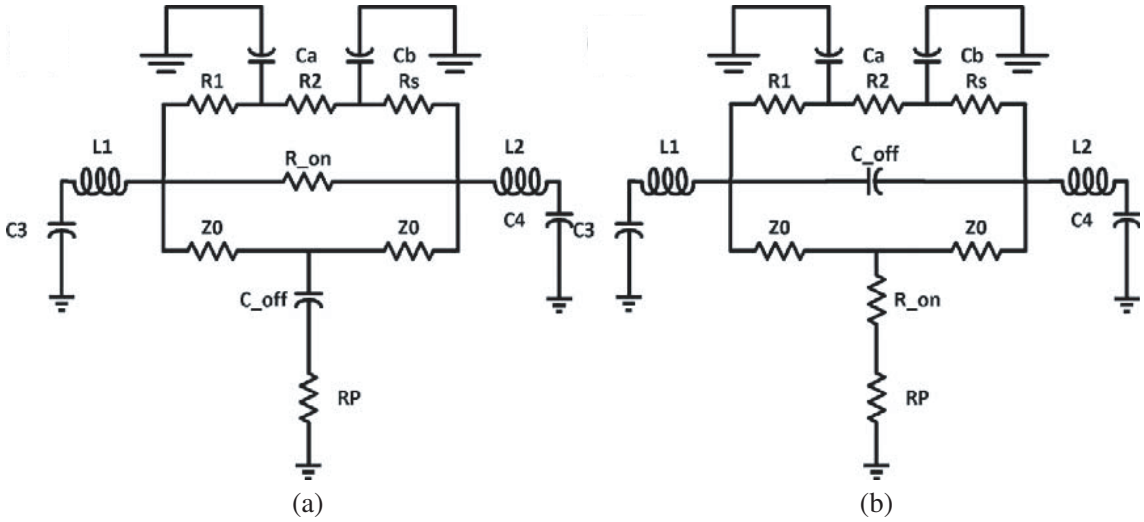

Figure 7. (a) Reference State. (b) Attenuation State.

Reference and attenuation states of the proposed design along with the phase correction network are shown in Figs. 7(a) and (b). The proposed phase correction network can effectively reduce the transmission phase difference of the conventional attenuator due to its phase-lag characteristic of low pass filter. The 2nd order low pass filter network, parallel to resistive network, reduces the attenuation level. In order to avoid this effect, a series resistor R_S is connected in series with 2nd order low pass filter phase correction network [1, 12], as shown in Fig. 7. By choosing the appropriate values for the components in phase correction structure and optimizing the values of switches, not only it serves a phase correction network, but also the required attenuation level is achieved. The proposed model of 4-bit digital step attenuator is simulated in the range of 31–33 GHz, consisting of 16 attenuation states and cascaded in the sequence of 2, 1, 0.5 and 4 dB as shown in Fig. 8.

Figure 8. 4-bit digital step attenuator bit ordering.

Between two attenuator blocks, LC matching network is used to acquire good impedance matching. To achieve the required attenuation and return losses, proper values of resistors, capacitors and the precise gate width of transistors along with optimal bit ordering are essential. When attenuation is changed from reference state to the maximum attenuation state, every bit must have to attain its own attenuation value in order to achieve exact overall attenuation. Furthermore, for a good accuracy of the attenuator result, proper matching of the input and output reflection coefficient is vital.

3. MEASURED RESULTS

Figure 9 shows a layout photograph of the designed 4-bit digital step attenuator including matching network between all blocks. The input and output ports are denoted with RF_IN and RF_OUT, respectively, and control terminals of each attenuator bit are represented with VC1, VC2, VC3 and VC4. This attenuator is fabricated using 0.13 µm SiGe BiCMOS technology with total chip size including pad $1.94 \times 0.4\,\text{mm}^2$. The simulation is performed using Cadence Virtuoso tool and for the enhanced results, EM simulation is performed using Peak View EM tool. The chip is tested with Cascade Microtech GSG probe and Agilent network analyzer. A DC 1.2 V is used for gate control.

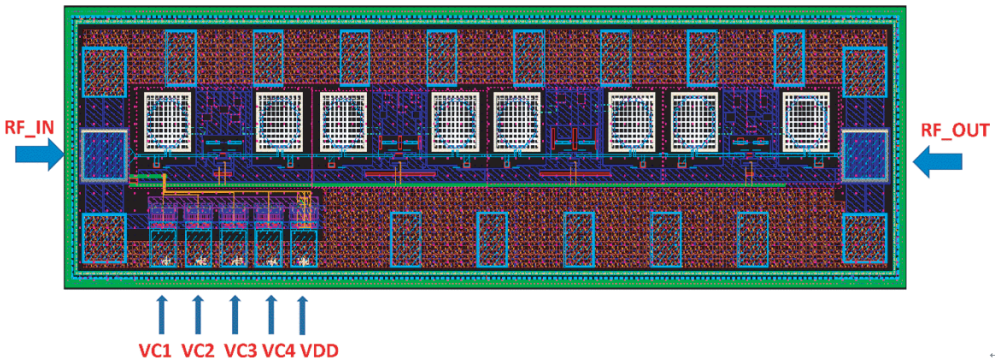

Figure 9. Layout design of proposed attenuator.

The 4-bit digital step attenuator has insertion loss of 19 dB at 31–33 GHz as shown in Fig. 10. In Figs. 11(a), (b) and 12(a), (b), the simulated and measured input and output return losses respectively of all attenuation states with 50 Ω load impedance are shown. The measured input and output return losses are lower than −5.5 dB and −12.7 dB respectively for all attenuation states in the range of 31–33 GHz.

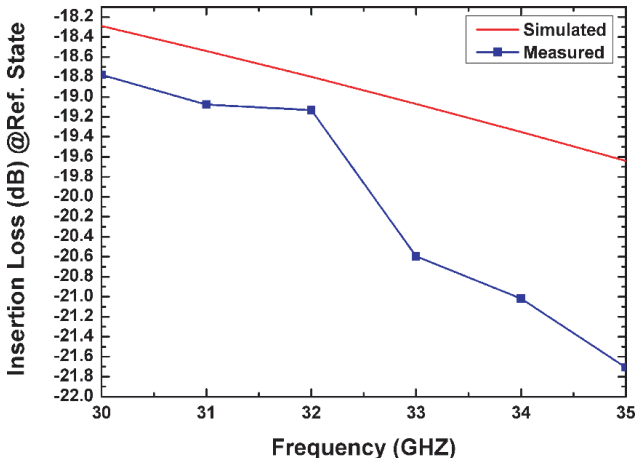

Figure 10. Measured and simulated insertion loss at reference state.

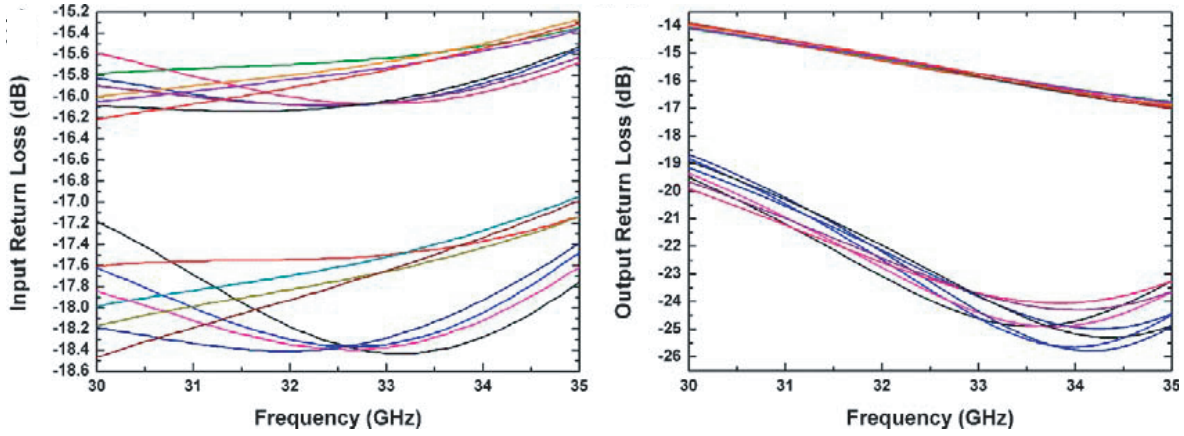

Figure 11. Simulated: Input and output return losses. (a) Input and (b) output return loss.

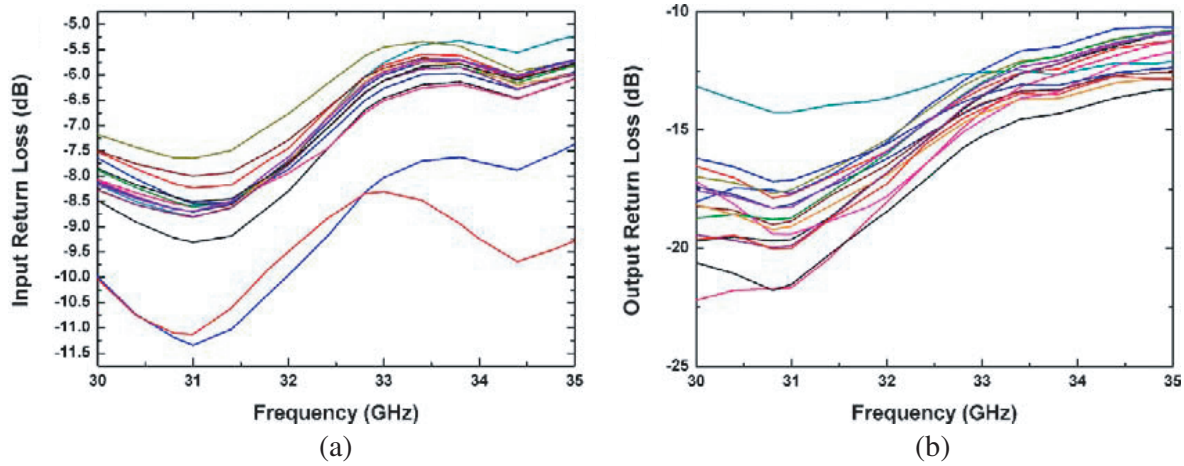

Figure 12. Measured: Input and output return losses. (a) Input and (b) output return loss.

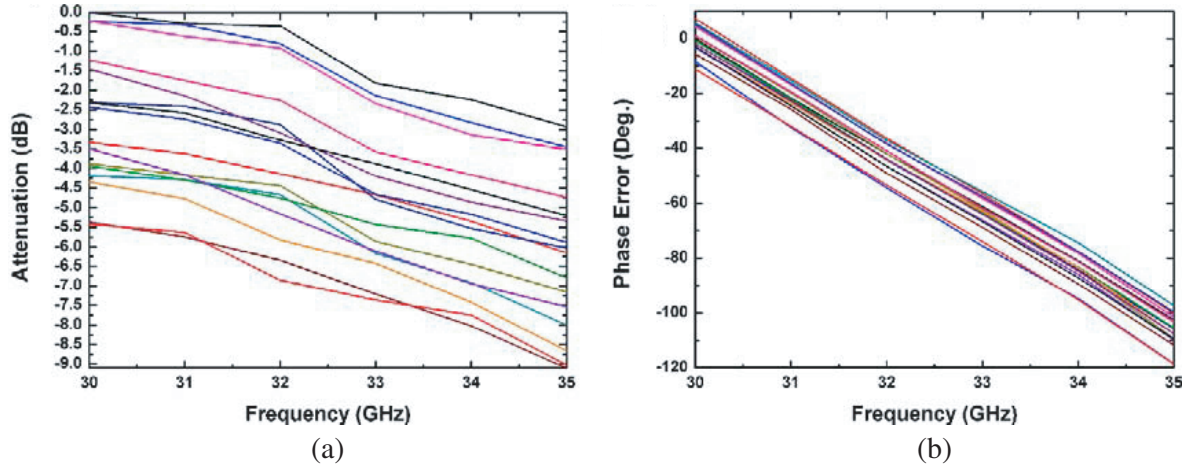

Figure 13. Measured: Relative attenuation and phase plots of 4-bit digital step attenuator. (a) Relative attenuation. (b) Relative phase.

Figure 13(a) shows the normalized attenuation relative to a reference state. The maximum attenuation range is 7.5 ± 0.5 dB in the range of 31–33 GHz. Fig. 13(b) shows the normalized phase relative to the reference state. Figs. 14(a) and (b) show the measured/simulated root mean square (RMS) amplitude and phase error respectively. The root mean square (RMS) amplitude error is 0.8 dB

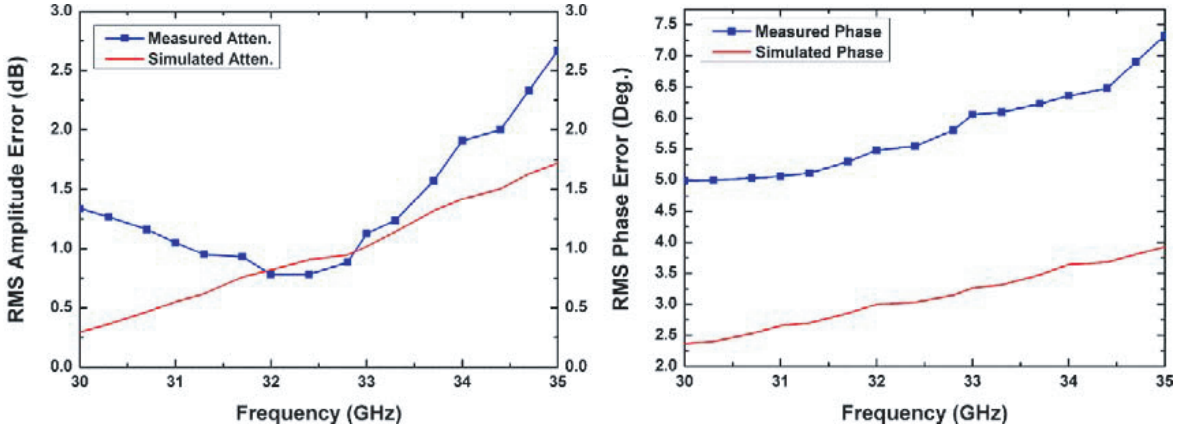

Figure 14. Measured vs simulated RMS plots considering all states. (a) RMS amplitude error and (b) RMS phase error.

Table 1. Comparison of digital step attenuators.

Reference	**[1]**	**[4]**	**[6]**	**[13]**	**[14]**	**[15]**	**[16]**	**This Work**
Frequency (GHz)	8–12 (X-band)	8–15	0.1–20	Dc-18	Dc-20	8.5–11.5	6–12.5	31–33
Attenuation Range (dB)	31.5 (6-Bit) (LSB = 0.5 dB)	23.5 (6-Bit) (LSB = 0.5 dB)	23 (5-Bit) (LSB = 0.75 dB)	27.9 (5-Bit) (LSB = 0.9 dB)	23.5 (4-Bit) (LSB = 0.5 dB)	15.5 (5-Bit) (LSB = 0.5 dB)	16.51 (7-Bit)	7.5 dB (4 bit) LSB = 0.5 dB
Insertion Loss (dB)	9.8–11.3	< 4.5	3–5	3–7	< 5	N/A	< 12.7	19
Return Loss (dB)	> 11	> 8	> 15	> 17	> 13	N/A	> 12	> 12.7
RMS Attenuation Error (dB)	< 0.4	< 0.45	< 1	< 0.5	0.5	N/A	< 0.26	< 0.8
RMS Phase Error (°)	−9–3	N/A	−13–21	0–18	N/A	N/A	2.2–3.5	2.8–5.8
Structure	Switched Pi/T	Switched Pi/T	N/A	N/A	Switched T	Switched T	Switched Pi/T	Switched Bridge-T
Technology	0.18 µm BiCMOS	GaAS	GaAS	GaAS	GaAS	GaAS	0.25 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS
Size (mm^2)	0.67×0.5*	3×2	2.34×1.5	42.4×1.6	2.6×1.6	N/A	0.29*	1.92×0.4

*The Chip size is excluding pads.

at 31–33 GHz while the RMS phase error is less than 5° at 31–33 GHz, and throughout the phase error varies from 2.4° to 7.32° in the range of 30–35 GHz. The measured results show that the proposed 4-bit digital step attenuator can be used for mm-wave band applications within the frequency range of 31–33 GHz for a well-controlled amplitude and phase.

4. COMPARISON WITH OTHER TECHNOLOGY ATTENUATOR

Measured results are compared with recently published work and listed in Table 1. The proposed attenuator has 7.5 dB maximum attenuation, and the highest resolution is 0.5 dB. The chip size of the proposed design is the smallest in size among all the GaAs attenuators listed in Table 1. In addition, the lowest phase variation has been achieved among all the GaAs attenuators. To the best of authors' knowledge, the proposed attenuator is the first attenuator design using 0.13 μm SiGe BiCMOS attenuator for Ka band applications.

5. CONCLUSION

The first Ka band 4-bit digital step attenuator with 2nd order low pass filter as a phase correction network is presented in this paper. Using the proposed method, the problem of large phase difference in conventional T-bridge attenuator at mm-wave frequency is alleviated. An optimal performance is obtained by an appropriate combination of all bits. The 4-bit digital step attenuator employing 2nd order phase correction structure is fabricated in 0.13 μm SiGe BiCMOS technology with maximum attenuation of 7.5 dB over 31–33 GHz, and the highest resolution bit is 0.5 dB. The input and output return losses are lower than −5.5 dB and −12.7 dB in the range of 31–33 GHz, respectively. The insertion loss is 19 dB for the said frequency range. The attenuator with phase correction structure shows the RMS amplitude/phase errorless compared to 0.8 dB/2.8° to 5.8° over 31–33 GHz. Die area is $1.92 \times 0.4\,\text{mm}^2$.

Results show that the attenuator is competitive with all GaAs attenuators listed in Table 1 due to its phase accuracy, high band operation and compact chip size. The proposed 4-bit digital step attenuator can be used for Ka band applications.

ACKNOWLEDGMENT

This project was funded by CAS-TWAS President's Fellowship for Muhammad Masood Sarfraz (Student ID: 2013A8011207116). The authors would like to thank the Global Foundries for the fabrication and Lorentz Solution for Peak View EM Design support. The authors also acknowledge the National Science Foundation of China (grant number: 61574165) for financial support of this work.

REFERENCES

1. Ku, B. H. and S. Hong, "6-bit CMOS digital attenuators with low phase variations for X-band phased-array systems," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 58, No. 7, 1651–1663, 2010.
2. Sun, P., "Analysis of phase variation of CMOS digital attenuator," *Electronics Letters*, Vol. 50, No. 25, 1912–1914, 2014.
3. Goyal, U. and A. Kumar, *Design and Development of an S-band 6 bit MMIC Attenuator with Low Insertion Loss*, 157–159, 2014.
4. Ciccognani, W., et al., "Compensating digital attenuator differential phase shift," *2008 14th Conference on Microwave Techniques*, 2008.
5. Hajimiri, A., "mm-wave silicon ICs: Challenges and opportunities," *2007 IEEE Custom Integrated Circuits Conference*, 2007.
6. Dogan, H., R. G. Meyer, and A. M. Niknejad, "Analysis and design of RF CMOS attenuators," *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 10, 2269–2283, 2008.
7. Sjogren, L., et al., "A low phase-error 44-GHz HEMT attenuator," *IEEE Microwave and Guided Wave Letters*, Vol. 8, No. 5, 194–195, 1998.

8. Hunton, J. K. and A. G. Ryals, "Microwave variable attenuators and modulators using PIN diodes," *IRE Transactions on Microwave Theory and Techniques*, Vol. 10, No. 4, 262–273, 1962.
9. Min, B. W. and G. M. Rebeiz, "A 10–50-GHz CMOS distributed step attenuator with low loss and low phase imbalance," *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 11, 2547–2554, 2007.
10. Bae, J., J. Lee, and C. Ngyyen, "A 10–67-GHz CMOS dual-function switching attenuator with improved flatness and large attenuation range," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 61, No. 12, 4118–4129, 2013.
11. Razavi, B., *Design of Analog CMOS Circuit Design*, 2nd Edition, Oxfard University Press, New York, 2004.
12. Zhang, Y., et al., "A 5-bit lumped 0.18-μm CMOS step attenuator with low insertion loss and low phase distortion in 3–22 GHz applications," *Microelectronics Journal*, Vol. 45, No. 4, 468–476, 2014.
13. Kaunisto, R., et al., "A linear-control wide-band CMOS attenuator," *ISCAS 2001, The 2001 IEEE International Symposium on Circuits and Systems (Cat. No. 01CH37196)*, 2001.
14. Ju, I., Y. S. Noh, and I. B. Yom, "Ultra broadband DC to 40 GHz 5-bit pHEMT MMIC digital attenuator," *European Microwave Conference*, Vol. 2, 4, 2005.
15. Kang, D.-W., et al., "Ku-band MMIC phase shifter using a parallel resonator with 0.18-μm CMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 54, No. 1, 294–301, 2006.
16. Davulcu, M., et al., "7-bit SiGe-BiCMOS step attenuator for X-band phased-array RADAR applications," *IEEE Microwave and Wireless Components Letters*, Vol. 26, No. 8, 598–600, 2016.