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Reduction of PCB PDN Impedance and Radiated Emissions Using a Hybrid Technique with Absorbing Materials and Decoupling Capacitors

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Abstract—In this paper, we present an approach to reduce the cavity resonant edge effects in printed circuit boards (PCBs) and semiconductor packages. Power supply noise, in the form of fast changing currents (di/dt), traverses the power-return paths of PCBs and semiconductor packages using power vias. The cavity effects produce considerable level of noise along the edges of PCB and integrated circuit (IC) package power planes due to signal coupling between vias and reflection from PCB edges with transient currents. The cavity effects also amplify the electromagnetic radiation from PCB edges, which are major sources of EMI/EMC problems in electronic devices. By using absorbing material and decoupling capacitors (de-caps) on power distribution networks (PDNs), we observe considerable mitigation in impedance noise, signal noise and electromagnetic interference/compatibility (EMI/EMC) issues caused by the cavity effects. In particular, simulation results show notable reduction of upper peak (anti-resonant) impedance noise and reduction in radiated emissions by as much as 20 dB. This article presents a comparative case-study using various models (Section 3) and report on their effectiveness to reduce the cavity effects. The models are listed as (1) "Original" model, (2) "Absorbing material along the edge" model, (3) "MURATA based De-cap only" model and (4) "Absorbing material along the edge w/De-cap" model. The used capacitance ranges between 0.1 μF and 22 μF. The ESR and ESL range between 2 mOhm–20 mOhm and 238 pH–368 pH, respectively. Conclusively, we learn by adding absorbing material along the PCB edges with a few decoupling capacitors. The PDN impedance noise is improved, and EMI issues in PCBs and semiconductor packages suppress the cavity effects.

1. INTRODUCTION

Passive interconnects are commonly used to help improve electrical performances of high speed digital systems and power delivery networks (PDN) for several decades and have been shown to impact each other [1–13]. For instance, the PDN impedance has significant influence on the signal, power integrity, and EMI of electronic systems. The reduction of radiated field emissions and the suppression of power supply noises are leading challenges of signal and power integrity in the development of digital systems. The use of metal enclosures and decoupling capacitors on printed circuit boards (PCBs) and semiconductor packages are conventional solutions. However, as the clocking frequency and signaling edge rate rise, EMI/EMC and power supply noise issues become more severe and difficult to solve in multi-layer interconnect structures due to fast transient currents (di/dt) [1, 2]. The power delivery network and ground plane act as physical networks that contain resistive and reactive (inductive and capacitive) properties which become more severe at higher gigahertz frequencies. Furthermore, the cables attached to the system including some metallic components on board could potentially act as antenna sources and radiate emissions. The relationship between electromagnetic interference and signal

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integrity expands into power integrity domain. Therefore, the EMI/EMC and noise coupled to signal traces can be substantially mitigated by suppressing the noise found in PDN.

In today's high speed and high density PCB designs, signal routing and vias (signal, power and ground) create discontinuity return paths (DRPs) throughout the power-ground planes. This is due to non-ideal return paths in signal traces and via structures [1–13]. DRPs form a strong electric-field which propagates along the edges of the cavity plane. Current passing thru DRPs creates a considerable amount of voltage fluctuations at the reference (ground) and power planes and via structures. An electric field is inherently produced as a result of the voltage fluctuations where noise is radiated along the PCB edge. This is known as cavity resonant edge effect (CREE).

EMI/EMC, signal and power integrity are all tightly related to each other, particularly now as operating frequencies continue to rise. If we can reduce resonant impedance amplitude, then we will effectively lower behavior modes (*TE* and *TM* modes) along PCB edges [1–11]. We employ the use of absorption material to mitigate cavity resonant effect and PDN impedance noise from power-ground planes. Absorbing materials have been widely used. Some of the areas include the defense industry, in traditional microwave component designs, and in conventional EMC/EMI test and control environments [14–33]. Recently, novel applications of microwave absorbing materials in computer system designs have been investigated [34–40].

In this study, we develop a technique by placing absorbing material along the cavity edge and decoupling capacitor (de-cap) models based on capacitance, ESR (equivalent series resistance) and ESL (equivalent series inductance) properties extracted from MURATA capacitor models [41]. We explore the use of the following component items for this study:

(a) Absorbing material is applied on the PCB peripheral edge. If there are gaps in power or ground plane on PCB surface layer, the absorbing material can also be applied onto these gaps. The electromagnetic energy associated with the cavity resonance is absorbed and the PDN impedance noise for a band of frequencies is dampened.

(b) Decoupling capacitors are populated on the surface layer of PCB where the impedance resonant characteristics are modulated with absorbing material. A reduction in impedance magnitude is observed as a result of increasing the capacitor value.

The use of ceramic decoupling capacitors helps decouple noise from the power distributed network (PDN). However, there are some restrictions with decoupling capacitor as the sole solution. First, the bandwidth of a single de-cap is usually narrow. In order to achieve broadband suppression of PDN noise, decoupling capacitors of different case-size and value may be needed. Second, the parasitic series inductance and resistance from the capacitor can possibly have an adverse effect on the power integrity.

The proposed method is a hybrid technique which is further explained in the next section to follow. Since the PDN of power/ground plane cavity is a passive LTI system, we combine (a) and (b) in the model. The hybrid technique has a variety of advantages compared to conventional methods.

(c) We add shorting vias which push cavity resonances to higher frequencies. However, the feasibility of adding shorting vias is limited by board area and the interference of internal routing. Furthermore, shorting vias cannot "reduce" the energy of resonance even with dense count of shorting vias.

(d) Applying metal enclosures on a chassis or components can shield against radiated field emissions, most of which are from the PCB and package edge. However, metal enclosures have several limitations: i). it can only mitigate the external radiation issues, not a solution for suppression the power/ground noise. ii). mechanical restriction for placing external enclosures. iii). the metal components such as hint sink can act as antenna structures and can become other sources of radiated emissions. iv). metal enclosures may not be helpful for the open-chassis requirements in EMC testing

The paper is organized as follows. In Section 2, we briefly discuss the hybrid model methodology that we used for the case-study. In Section 3, we present an analysis on each case-study and what is done to reduce PDN impedance. In section 4, we discuss the results of the radiated emissions suppression using different absorption material. Finally, in Section 5, we conclude our study with a summary of the work.

2. METHODOLOGY

In this section, we discuss the method for suppressing cavity resonant edge effects and use a hybrid approach by placing absorbing materials along the PCB edge. De-caps are added later to further suppress cavity resonant edge effects.

2.1. Power-Ground Cavity Resonant Plane with Ports

The model shown in Fig. 1 is a simple cavity plane separated by dielectric material FR-4 with permittivity of 4.4, loss tangent of 0.02, height of 40 mils, and x-y dimensions of 1×5 inches. The model contains 5 impedance ports distributed throughout the model as shown in Fig. 1.

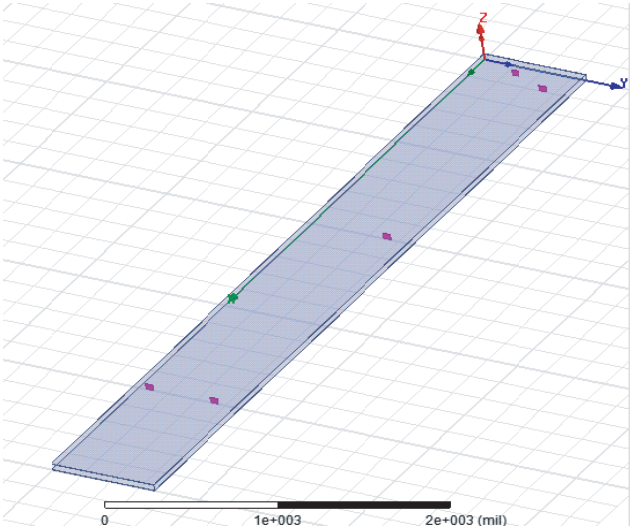


Figure 1. Original power-ground plane cavity model without absorbing material (red pieces are ports) constructed using 3-D field solver (HFSS).

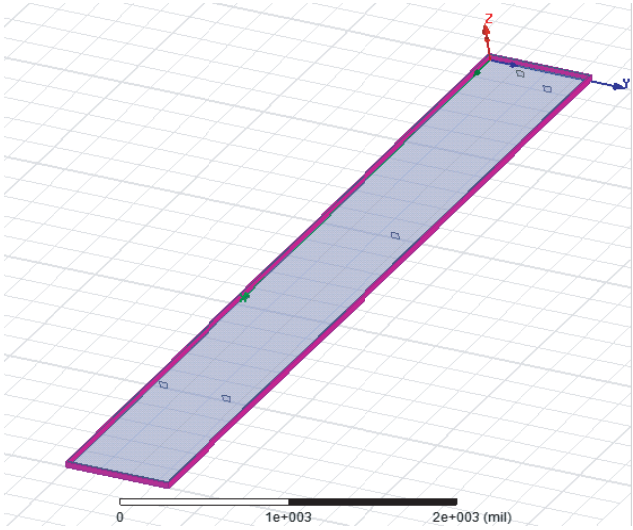


Figure 2. New power-ground plane cavity model with absorbing material attached to the edge (red is absorbing material).

2.2. Absorption Material Placed along the Edges

The model shown in Fig. 2 is the proposed application with absorbing material attached to the cavity edge. The absorption material can be seen in red wrapped around PCB edge of Fig. 2. There are different ways to place the absorbing material along the PCB edge for practical implementation. For instance, a few types of adhesive to secure the absorbing material include pasting, glue, tape, epoxies and acrylic adhesives.

2.3. Combination of Absorbing Material and De-Cap

A hybrid technique that combines absorbing material and high frequency de-cap is shown in Fig. 3. By combining the suppression strength of absorbing material and high frequency de-caps, the hybrid technique is capable of minimizing broadband noises with few SMT de-caps that would normally occupy motherboard space. The field radiations of EMC and EMI are substantially suppressed from the PCB edge. Power integrity is also improved with the use of hybrid technique. Therefore, the hybrid technique offers a comprehensive solution to resolve signal and power integrity issues along with field radiation from EMI/EMC. Fig. 3 shows a model of the proposed hybrid technique. The de-cap value that we use ranges from 0.1 µF and 22 µF.

Note that in the paper we use two steps in the simulation verification: First step, we create 3D full wave models of PDN structures in HFSS. The full wave models are simulated using HFSS where S-parameters are extracted. Fig. 3 shows arrows pointing to the decoupling capacitor locations. Second

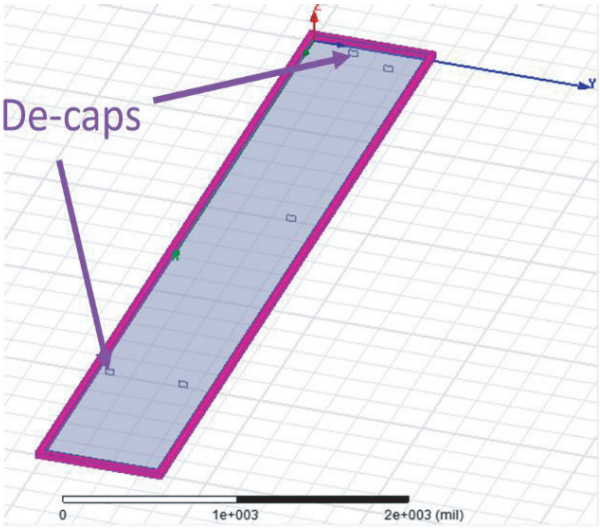


Figure 3. New power-ground plane cavity model with absorbing material placed along the edge (in red) and de-caps highlighted by arrow.

step, once the S-parameters are generated, they are imported into the ADS tool where a circuit model with high-frequency de-caps is created.

3. APPLICATIONS TO REDUCE PDN IMPEDANCE CAUSED BY CAVITY RESONANT EDGE EFFECTS FOR SIGNAL AND POWER INTEGRITY

Three different case studies are presented in this section. We benchmark how effective absorbing material is by itself and then combine high frequency decoupling capacitor models. The characteristics of the de-cap model used in our study is derived from MURATA's Monolithic Ceramic Capacitor (MLCC) product catalog [39]. We present two different cavity models: (1), a simple power-ground PCB cavity plane model and (2), a relatively complex model that includes multiple P/G-vias connected to two pairs of power-ground planes.

Note:

(i) Using 3D full wave simulations, we validate the invention for

(ii) Different types of commercial absorbers, such as MT-30, SB1001, and WXA are used as examples. Results show all works well.

(iii) Vary the thickness of absorbing material. Results show that thicker absorber can have stronger reduction of cavity resonance. 10 mils already give decent suppression.

(iv) We explore some ideas to secure absorbing material along the PCB edge. For practical implementation, we list a few ways to secure the placement of absorbing material along the edge, including paste, glue, tape and paint.

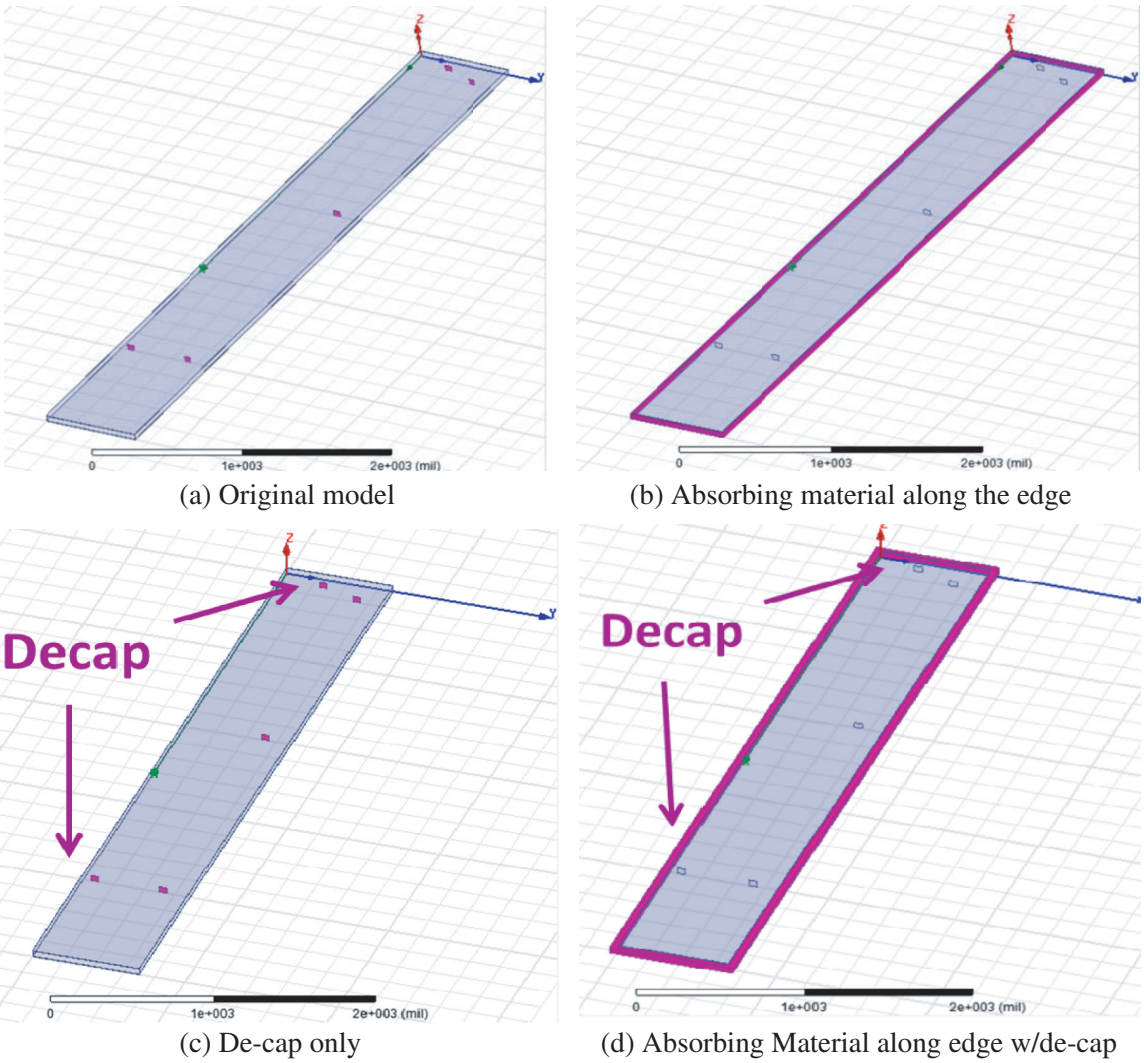
(v) We also study the effects of DC resistance of absorbing material on the PDN. Absorbing material along the edge will not cause DC voltage degradation, because, i) the DC resistance of PDN is much smaller than the equivalent DC resistance of absorbing material, and ii) the absorbing material along the edge is (NOT series) connected to PDN in parallel.

(vi) We investigate the performance of the invention for different cases with or without gaps on the power plane. The results show the invention works for all cases.

However, in order to make the paper short, those results and information are not included in this paper.

3.1. Case 1: Performance without Gap on the Power Plane

The models shown in Figs. (4a)–(4d) are all simple cavity plane separated by dielectric material FR-4 with permittivity of 4.4, loss tangent of 0.02, height of 40 mils, and x-y dimensions of 1×5 inches. The models are constructed using an EM field solver (e.g., HFSS) and contain same 5 ports distributed throughout. There are two pairs of ports, one pair placed on one end and the other pair placed on the opposite end of the model. The fifth port (port 5) is placed at the center. The original model in Fig. 4(a) contains no absorbing material. Fig. 4(b) shows original cavity model with absorbing material wrapped around all 4 sides of the cavity plane. Fig. 4(c) shows the original model only using MURATA de-caps. Fig. 4(d) is the proposed hybrid case with absorbing material + MURATA de-caps.

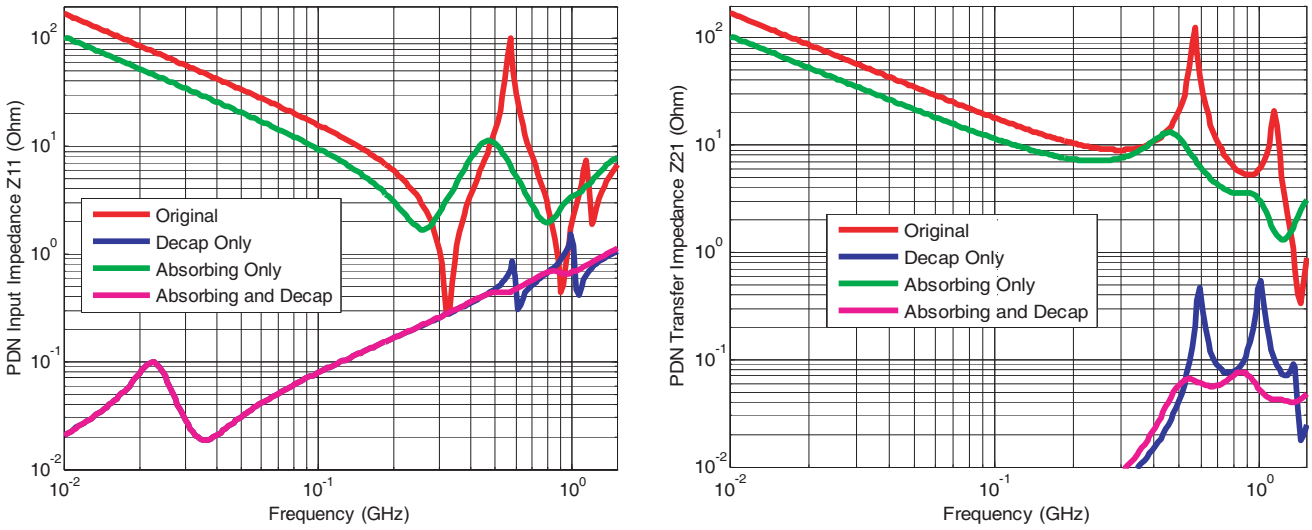


(a) Original model (b) Absorbing material along the edge

(c) De-cap only (d) Absorbing Material along edge w/de-cap

Figure 4. HFSS models of two layers cavity of power/ground planes with no gaps: (a) Original power-ground cavity model contains 5 ports (ports are colored red), (b) cavity model with absorbing material wrapped along the side walls, (c) cavity model with MURATA de-caps only, (d) cavity model with absorbing material and MURATA de-caps.

The model shown in Fig. 4(b) only contains absorbing material along the edge. In practical implementation, there are different schemes of how absorbing material can be placed along the edge, such as pasting, glue, tape, and painting. The simulation results of the models in Figs. 4(a)–4(d) are plotted in Figs. 5(a) and (b) with analysis.



(a) Self-Impedance: Z_{11} (b) Transfer Impedance: Z_{21}

Figure 5. Self-impedance and transfer impedance plots for models in Fig. 4. Each figure contains 4 curves for Z_{11} (self-impedance) and Z_{21} (transfer impedance). Red — The impedance curve of the original structure, Blue — the impedance curve using MURATA de-cap models only, Green — the impedance curve using absorbing material only, and Magenta — finally the proposed hybrid technique combining absorbing material + MURATA de-cap models.

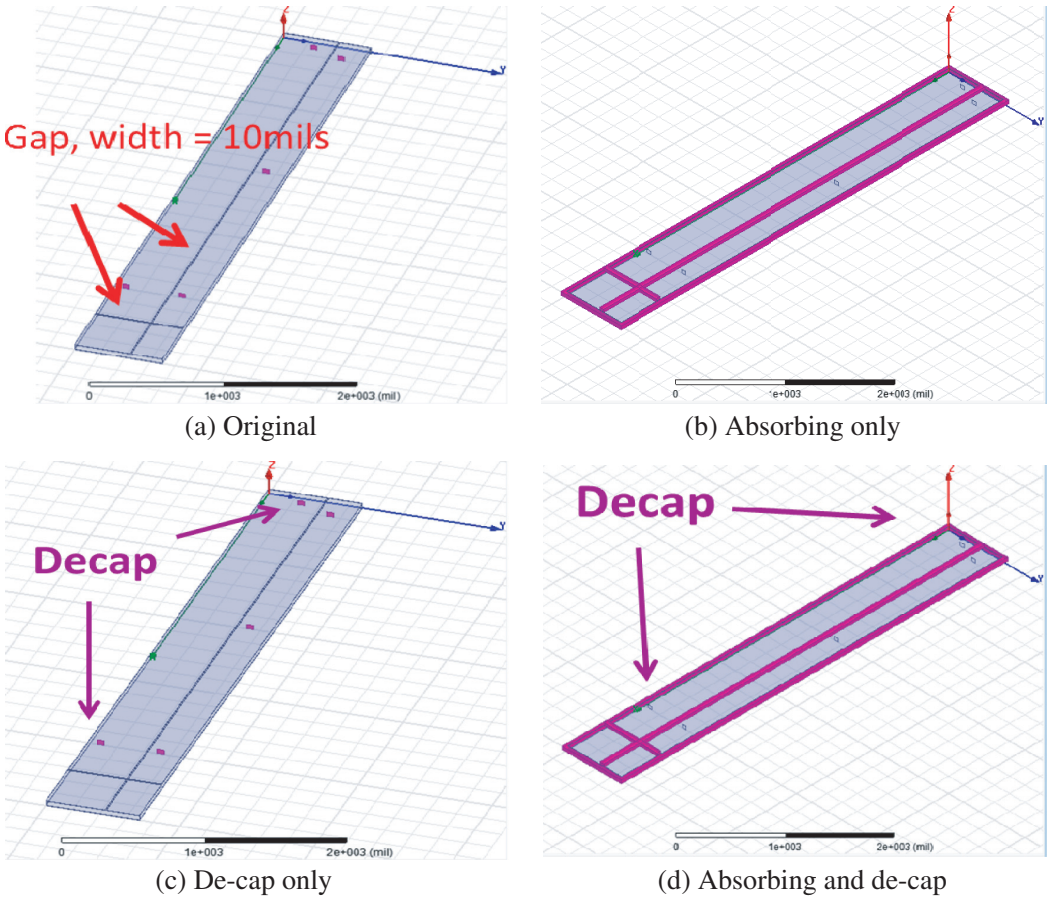
When de-caps are used exclusively (e.g., MURATA de-caps), they help lower impedance at sub-GHz range. Yet, de-caps alone cannot lower the sharp anti-resonant peaks which represent concentrated energy at a particular resonant frequency point. As shown in Fig. 5, the de-cap models used in this study show effectiveness between 100 kHz and 1 MHz. The capacitor values used are 0.1 μF and 22 μF capacitors. The ESR and ESL of the 0.1 μF are 20 mOhm and 238 pH, respectively. For the 22 μF, ESR and ESL are 2 mOhm and 368 pH. The decoupling capacitors are placed along the PCB edge to target cavity resonant edge effects and PDN noise most effectively. When we combine the de-cap models and absorbing material, we obtain the following impedance results shown in Fig. 5 where the curve lines are represented in magenta color. The strong dampening attributes of the absorbing material along with MURATA de-caps reduce the sharp resonant peaks. If more de-caps are used instead of absorbing material, the sharp upper peaks of the impedance may potentially shift to either lower or higher frequencies. We note that absorbing material is a broadband solution for frequencies up to 40 GHz.

3.2. Case 2: Performance with Gaps in Power Plane

In Fig. 6, the HFSS models show power plane with 10 mils of spacing. Fig. 6(a) shows original model with 10 mils spacing. Fig. 6(b) shows absorbing material along the edges and between the power plane spacing. Fig. 6(c) has MURATA de-caps distributed across the PDN cavity design, and Fig. 6(d) shows in essence a hybrid implementation.

There is a gap on the surface of the power plane. The width of gap is 10 mils. Simulating a power plane with spacing on the surface is practical for PCBs containing different power shapes distributed along the motherboard. The purpose of adding a gap to the power plane model is to eventually get to a realistic power plane model. We are also interested in seeing the impedance properties of the PDN while progressively adding more PDN structures to the model (e.g., power-ground vias) and observing how the PDN impedance property change.

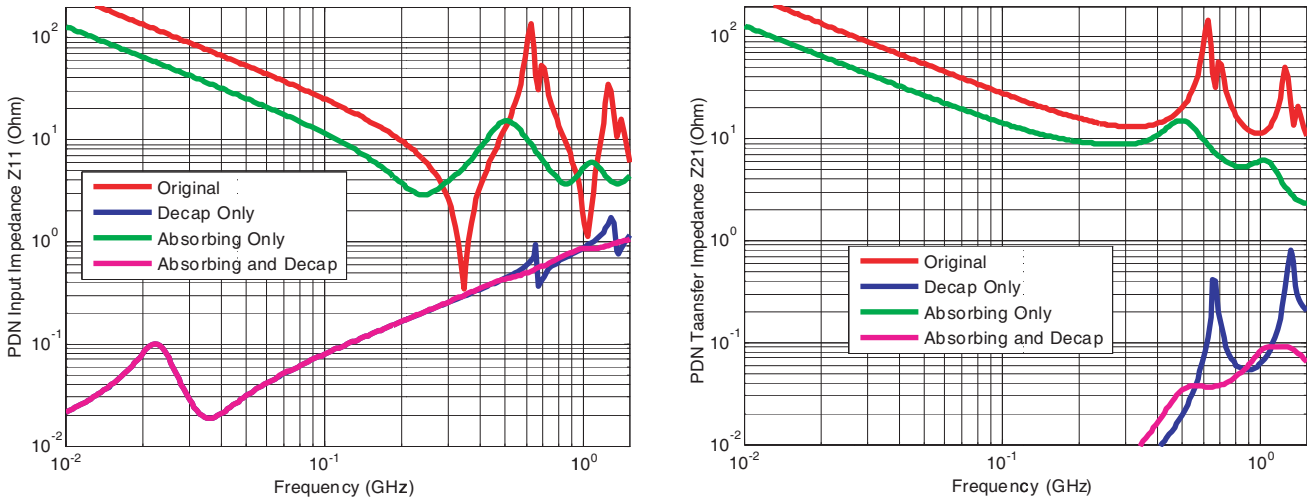
Figures 7(a) and 7(b) show several self-impedance and transfer impedance plots, respectively. Each figure contains 4 curves for Z_{11} (self-impedance) and Z_{21} (transfer impedance). Red — the impedance curve of the original structure, Blue — the impedance curve using MURATA de-cap models only, Green — the impedance curve using absorbing material only and Magenta — finally the proposed hybrid



(a) Original (b) Absorbing only

(c) De-cap only (d) Absorbing and de-cap

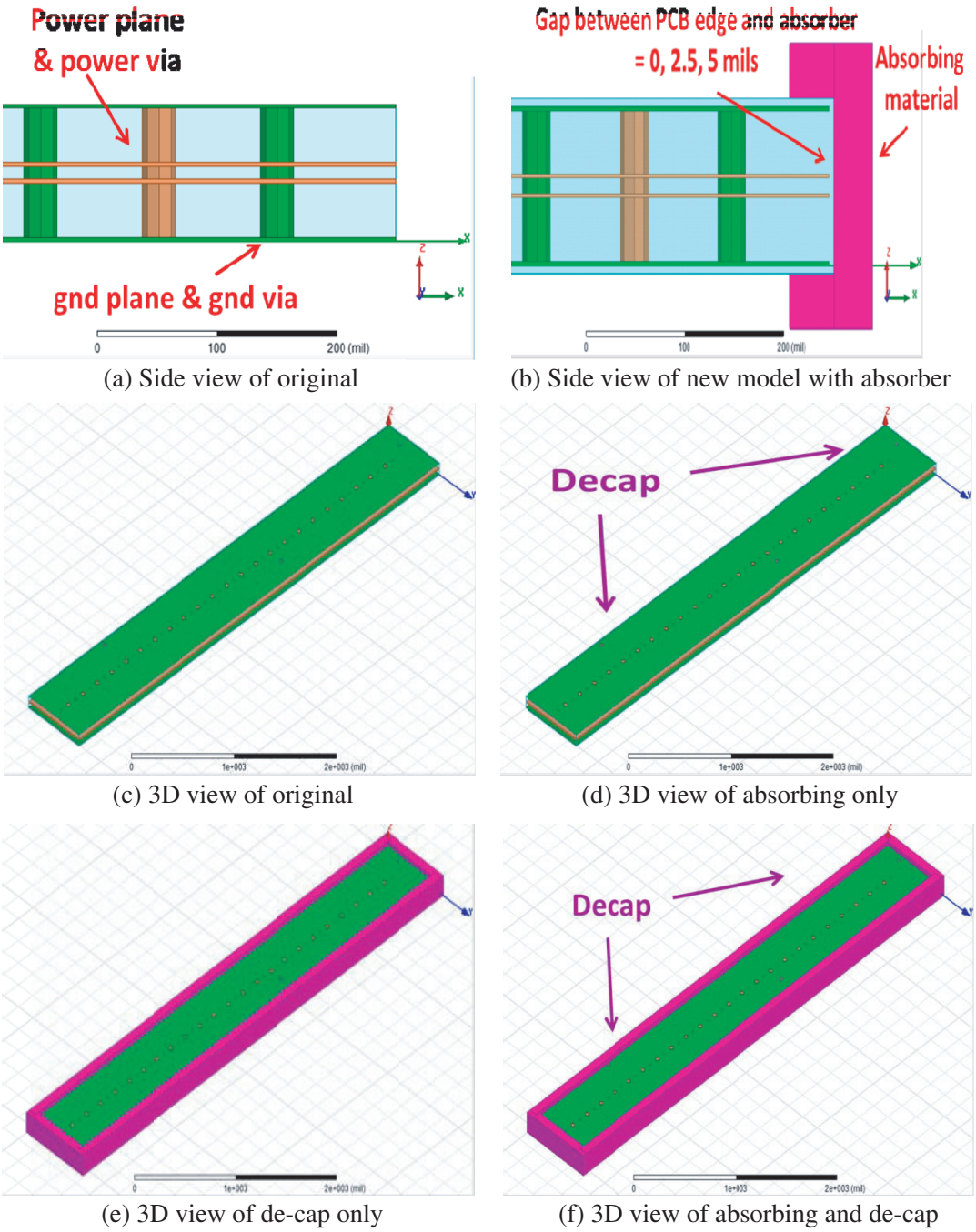
Figure 6. 3D HFSS models for PDN cavity with gap in the power plane: (a) original model, (b) model with absorbing material, (c) model with de-caps, (d) model with both absorbing material and de-caps.



(a) Self-Impedance (Z_{11}) (b) Transfer Impedance (Z_{21})

Figure 7. Compare different models for PDN cavity impedance: (a) input impedance Z_{11}, (b) transfer impedance Z_{21}.

technique combining absorbing material + MURATA de-cap models. The simulation results show that when de-caps are used exclusively (e.g., MURATA de-caps), they help lower impedance at sub-GHz range. In Figs. 7(a) and 7(b), we observe comparable self-impedance results between two models, and they are the "De-cap only" model and "Absorbing and De-cap" model. This can be due to material property of the absorbing material that we use in Fig. 7. The capacitor values used are 0.1 μF and 22 μF. The ESR and ESL of the 0.1 μF capacitor are 20 mOhm and 238 pH, respectively. For the 22 μF one,



(a) Side view of original

(b) Side view of new model with absorber

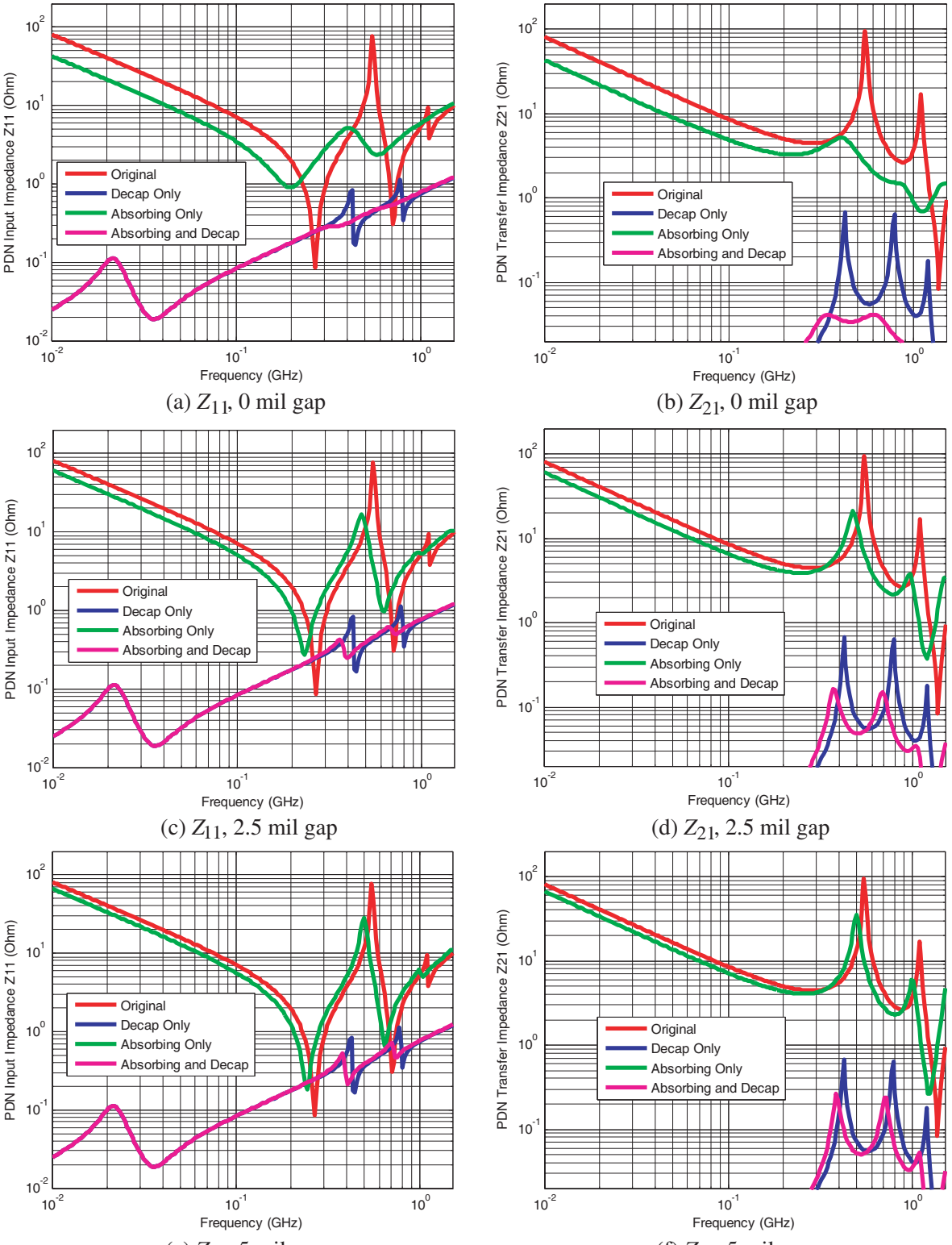
(c) 3D view of original

(d) 3D view of absorbing only

(e) 3D view of de-cap only

(f) 3D view of absorbing and de-cap

Figure 8. HFSS models for multilayer Layers with ground/power vias, gaps between absorbing material and PCB edge: (a) top view of original model, (b) top view of model with absorbing material along edge, (c) 3D view of original model, (d) 3D view of model with absorbing material along edge, (e) 3D view of model with de-cap, (f) 3D view of model with de-cap and absorbing material along edge.



(a) Z_{11}, 0 mil gap

(b) Z_{21}, 0 mil gap

(c) Z_{11}, 2.5 mil gap

(d) Z_{21}, 2.5 mil gap

(e) Z_{11}, 5 mil gap

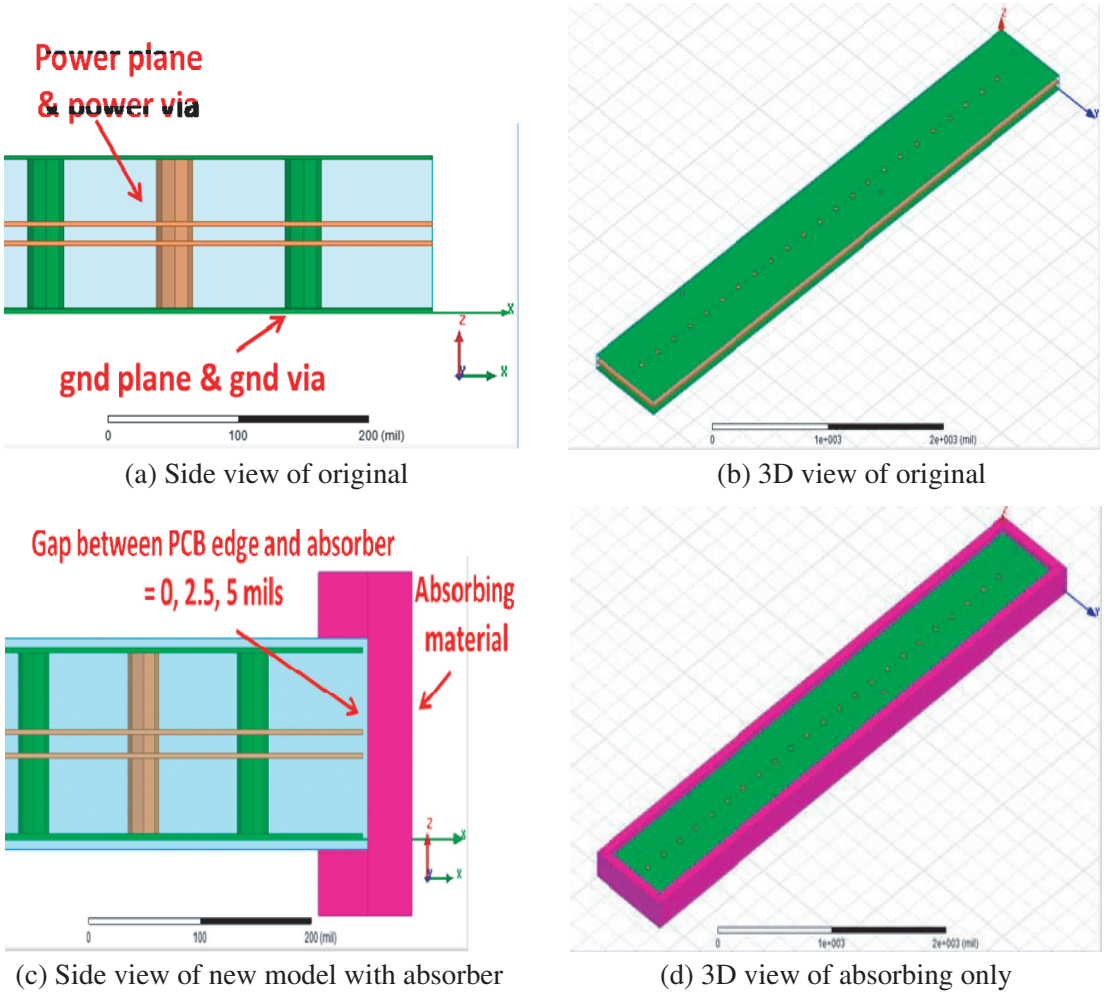
(f) Z_{21}, 5 mil gap

Figure 9. PDN Impedance: (a) Z_{11} for gap = 0 mil, (b) Z_{21} for gap = 0 mil, (c) Z_{11} for gap = 2.5 mils, (d) Z_{21} for gap = 2.5 mils, (e) Z_{11} for gap = 5 mils.

ESR and ESL are 2 mOhm and 368 pH. The decoupling capacitors are placed along the PCB edge to target cavity resonant edge effects and PDN noise. When we combine the de-cap models and absorbing material, we obtain the following impedance results where the curve lines are represented in magenta color. The strong dampening traits of the absorbing material along with MURATA de-caps help target the sharp resonant peaks directly. If more de-caps are used instead of absorbing material, the sharp upper peaks of the impedance may potentially shift to either lower or higher frequencies. It should be noted that absorbing material is a broadband solution for frequencies up to 40 GHz.

3.3. Case 3: Performance with Gaps between Absorbing Material and PCB Edge

As shown in Fig. 8, case 3 is a comprehensive power plane model of case 1 and case 2 with the insertion of power-ground vias. The power-ground vias are 50 mils in height and 2 mils in diameter. The MURATA de-caps are placed near the power vias. The analysis of the impedance property for a power plane model with P/G vias and different spacing sizes is shown in Figs. 9(c)–9(e). By varying the gap sizes, we observe that the impedance upper peaks are slightly reduced relative to the results in Fig. 9(a) and Fig. 9(b) with no gaps. In order to further lower the impedance in Figs. 9(c)–9(e), we will need to increase the thickness of the absorbing material. By doing so, we will obtain similar results to Figs. 9(a) and 9(b).



(a) Side view of original

(b) 3D view of original

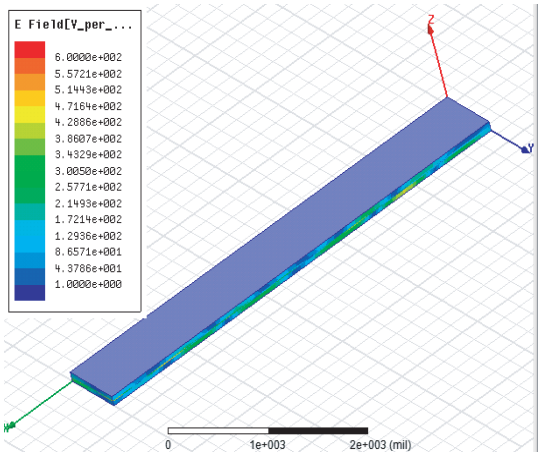
(c) Side view of new model with absorber

(d) 3D view of absorbing only

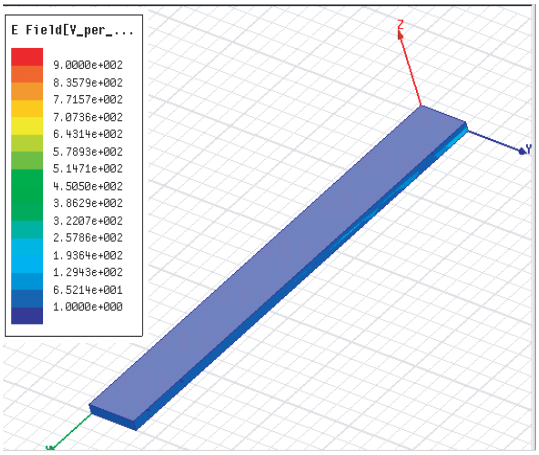
Figure 10. HFSS models for multilayer Layers with ground/power vias, gaps between absorbing material and PCB edge: (a) top view of original model, (b) 3D view of original model, (c) top view of model with absorbing material along edge, (d) 3D view of model with absorbing material along edge.

3.4. Applications to Suppress Radiated Emissions Caused by Cavity Resonances for EMC/EMI

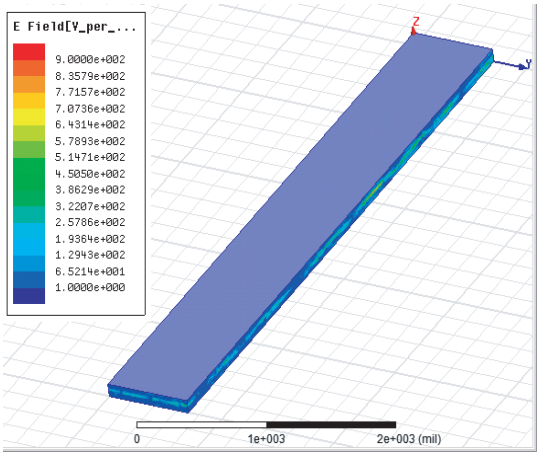
In previous sections, we have shown the PDN impedance results for the present method. In this section, we show radiated emission results for different gap spacings between the absorber and the edge. In practical manufacturing, there can be small gaps around 0.5 to 2 mils between absorbers and edges. It is important to check if the absorbing materials can still work for the cases with such gaps. Figs. 10(a), 10(b) and 10(c) show the HFSS Models with different gap spacings between the absorber and the PCB edge. Figs. 10(a) and 10(b) are the side view and 3D view for the original model. Figs. 10(c) and 10(d) are the side view and 3D view for the model with absorbing material along the edge. There are gaps between the absorbing material layers and the PCB edge. In Figs. 11(a), 11(b) and 11(c), we compare the surface electric fields along the edge. It can be seen that the absorbing material significantly suppress the surface electric field even there are gaps. Since the surface E-field is equivalent antenna sources in EMC emission problems, the absorbing material can reduce the emission fields from PCB or packages. The simulation frequency is 5 GHz, and the absorbing material used in the simulations is SB1001. In Figs. 12(a), 12(b) and 12(c), we compare the radiation E-fields. Results demonstrate that the absorbing material significantly reduces the radiation E-field by more than one order (10 times). Thus, in dB scale of radiation power, the absorbing material will make more than 20 dB suppression in emission. This



(a) Original, E-field along edge

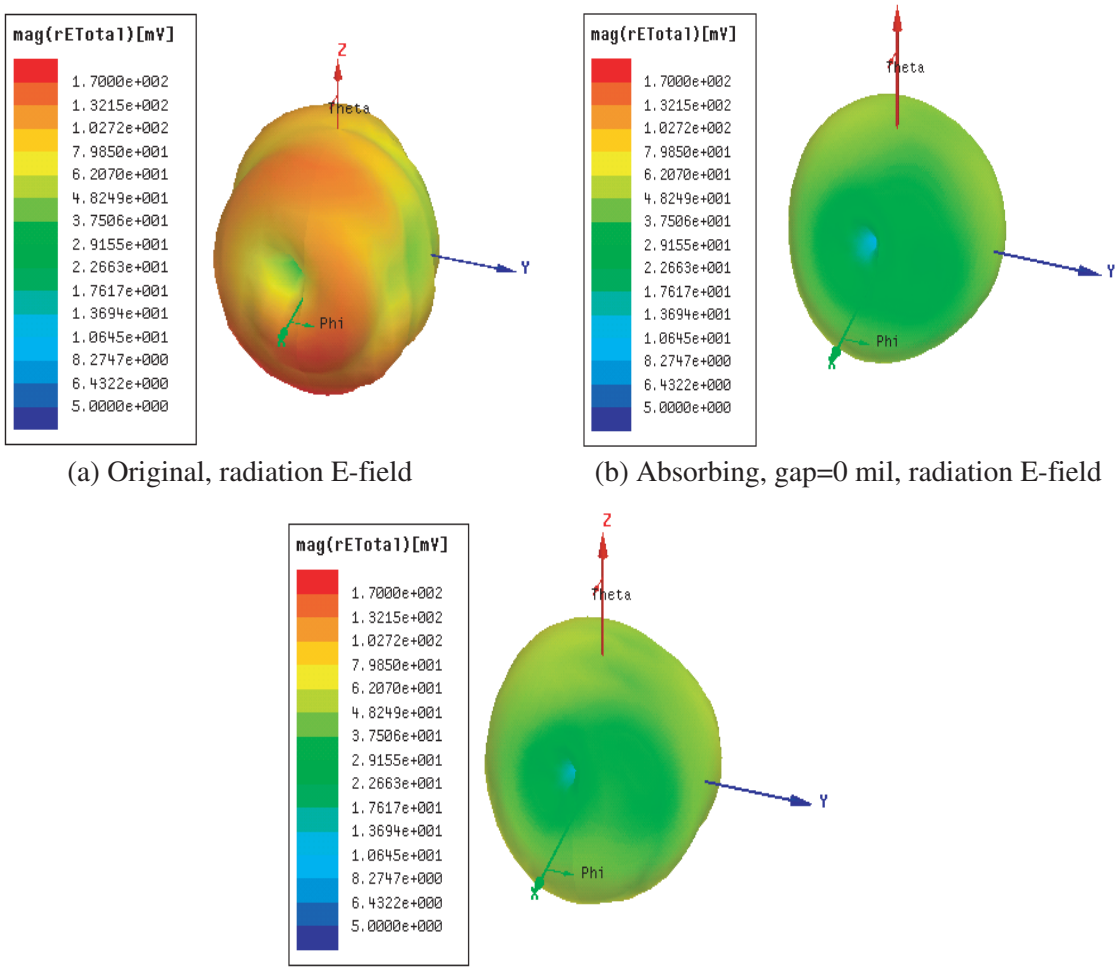


(b) Absorbing, gap=0 mil, E-field along edge



(c) Absorbing, gap=2.5 mil, E-field along edge

Figure 11. (a) The surface electric field along edge of original model, (b) the surface electric field along edge of absorbing model with 0 mil gap, (c) the surface electric field along edge of absorbing model with 2.5 mils gap.



(a) Original, radiation E-field

(b) Absorbing, gap=0 mil, radiation E-field

(c) Absorbing, gap=2.5 mils, radiation E-field

Figure 12. (a) The radiation electric field of original model, (b) the radiation electric field of absorbing model with 0 mil gap, (c) the radiation electric field of absorbing model with 2.5 mils gap.

indicates that the invention has great potential for EMC and EMI applications.

Note that the proposed hybrid technique needs to add absorbing materials along the edge of PCB. The related manufacturing process for the assembly of absorbing materials along the PCB edges needs further development so that the proposed hybrid technique can be enabled for practical high volume manufacturing applications.

3.5. Performance at High Frequencies

In this section, we investigate the performance of absorbing materials at high frequencies up to 10 GHz.

Figure 13(a) is a pair of power and ground planes with no absorbing materials or de-caps. Five small pieces are the ports in HFSS simulations. Fig. 13(b) is the same as Fig. 13(a), except that absorbing materials are attached to the edge of the planes.

In Figs. 14(a), 14(b) and 14(c), we compare the PDN impedances of the model in Fig. 13(a) and the models in 13(b) with two different absorbing materials, WXA and SB1001. Results indicate that both WXA and SB1001 greatly suppress the PDN impedances at broadband frequency range from 0.01 MHz to 10 GHz. The absorbing materials greatly smooth out all the resonant peaks at 1.5 GHz, 3 GHz, 4.5 GHz, as well as those between 5 GHz and 10 GHz. At high frequencies from 1 GHz to 10 GHz, the absorbing materials give more than 10 times of suppression for the transfer impedances.

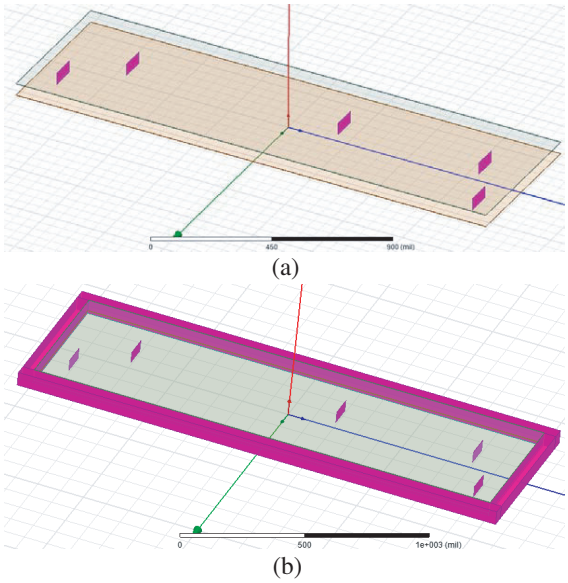


Figure 13. 3D models of two power and ground planes. (a) No absorbing materials, (b) with absorbing material attached along the plane edge.

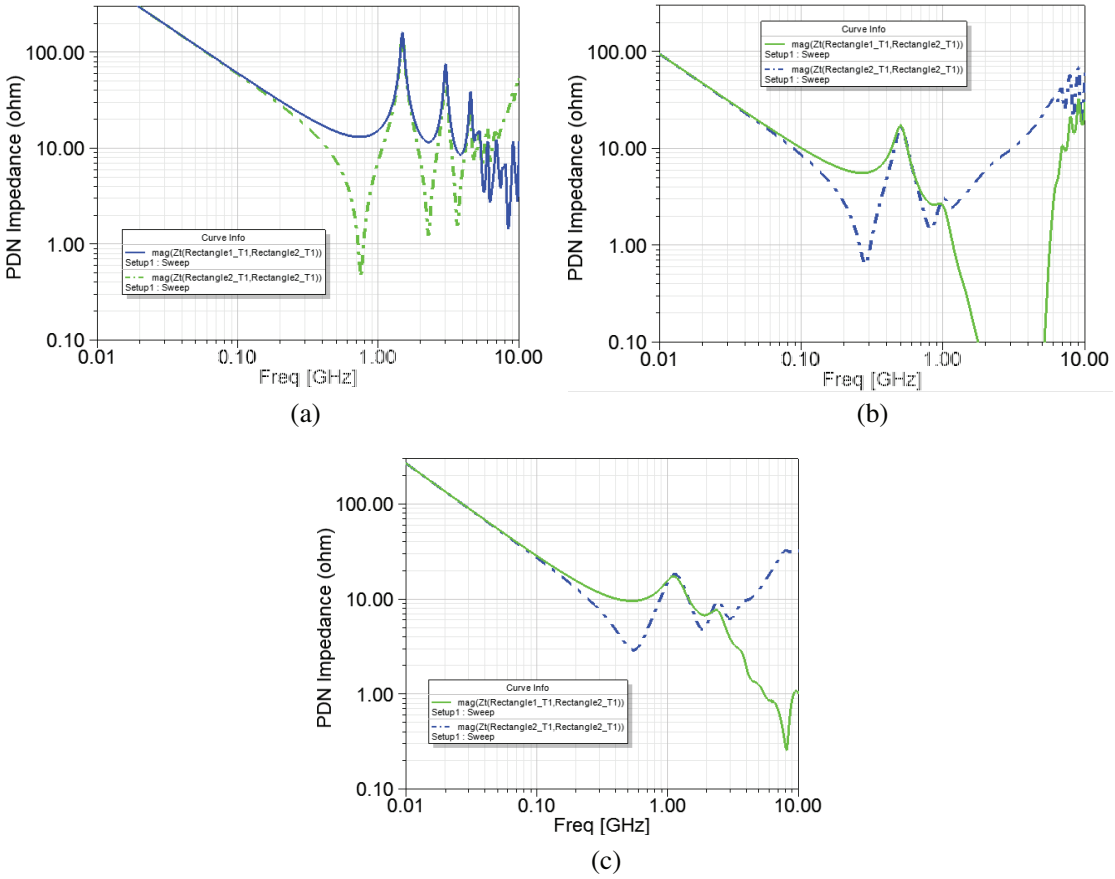


Figure 14. Comparison of PDN impedances for higher frequency range up to 10 GHz. (a) no absorbing material, (b) with WXA absorbing material along the edge, (c) with SB1001 absorbing material along the edge.

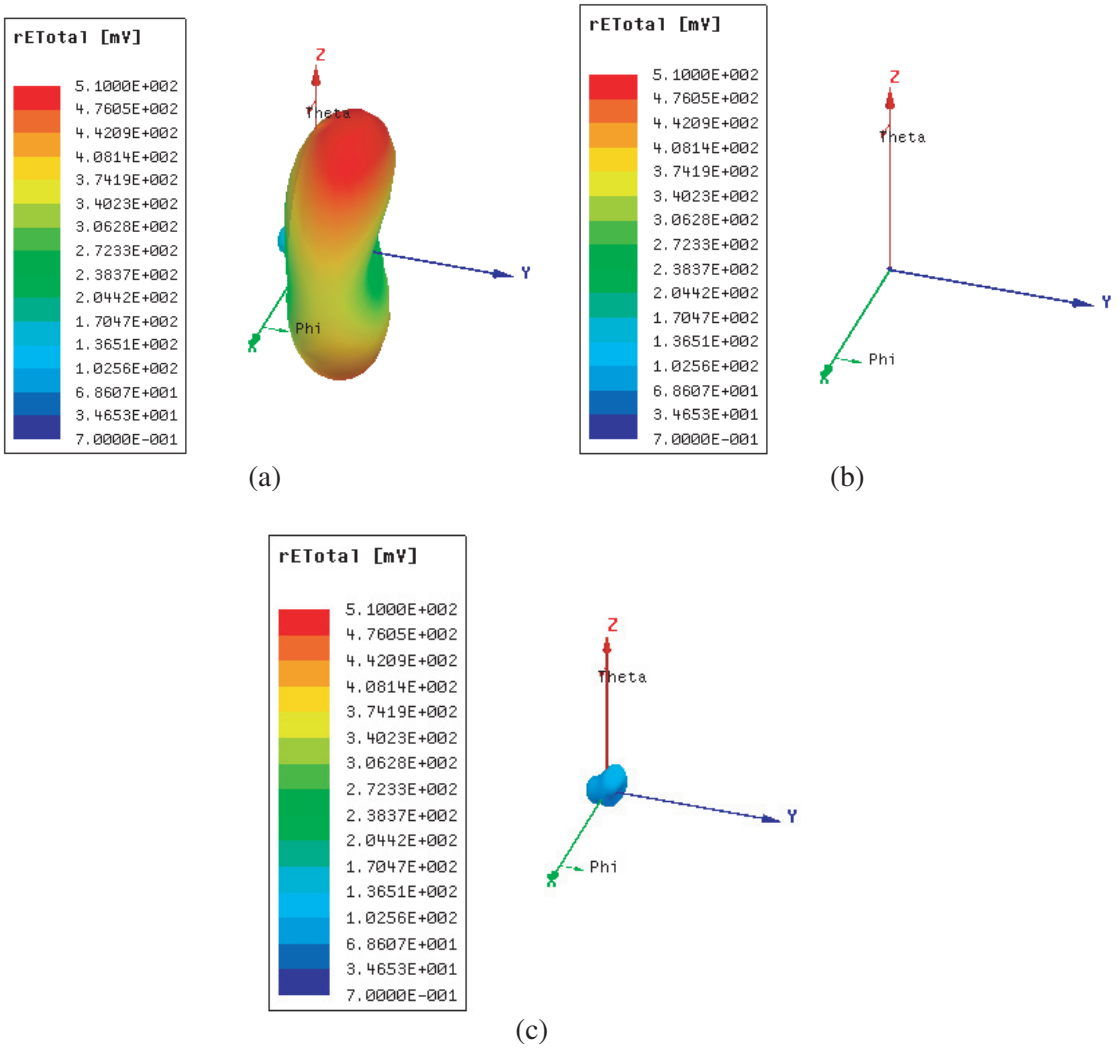


Figure 15. Comparison of radiated E-fields at 5 GHz. (a) No absorbing material, (b) with WXA absorbing material along the edge and (c) with SB1001 absorbing material along the edge.

In Figs. 15(a) to 15(c), we compare the radiated E-fields at 5 GHz among the model in Fig. 13(a) and the models in 13(b) with two different absorbing materials, WXA and SB1001. Results indicate that both WXA and SB1001 greatly suppress the radiated E-fields at 5 GHz. The radiated field is almost invisible after WXA absorbing material is attached. WXA is better than SB1001 because it has larger imaginary part of permittivity at higher frequency, which gives strong attenuation of surface fields at PCB edge as well as the radiated fields.

In Figs. 16(a) to 16(c), we compare the radiated E-fields at 10 GHz. Similar to the results in Figs. 15(a) to 15(c), both WXA and SB1001 work well for EMI suppression. WXA is better than SB1001. The radiated field is also almost invisible after WXA absorbing material is attached. The simulation results show that the absorbing materials placed along the PCB edges are very effective in suppressing EMI noise at high frequencies.

Overall, the absorbing materials are effective in reducing PDN impedances and radiated E-fields over high frequency ranges up to 10 GHz.

To reduce noises at GHz range, the use of on-package de-caps alone is an ineffective way, and plus it will require a significant amount of real-estate. Hybrid technique relies primarily on absorbing materials rather than on-package de-caps for PDN cavity resonant effects mitigation. As shown in simulation results of Fig. 14, absorbing materials alone can work very well at sub-10 GHz, so we apply

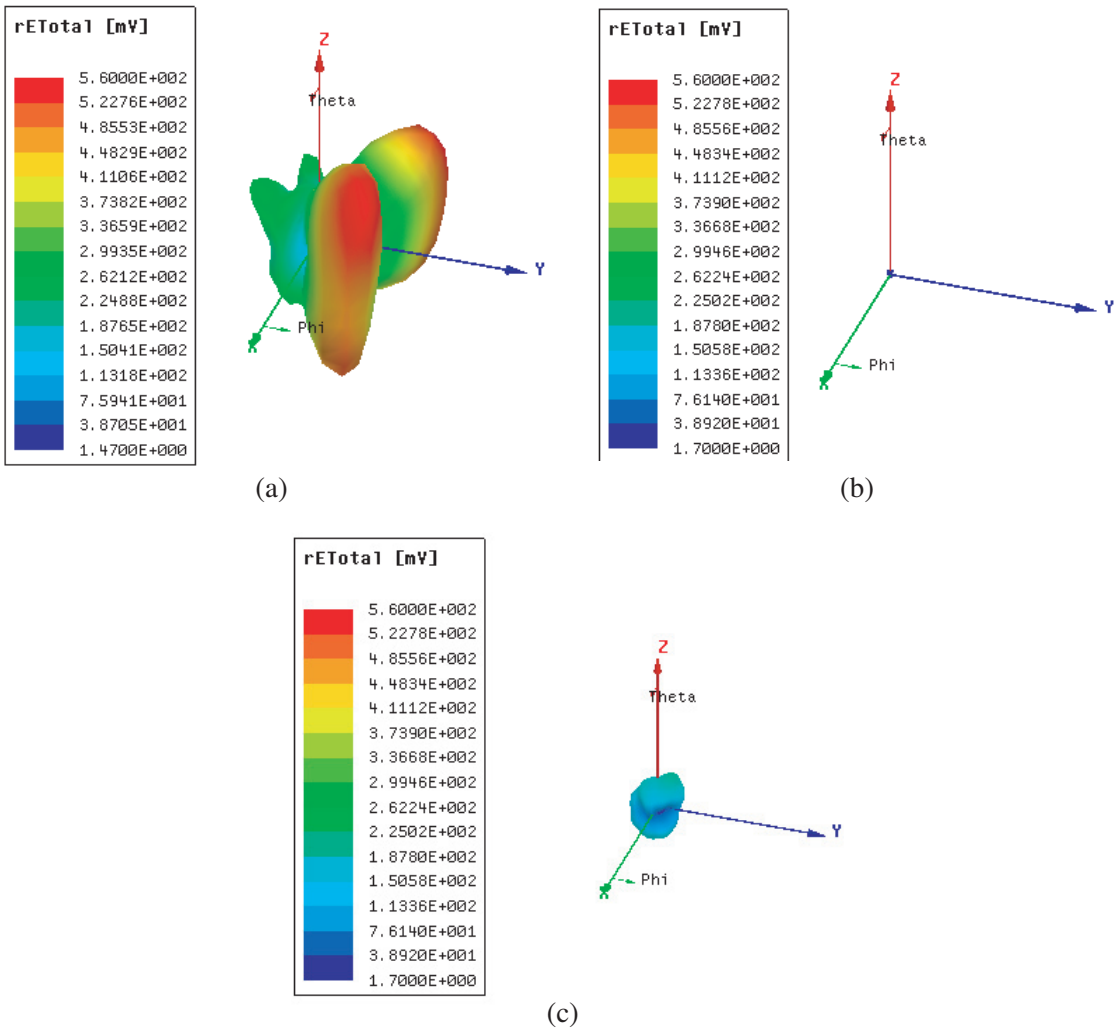


Figure 16. Comparison of radiated E-fields at 10 GHz. (a) No absorbing material, (b) with WXA absorbing material along the edge, (c) with SB1001 absorbing material along the edge.

their properties and on-package de-caps to lower PDN impedance. Using the proposed hybrid technique during the power design and simulation phase will provide insight as to how many on-package or on-board de-caps to use. It may potentially assist with reducing BOM (bill of materials) count if hybrid technique is used effectively.

Remarkably, in this paper, the verification focuses on 3D full wave simulations using HFSS and the measurement dielectric data of absorbing materials, which should be good enough for the proof of concept. In the future study, further experimental verification will be carried out, which will be helpful for further industry practical applications of the proposed technique.

4. CONCLUSION

In this study, we report a technique for PCB SI/PI/EMC/EMI improvements using various absorbing materials applied along the edges to address cavity resonant edge effects and the combination of absorbing material and de-caps. Since the cavity resonant edge effects and the PDN impedance are tightly related, we use the impedance characteristics to determine whether cavity resonant edge effects have been mitigated along the edges of the cavity plane. Modeling and simulations are performed to test the performance. The results of this study show that absorbing material is effective in dampening

the impedance characteristics and suppressing the radiated emissions caused by the PDN resonances. It is also demonstrated that the proposed hybrid technique combining absorbing materials placed along the edge and de-caps added to PDN can further reduce the effects of cavity resonant edge. In addition, the results show that the proposed technique still works for the cases with a gap between absorber and the edge.

REFERENCES

1. Swaminathan, M. and E. Engin, *Power Integrity Modeling and Design for Semiconductors and Systems*, Pearson Education, 2007.
2. Archambeault, B., C. Brench, and S. Connor, "Review of printed-circuit-board level EMI/EMC issues and tools," *IEEE Transactions on Electromagnetic Capability*, Vol. 52, No. 2, 455–461, May 2010.
3. Wang, X.-X. and D.-L. Su, "The influence of power-ground resonance to via's SSN noise coupling in multilayer package and three mitigating ways," *Proc. IEEE Conf. Electron Mater. Packag. (EMAP)*, 1–5, Dec. 11–14, 2006.
4. Pak, J. S., H. Kim, J. Lee, and J. Kim, "Modeling and measurement of radiated field emission from power-ground plane cavity edge excited by through-hole signal via based on balanced TLM and via coupling model," *IEEE Trans. Adv. Packag.*, Vol. 30, No. 1, 73–85, Feb. 2007.
5. Ding, T.-H., Y.-S. Li, D.-C. Jiang, Y.-Z. Qu, and X. Yan, "Estimation method for simultaneous switching noise in power delivery network for high-speed digital system design," *Progress In Electromagnetics Research*, Vol. 125, 79–95, 2012.
6. Tsang, L. and S. Huang, "Broadband Green's function with low wavenumber extraction for arbitrary shaped waveguide and applications to modeling of vias in finite power/ground plane," *Progress In Electromagnetics Research*, Vol. 152, 105–125, 2015.
7. Huang, S. and L. Tsang, "Fast electromagnetic analysis of emissions from printed circuit boards using broadband Green's function method," *IEEE Transactions on Electromagnetic Capability*, Vol. 58, No. 5, 1642–1652, 2016.
8. Huang, S. and L. Tsang, "Fast electromagnetic modeling of traces connecting vias in printed circuit boards using broadband Green's function method," IEEE *Transactions on Components, Packaging and Manufacturing Technology*, 2017, in press.
9. Huang, S. and J. DeLaCruz, "Improvements of system-in-package integration and electrical performance using BVA wire bonding," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2017, in press.
10. Huang, S. and B. Lee, "Novel broadband equalizer optimization technique for high-speed digital system designs," *Progress In Electromagnetics Research B*, Vol. 65, No. 1, 143–155, 2016.
11. Huang, S. and B. Lee, "New de-embedding method with look-up table for characterization of high-speed interconnects," *Progress In Electromagnetics Research B*, Vol. 65, No. 1, 129–141, 2016.
12. Ravelo, B. and O. Maurice, "Kron-Branin modeling of Y-Y-tree interconnects for the PCB signal integrity analysis," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 59, No. 2, 411–419, Apr. 2017.
13. Ravelo, B., "Behavioral model of symmetrical multi-level T-tree interconnects," *Progress In Electromagnetics Research B*, Vol. 41, 23–50, 2012.
14. Perini, J. and L. S. Cohen, "Design of broad-band radar-absorbing materials for large angles of incidence," *IEEE Transactions on Electromagnetic Capability*, Vol. 35, No. 2, 223–230, May 1993.
15. Vinoy, K. J. and R. M. Jha, *Radar Absorbing Materials — From Theory to Design and Characterization*, Kluwer Academic Publishers, Boston, MA, 1996.
16. Hatakeyama, K. and H. Togawa, "Incombustible electromagnetic wave absorber made of nonwoven ceramic fibers," *IEEE Transactions on Electromagnetic Capability*, Vol. 40, No. 1, 27–32, Feb. 1998.
17. Petrov, V. M. and V. V. Gagulin, "Microwave absorbing materials," *Inorganic Materials*, Vol. 37, No. 2, 93–98, 2001.

18. Neo, C. P. and V. K. Varadan, "Optimization of carbon fiber composite for microwave absorber," *IEEE Transactions on Electromagnetic Capability*, Vol. 46, No. 1, 102–106, Feb. 2004.
19. Dixon, P., "Cavity-resonance dampening," *IEEE Microw. Mag.*, Vol. 6, No.2, 74–84, 2005.
20. Zhang, C., H. Li, and M. Lu, "Development of stealth technique compounded radar absorbing material and FSS," *Materials Review*, Vol. 21, No. 1, 118–120, 2007.
21. Ford, K. L. and B. Chambers, "Application of impedance loading to geometric transition radar absorbent material," *IEEE Transactions on Electromagnetic Capability*, Vol. 49, No. 2, 339–345, May 2007.
22. Xu, Z., W. Lin, and L. Kong, "Controllable absorbing structure of metamaterial at microwave," *Progress In Electromagnetics Research*, Vol. 69, 117–125, 2007.
23. Oraizi, H., A. Abdolali, and N. Vaseghi, "Application of double zero metamaterials as radar absorbing materials for the reduction of radar cross section," *Progress In Electromagnetics Research*, Vol. 101, 323–337, 2010.
24. Kim, J.-B. and J.-H. Byun, "Salisbury Sn absorbers of dielectric lossy sheets of carbon nanocomposite laminates," *IEEE Transactions on Electromagnetic Capability*, Vol. 54, No. 1, 37–42, Feb. 2012.
25. Cheng, E. M., M. F. B. A. Malek, M. Ahmed, K. Y. You, K. Y. Lee, and H. Nornikman, "The use of dielectric mixture equations to analyze the dielectric properties of a mixture of rubber tire dust and rice husks in a microwave absorber," *Progress In Electromagnetics Research*, Vol. 129, 559–578, 2012.
26. Koledintseva, M. Y., A. G. Razmadze, A. Y. Gafarov, V. V. Khilkevich, J. L. Drewniak, and T. Tsutaoka, "Attenuation in extended structures coated with thin magneto-dielectric absorber layer," *Progress In Electromagnetics Research*, Vol. 118, 441–459, 2011.
27. Kollatou, T. M., A. I. Dimitriadis, S. Assimonis, N. V. Kantartzis, and C. S. Antonopoulos, "A family of ultra-thin, polarization-insensitive, multi-band, highly absorbing metamaterial structures," *Progress In Electromagnetics Research*, Vol. 136, 579–594, 2013.
28. Araneo, R., G. Lovat, and S. Celozzi, "Compact electromagnetic absorbers for frequencies below 1 GHz," *Progress In Electromagnetics Research*, Vol. 143, 67–86, 2013.
29. Zahid, L., M. F. B. A. Malek, H. Nornikman, N. A. MohdAffendi, A. Ali, N. Hussin, B. H. Ahmad, and M. Z. A. Abdul Aziz, "Development of pyramidal microwave absorber using sugar cane bagasse (SCB)," *Progress In Electromagnetics Research*, Vol. 137, 687–702, 2013.
30. Zhang, F., L. Yang, Y. Jin, and S. He, "Turn a highly-reflective metal into an omnidirectional broadband absorber by coating a purely-dielectric thin layer of grating," *Progress In Electromagnetics Research*, Vol. 134, 95–109, 2013.
31. Wang, G.-D., J.-F. Chen, X. Hu, Z.-Q. Chen, and M. Liu, "Polarization-insensitive triple-band microwave metamaterial absorber based on rotated square rings," *Progress In Electromagnetics Research*, Vol. 145, 175–183, 2014.
32. Lin, J., H. Zhang, P. Li, X. Yin, and G. Zeng, "The electromagnetic shielding effectiveness of a low-cost and transparent stainless steel fiber/silicone resin composite," *IEEE Transactions on Electromagnetic Capability*, Vol. 56, No. 2, 328–334, Apr. 2014.
33. Dincer, F., O. Akgol, M. Karaaslan, E. Unal, and C. Sabah, "Polarization angle independent perfect metamaterial absorbers for solar cell applications in the microwave, infrared, and visible regime," *Progress In Electromagnetics Research*, Vol 144, 93–101, 2014.
34. Huang, S. and J. J. Abbott, "Reflected signal absorption in interconnect," US patent No. 14/303396, 2014.
35. Huang, S., K. Xiao, B. Lee, B. Wu, and X. Ye, "Absorbing termination in an interconnect," US patent No. 14/539597, 2014.
36. Huang, S., K. Xiao, and B. Lee, "Electromagnetic wave absorption technology for stub effects mitigation", *DesignCon*, Santa Clara, CA, 2016.
37. Huang, S., X. Ye, N. Kang, B. Lee, and K. Xiao, "Suppression of couplings in high-speed interconnects using absorbing materials," *IEEE Transactions on Electromagnetic Compatibility*,

Vol. 58, No. 5, 1432–1439, Oct. 2016.

38. Huang, S., K. Xiao, B. Lee, and X. Ye, "Stub effect mitigations using absorbing materials," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 6, No. 8, 1233–1244, 2016.
39. Li, J., X. Li, S. Toor, H. Fan, A. U. Bhobe, J. Fan, and J. L. Drewniak, "EMI coupling paths and mitigation in a board-to-board connector," *IEEE Transactions on Electromagnetic Capability*, Vol. 57, No. 4, 771–779, Aug. 2015.
40. Huang, S., G. Charles, K. Xiao, B. Lee, G. Ouyang, and H. Zhang, "Suppression of cavity resonant edge effects and PDN impedance using absorbing material," *2015 IEEE Symposium on Electromagnetic Compatibility and Signal Integrity*, 12–16, Santa Clara, CA, 2015.
41. Murata capacitor product online data base, http://www.murata.com/en-us/tool/download/simsurfing, 2016.