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An 8 GHz Front-End Module with High-Performance T/R Switch and LNA

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Abstract—A front-end module (FEM) consisting of a single-pole-double-throw (SPDT) switch and a low noise amplifier (LNA) with good performance is proposed. The SPDT switch is based on PIN diodes, which are mounted on impedance transforming lines parallelled to the main transmission lines with an asymmetric topology. This asymmetric topology is utilized to achieve low insertion loss and high transmit-to-receive isolation. The interstage matching of switch and LNA is designed to achieve low noise figure. To validate the design, the FEM is simulated, fabricated and measured. The experiment results show that, within the range of 7.8–8.1 GHz, the FEM achieves a gain of 22 dB and noise figure of 1.9 dB in receiving mode, with an insertion loss of 0.9 dB and isolation of 40 dB in transmitting mode. In addition, the FEM can handle up to 4 W transmitting power at 8 GHz with good linearity.

1. INTRODUCTION

For many radio systems, such as radars and time-division duplex (TDD) wireless communication systems, transmit/receive (T/R) switch and LNA are key components of the front-end. T/R switch is used to share the same antenna for both the receiver and transmitter, and a low insertion loss switch can help improve the system equivalent isotropic radiated power (EIRP) and gain-to-noise-temperature (G/T) of receiving channel. An LNA with low noise figure and proper gain can improve the receiver sensitivity. On the other hand, modern radio systems always require compact size. In addition, high power handling capability is a key factor in many applications.

In the past decades, a variety of high-performance switches [1–4] and LNAs have been reported. Although they have good performance, these independent designs lead to additional insertion loss caused by interstage connectors and matching networks, resulting in bulk size. To achieve better performances and compact size, integrated designs of switch and LNA were also reported [5, 6]. In [5], an asymmetric SPDT transmit/receive (T/R) switch co-optimized with an LNA tailored to X-band operation and implemented in a 0.13 µm silicon-germanium (SiGe) BiCMOS technology was presented. This design is compact with integration except for high power application. An integrated aluminium gallium nitride (AlGaN)/gallium nitride (GaN) X-band receiver front-end consisting of an SPDT switch and an LNA is shown in [6]. The AlGaN/GaN monolithic microwave integrated circuit (MMIC) technology is an excellent candidate for high power application, but the performance of this design is not comparable with available receivers.

In this work, an 8 GHz FEM consisting of an SPDT PIN switch and an LNA is implemented on a Rogers RO4350b substrate board. PIN diodes are used for this SPDT switch and mounted on impedance transforming lines, which are parallel to the main transmission lines with an asymmetric topology. This asymmetric topology is good for achieving low insertion loss and high transmit-to-receive isolation. Due to using PIN diodes as switching components, the switch has high power handling capability and fast

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switching speed [1]. The input impedance of the LNA is matched directly to the output impedance of the SPDT switch instead of matching both of them to 50 ohm. This integrated design eliminates the loss caused by interstage radio frequency (RF) connectors and port matching networks, and is characterized by compact size compared to front-end composed of independently designed modules. The measurement results show that 22 dB gain with 1.9 dB noise figure (NF) is achieved in receiving mode, while 0.9 dB insertion loss with 40 dB isolation is achieved in transmitting mode within the range of 7.8–8.1 GHz. In addition, the FEM can handle up to 4 W transmitting power at 8 GHz with good linearity.

2. DESIGN PROCEDURE

The diagram of the FEM is shown in Fig. 1. The ANT port is connected to the antenna. The TX port is reserved for transmitting and RX port for receiving. One path of the SPDT switch is connected to the LNA input port, and the other path is connected to the TX port.

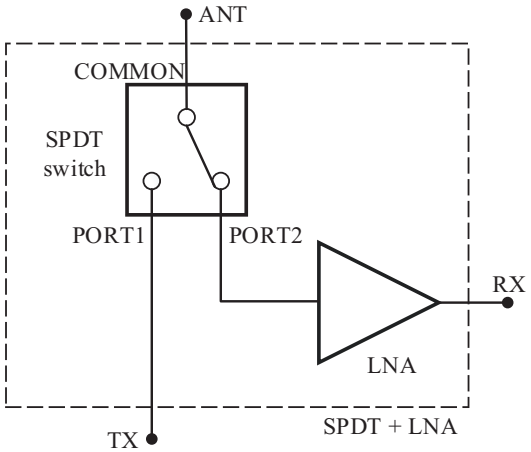

Figure 1. Diagram of the proposed FEM including the SPDT switch and LNA.

For transmitting, the insertion loss of the path from TX to ANT should be low to reduce the transmitting power loss from power amplifier (PA) to antenna, and the isolation from PORT1 to PORT2 of the SPDT switch should be high enough to prevent the LNA from being damaged by the power from TX. For receiving, low insertion loss from COMMON to PORT2 can reduce the NF of the receiving channel. PIN diodes are used as switching components to achieve high power handling capability. An LNA with low noise figure and proper gain can improve the sensitivity of the receiving channel, and flat gain can help to reduce the error vector magnitude (EVM) for the receiver [7]. The interstage matching network connected with the SPDT and LNA can also be optimized to reduce the noise figure.

2.1. SPDT Switch Design

For the conventional series type and shunt type PIN switch, the PIN diodes are mounted on the RF path, and the bonding process will have a significant impact on RF performance of the switch. The conventional shunt type PIN SPDT switch requires direct current (DC) blocking capacitors [8], which can introduce additional insertion loss. Therefore, it is desirable to design a switch that does not have a PIN diode and DC blocking capacitor on the RF path. Learning from the switch topology of [2], we propose the switch topology of this paper.

The schematic of the proposed SPDT switch is depicted in Fig. 2. The path from PORT1 to COMMON is for transmitting and the path from COMMON to PORT2 for receiving. PIN diodes D1, D2 and D3 are introduced on the parallel microstrip line stubs to realize turning on/off of the main RF channel. Switch operation is performed by changing the voltage of VC_TX and VC_RX, which will set the PIN diodes to be on-state or off-state. For transmitting, D1 is set to on-state while D2 and D3 are

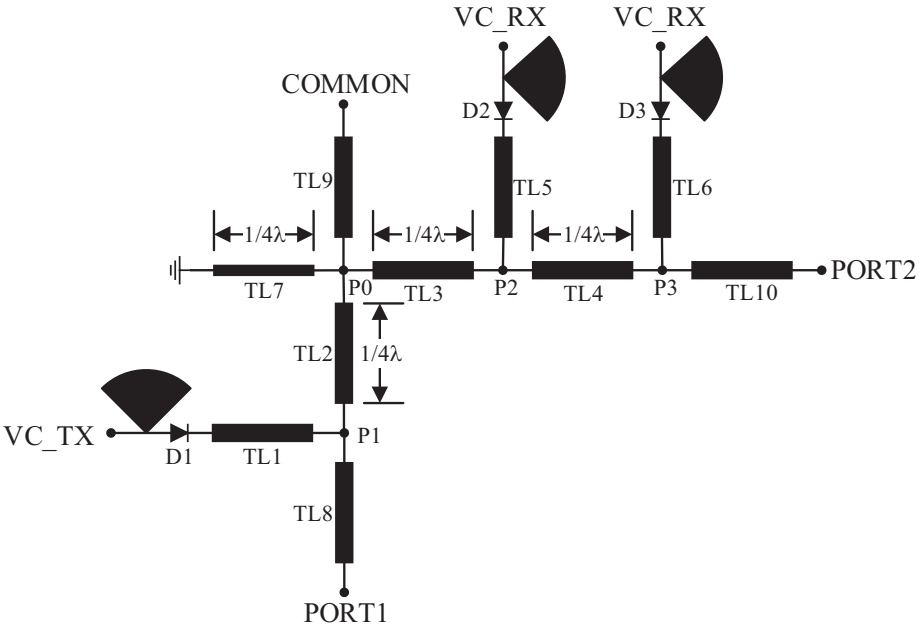

Figure 2. Topology of the SPDT switch.

set to off-state at the same time. The low impedance of D1 is transformed to high impedance at point P1 by the microstrip line TL1, and the high impedances of D2, D3 are transformed by microstrip lines TL5, TL6 to low impedances at junctions P2, P3. With the quarter-wavelength microstrip lines TL3, TL4, the low impedances at P2, P3 will be transformed to high impedance at P0, so the signal can be transmitted on the path from PORT1 to COMMON with low insertion loss and isolated to PORT2. Similarly for receiving, D1 is set to off-state while D2 and D3 are simultaneously set to on-state, so that the signal can be transmitted on the path from COMMON to PORT2 with low loss and isolated to PORT1. PIN D3, impedance transformation line TL6 and quarter-wavelength microstrip line TL4 are used to improve the isolation performance of path PORT1 to PORT2. TL7 is a quarter-wavelength microstrip line used to provide DC ground for the bias voltage of PIN diodes. TL8, TL9, TL10 are the microstrip lines used to connect to the external ports.

The modeling and simulation of the SPDT switch are performed on ANSYS HFSS. The substrate material is Rogers RO4350b, with the thickness of 0.762 mm. When initially setting up the model, the characteristic impedances of the microstrip lines are set to 75 ohm except TL7 (130 ohm). The lengths of TL2, TL3 and TL4 are equal, and the lengths of TL1, TL5 and TL6 are equal. In order to improve the switch performance, low junction capacitance PIN chip diodes MA/COM MA4P161-134 are used. The diodes are soldered on the microstrip lines, and the anodes of the diodes are connected to fan-stub capacitors by gold bonding wires. The preliminary model is shown in Fig. 3. By simulation, it can be found that the length of impedance transforming lines TL1, TL5 and TL6 has a major effect on the center frequency. Reducing the length of TL1, TL5 and TL6 can increase the center frequency, and appropriately adjusting the length of TL2, TL3 and TL4 can improve the return loss (RL) of the input/output ports. The lengths of TL8, TL9 and TL10 have no significant effect on the performance. The influence of length of impedance transforming lines TL1, TL5, TL6 on center frequency is shown in Fig. 4, and the influence of length of quarter-wavelength lines TL2, TL3, TL4 on return loss of input/output ports is shown in Fig. 5. Finally, the length of TL1, TL5 and TL6 is chosen as 150 mil, and the length of TL2, TL3 and TL4 is chosen as 255 mil. The center frequency corrected switch model is shown in Fig. 6, and the design parameters are shown in Table 1.

By simulation, as the results shown in Fig. 7, it can be found that the switch with microstrip line of 75 ohm characteristic impedance design (TL1, TL2, ... TL10 except TL7) has better insertion loss performance than that of 50 ohm design and has similar insertion loss performance to 100 ohm design. In consideration of high power handling for the switch, the SPDT switch is designed with microstrip

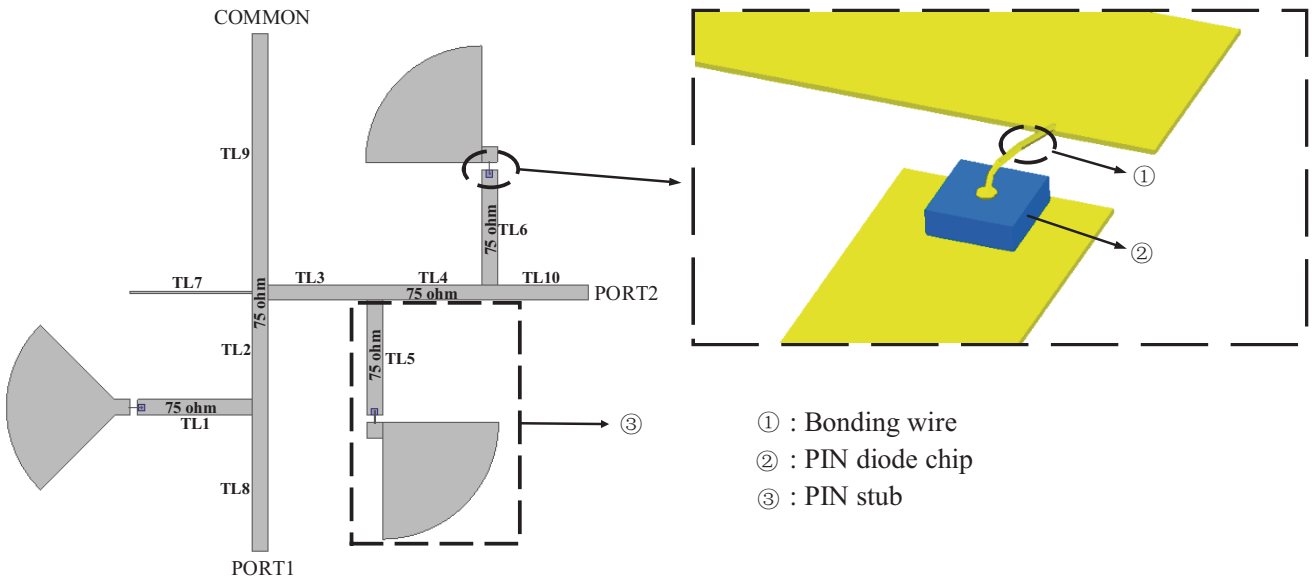

Figure 3. Preliminary model of the SPDT switch with 75 ohm microstrip lines.

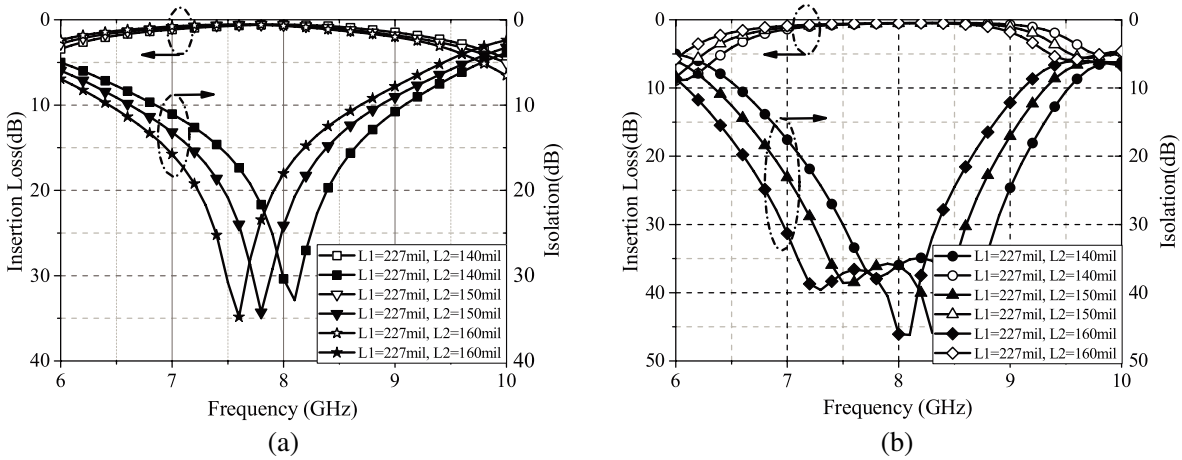

Figure 4. Influence of length of impedance transformation lines TL1, TL5 and TL6 on center frequency of the switch. (L1 represents the length of TL2, TL3 and TL4. L2 represents the length of TL1, TL5 and TL6.) (a) Insertion loss of PORT1-to-COMMON and isolation of PORT1-to-PORT2 in transmitting mode. (b) Insertion loss of COMMON-to-PORT2 and isolation of COMMON-to-PORT1 in receiving mode.

Table 1. Design parameters of the center frequency corrected switch model.

Microstrip line	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10
Length (mil)	150	255	255	255	150	150	237	241	496	124

lines of 75 ohm characteristic impedance.

The switch model shown in Fig. 6 was modified with single PIN stub on receiving channel to investigate the impact of the second PIN stub on switch performance, as shown in Fig. 8. The simulation results are shown in Fig. 9. From the figure, it can be found that the switch with double PIN stubs on

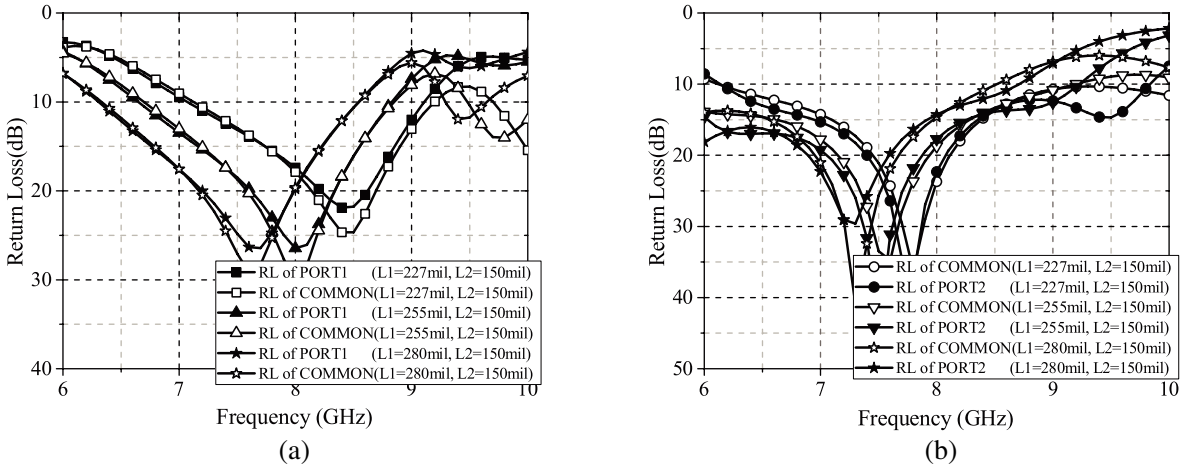

Figure 5. Influence of length of quarterwave-length lines TL2, TL3 and TL4 on return loss of input/output ports. (L1 represents the length of TL2, TL3 and TL4. L2 represents the length of TL1, TL5 and TL6.) (a) Return loss of PORT1 and COMMON in transmitting mode. (b) Return loss of PORT2 and COMMON in receiving mode.

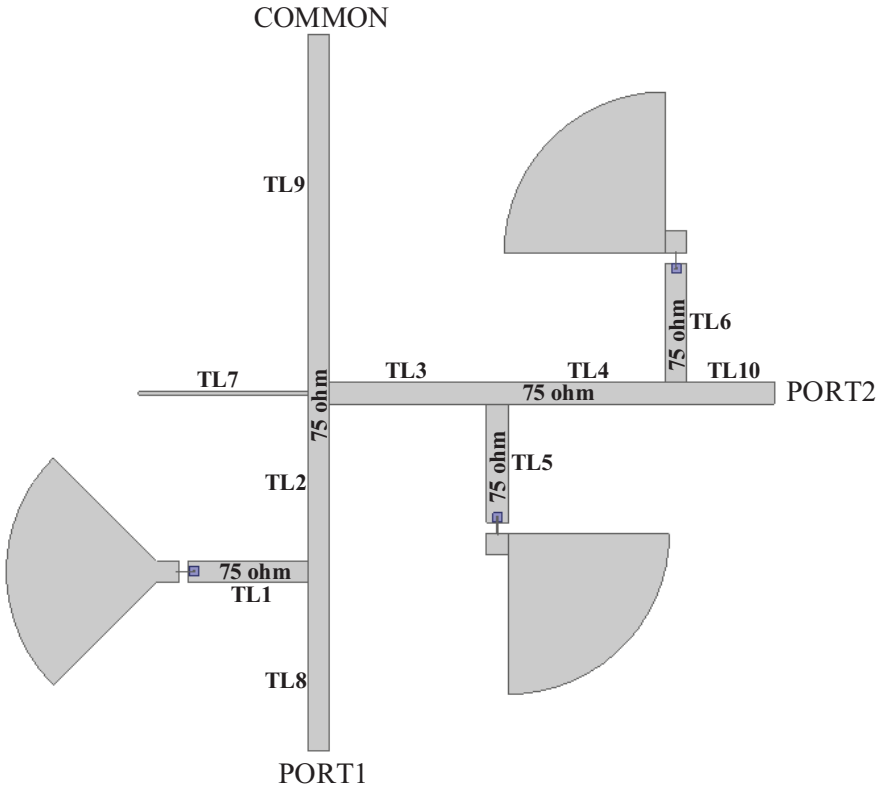

Figure 6. The center frequency corrected switch model.

receiving channel has much better transmit-to-receive (PORT1 to PORT2) isolation performance, and the insertion loss of the receiving channel (COMMON to PORT2) has almost the same performance as the switch with single PIN stub among 7–9 GHz. From E-field distribution of the switch with single PIN stub on receiving channel as shown in Fig. 10(a), it can be found that when the switch is in transmitting mode, the signal travels from PORT1 to COMMON in a travelling wave, and most of the

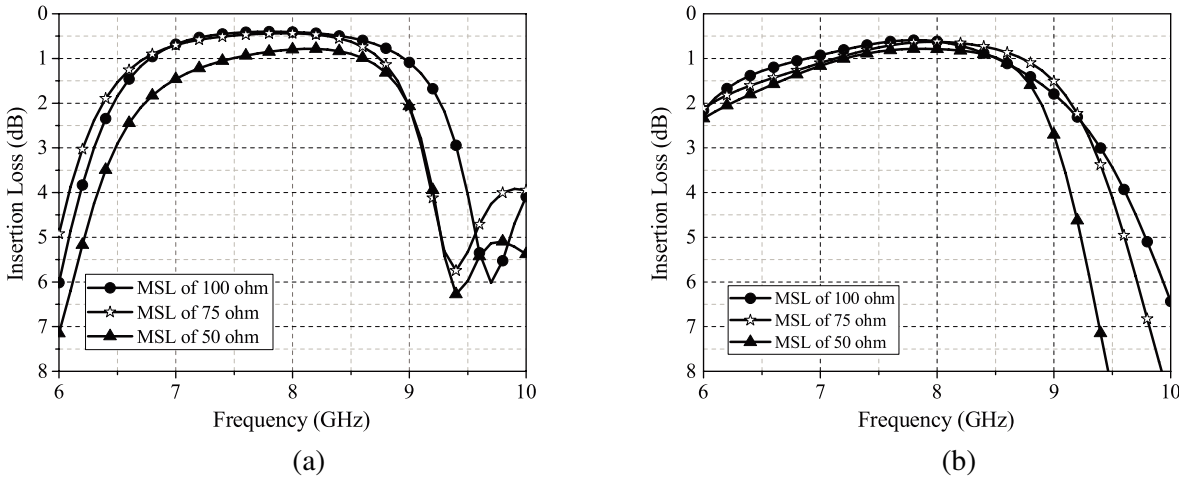

Figure 7. Simulated insertion loss of the SPDT switch with different microstrip line (MSL) characteristic impedance for (a) PORT1 to COMMON in transmitting mode. (b) COMMON to PORT2 in receiving mode.

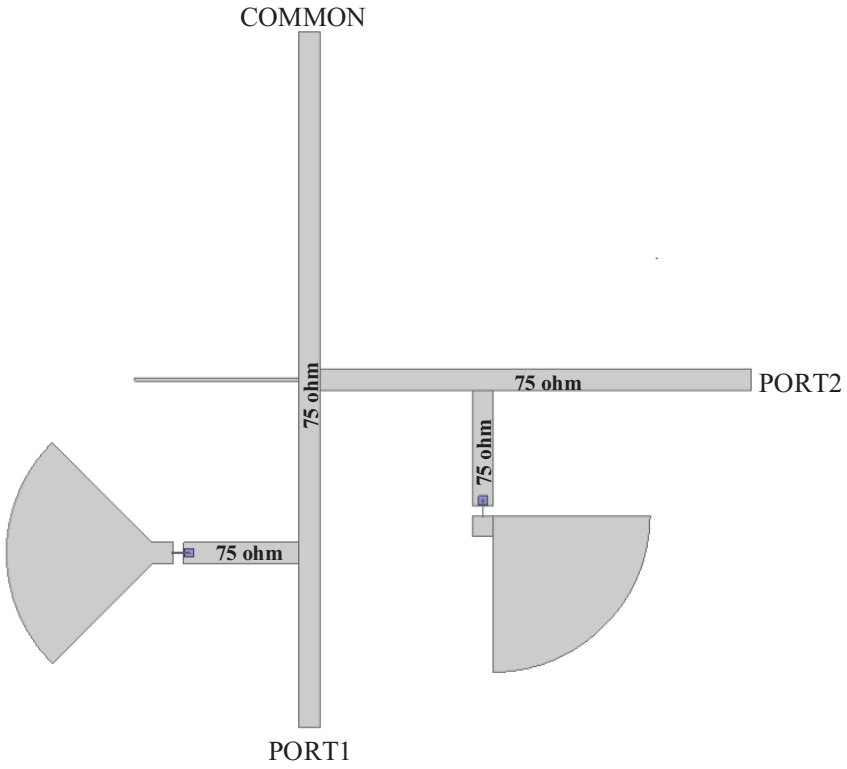

Figure 8. Layout of SPDT switch with single PIN stub on receiving channel.

signal that travels from PORT1 to COMMON is reflected by the PIN stub due to the low impedance at P2 junction, with a little signal leaking to PORT2. On the other hand, for the switch with double PIN stubs on receiving channel as shown in Fig. 10(b), the signal leaked from P2 is reflected again due to the low impedance at P3. Therefore, the switch with double PIN stubs on the receiving channel has better transmit-to-receive isolation. In order to get better transmit-to-receive isolation, the design with double PIN stubs on the receiving channel shown in Fig. 3 is used.

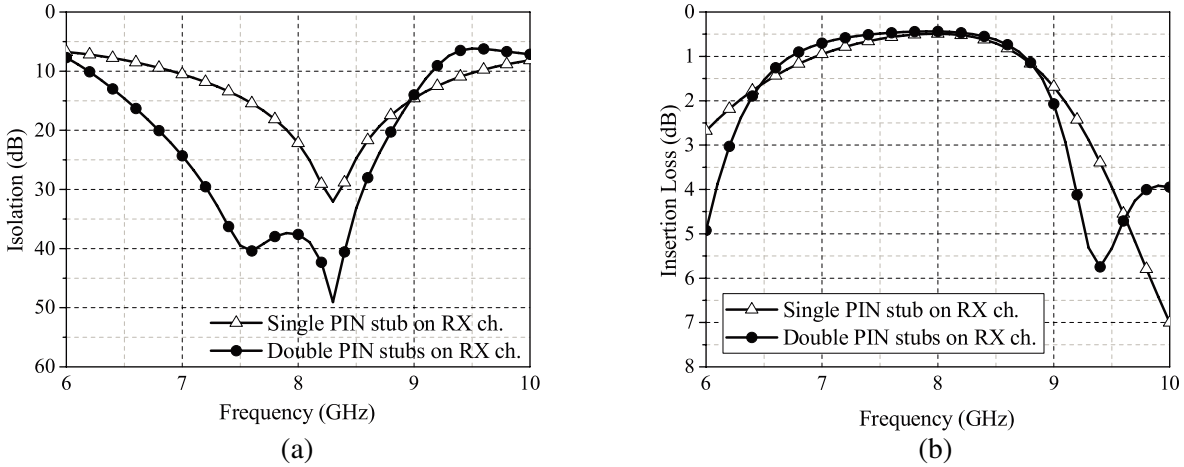

Figure 9. Performance comparison of switch receiving channel with single or double PIN stub. (a) Isolation of PORT1 to PORT2. (b) Insertion loss of COMMON to PORT2.

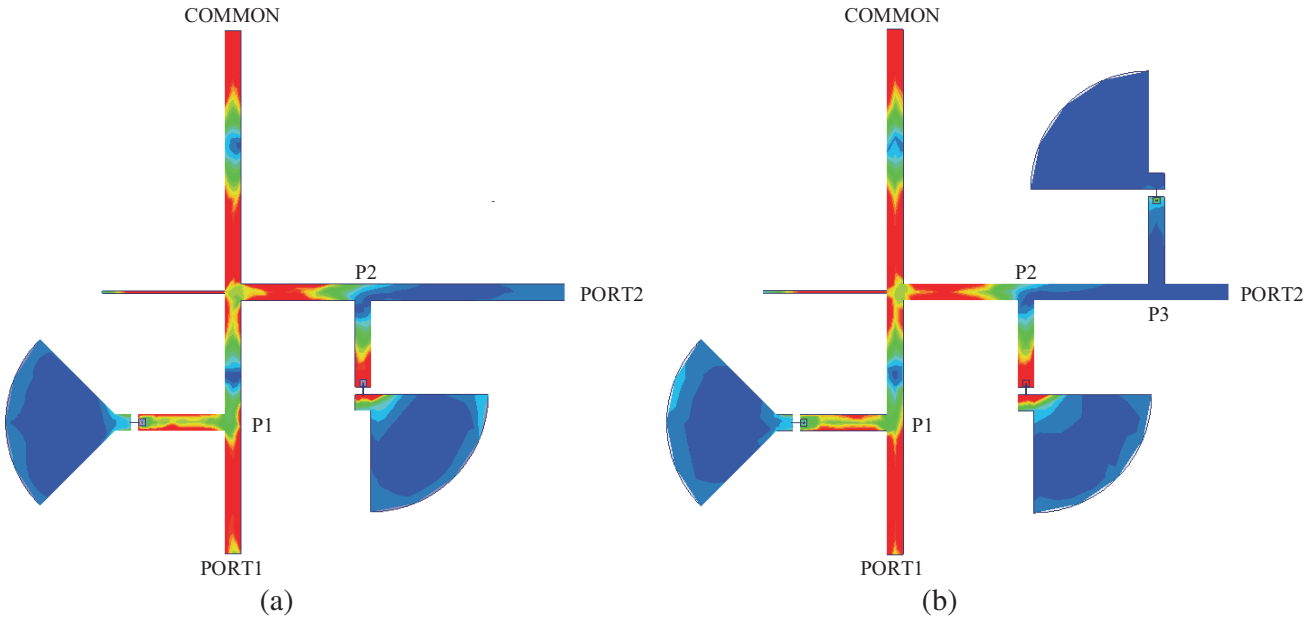

Figure 10. E-field distribution comparison of switch with single or double PIN stub. (a) Switch with single PIN stub. (b) Switch with double PIN stubs.

Based on the prototype shown in Fig. 3, additional microstrip lines are used to match with the 50 ohm characteristic impedances for the external ports PORT1 and COMMON. Considering the compact design of the RF module, the layout of the switch is modified finally as in Fig. 11.

2.2. LNA Design

A two-stage LNA is designed to obtain low noise performance and adequate gain, as shown in Fig. 12. According to the noise figure formula for cascade system, the noise figure of the LNA at the first stage should be as low as possible. Therefore, the first stage LNA is matched by minimum noise method. To compensate the transistor gain degrading with frequency [9], a negative feedback network is introduced between the drain and gate of the second stage LNA. Furthermore, the interstage matching and output matching are designed by conjugated impedance matching.

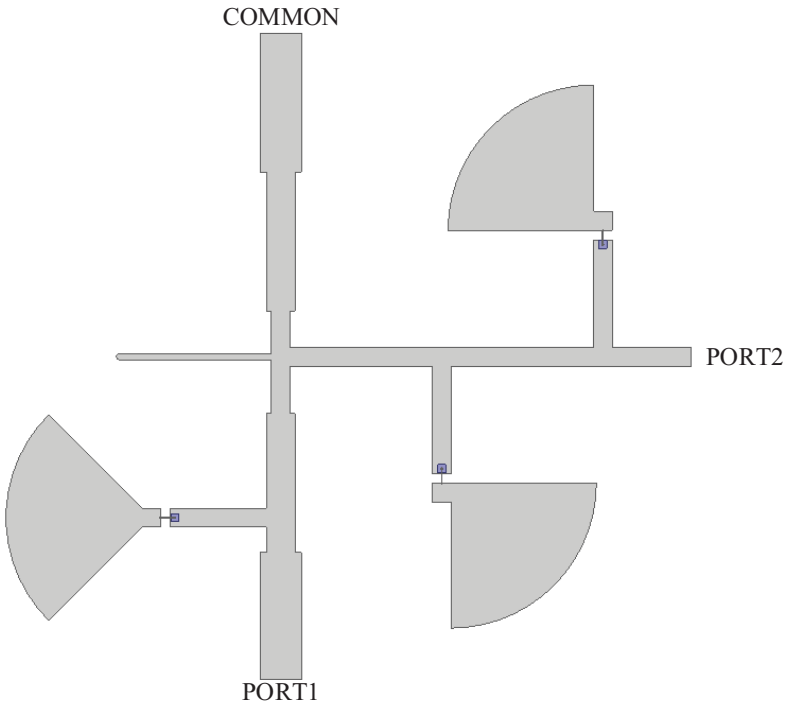

Figure 11. Layout of the SPDT switch with 50 ohm impedance of COMMON and PORT1.

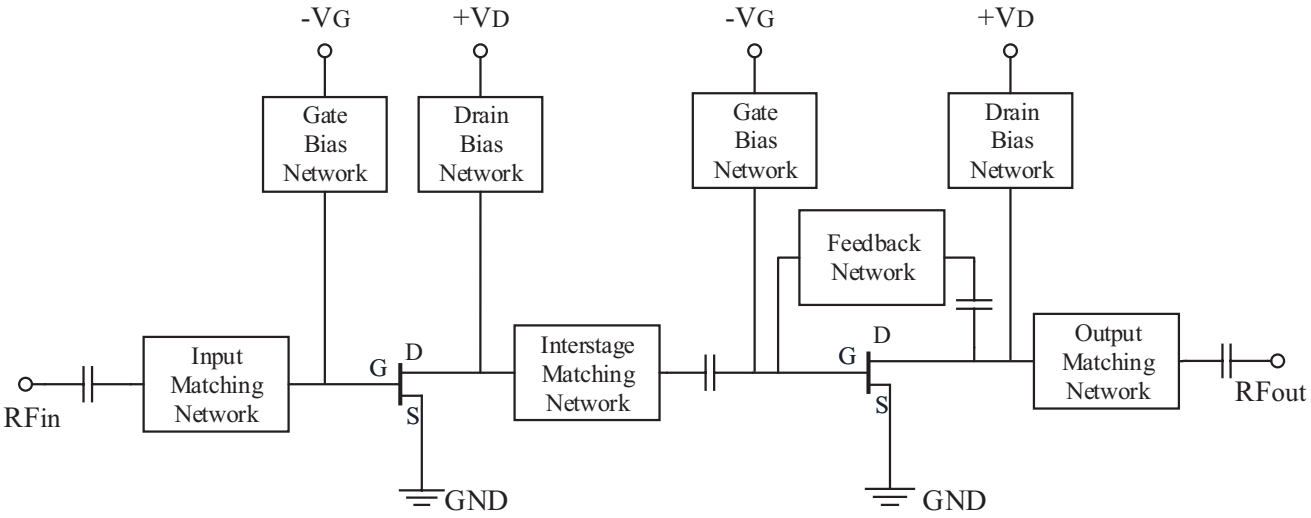

Figure 12. LNA diagram.

The Mitsubishi MGF4941AL low noise high electron mobility transistor (HEMT) is used as the amplifier. The transistor has low noise and proper gain. The LNA is designed and simulated by Agilent ADS software. The substrate material is Rogers RO4350b, with a thickness of 0.762 mm. The quiescent operation point of the transistor is set as $Vd = 2$ V and $Ids = 10$ mA. The input matching network of the first stage LNA is matched directly to the output impedance of the SPDT PORT2 in receiving mode by a single-stub matching network instead of matching both of them to 50 ohm. Compared to independent designs, this design can reduce the extra loss caused by port matching networks and achieve a compact size. The interstage and output matching networks are realized by single microstrip line of different

characteristic impedances and lengths. Quarter-wavelength microstrip lines and fan-shape stubs are used as the DC feeding networks.

A parallel resistor feedback network is used on the second stage LNA to get flat gain. During the electromagnetic-circuit (EM-circuit) co-simulation, it can be found that co-simulation results of EM-circuit vary significantly compared to simulation results of circuit, and co-simulation results of EM-circuit are very sensitive to the layout of feedback network. The main reason is that the feedback microstrip line couples with the nearby GND via. In order to get more accurate design during the circuit simulation, the feedback microstrip line is modeled with nearby GND via to the EM model by ADS Momentum, and then imported to the circuit schematic to do the LNA circuit simulation. The established model and LNA layout are shown in Fig. 13.

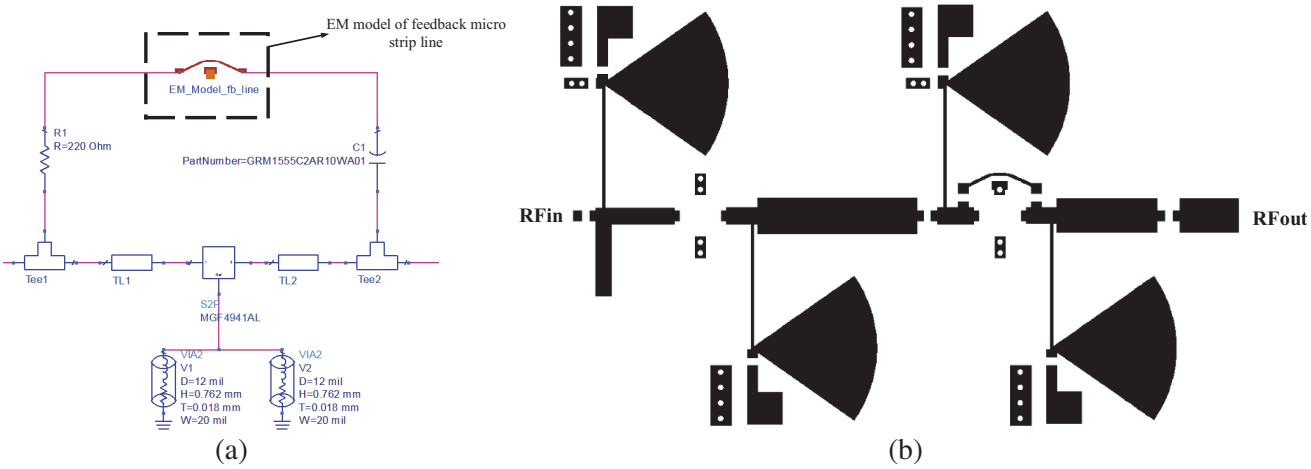

Figure 13. (a) Circuit simulation using EM model of the feedback microstrip line on the 2nd stage LNA. (b) LNA layout.

3. RESULT AND DISCUSSION

The SPDT switch and LNA are designed at 7.9 GHz and implemented on a Rogers RO4350b substrate board. The board photograph is shown in Fig. 14. All the test results include effects of the SubMiniature version A (SMA) connectors (the insertion loss is about 0.2 dB for one SMA connector), and these effects were not considered in simulation.

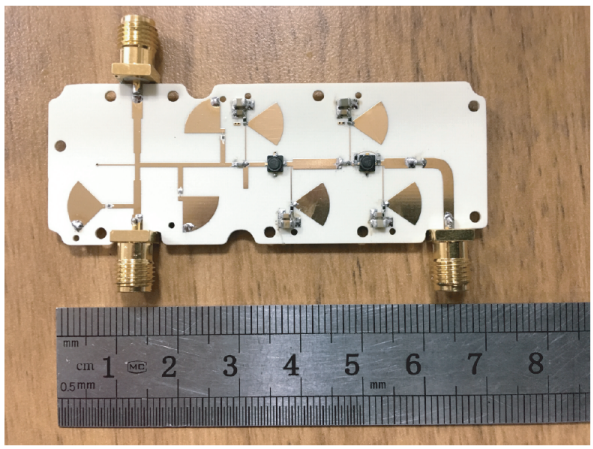

Figure 14. Photograph for the proposed FEM.

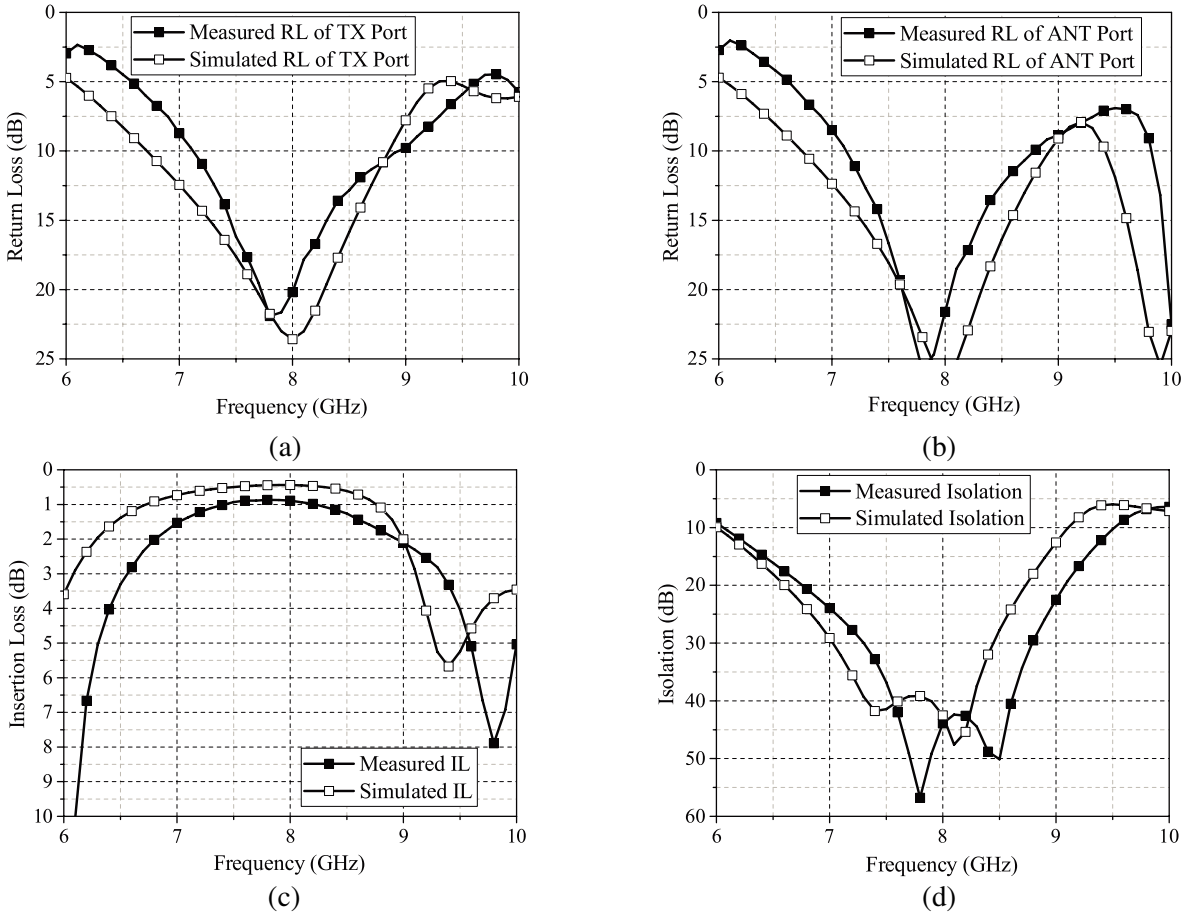

Figure 15. Simulated and measured S-parameters in transmitting mode. (a) Return loss on TX port. (b) Return loss on ANT port. (c) Insertion loss of TX port to ANT port. (d) Isolation of TX port to LNA.

The S-parameters measurements are performed with an Agilent E8361C PNA network analyzer. To measure the isolation (ISO) and insertion loss (IL) in transmitting mode, PIN D1 is set to on-state with 50 mA, and D2, D3 set to off-state simultaneously with -12 V. Since the isolation from TX port to the LNA input port cannot be measured directly on board as shown in Fig. 14, a stand-alone switch board is used for isolation measurement. The simulated and measured S-parameters of the SPDT switch in transmitting mode are shown in Fig. 15. The measured insertion loss of transmitting channel is 0.9 dB, and the isolation of transmit-to-receive (PORT1 to PORT2) is more than 40 dB within the range of 7.8–8.1 GHz. Due to experimental conditions and equipments limitations, power handling capability test was only tested up to 4 W transmitting power at 8 GHz. The measured insertion loss of TX port to ANT port for different transmitting power is shown in Fig. 16. The test result shows that the FEM works well with good linearity for transmitting power from 0.5 W to 4 W.

To measure the S-parameters in receiving mode, the PIN D1 is set to off-state with -12 V, and D2, D3 are set to on-state simultaneously with 50 mA. The LNA is biased with 2.7 V on the drain and -0.27 V on the gate. The simulated and measured S-parameters in receiving mode are shown in Fig. 17. The NF is measured by Keysight N9020A signal analyzer and N4002A noise source probe, with careful calibration of cable and probe losses. 10 samples were measured and then averaged to minimize NF measurement error. The simulated and measured NFs in receiving mode are shown in Fig. 18. The measured NF is 1.9 dB, and the measured gain is 22 dB within the range of 7.8–8.1 GHz.

Table 2 lists the performance comparison among recently published SPDT switch and LNA of C-band and X-band. In the table, the proposed FEM shows good performance. The disadvantage of this design is the relatively narrow working bandwidth owing to the topology of the SPDT switch.

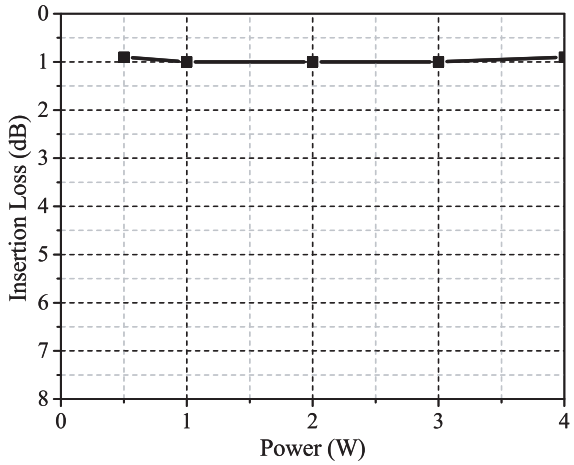

Figure 16. Measured insertion loss of TX port to ANT port for different transmitting power.

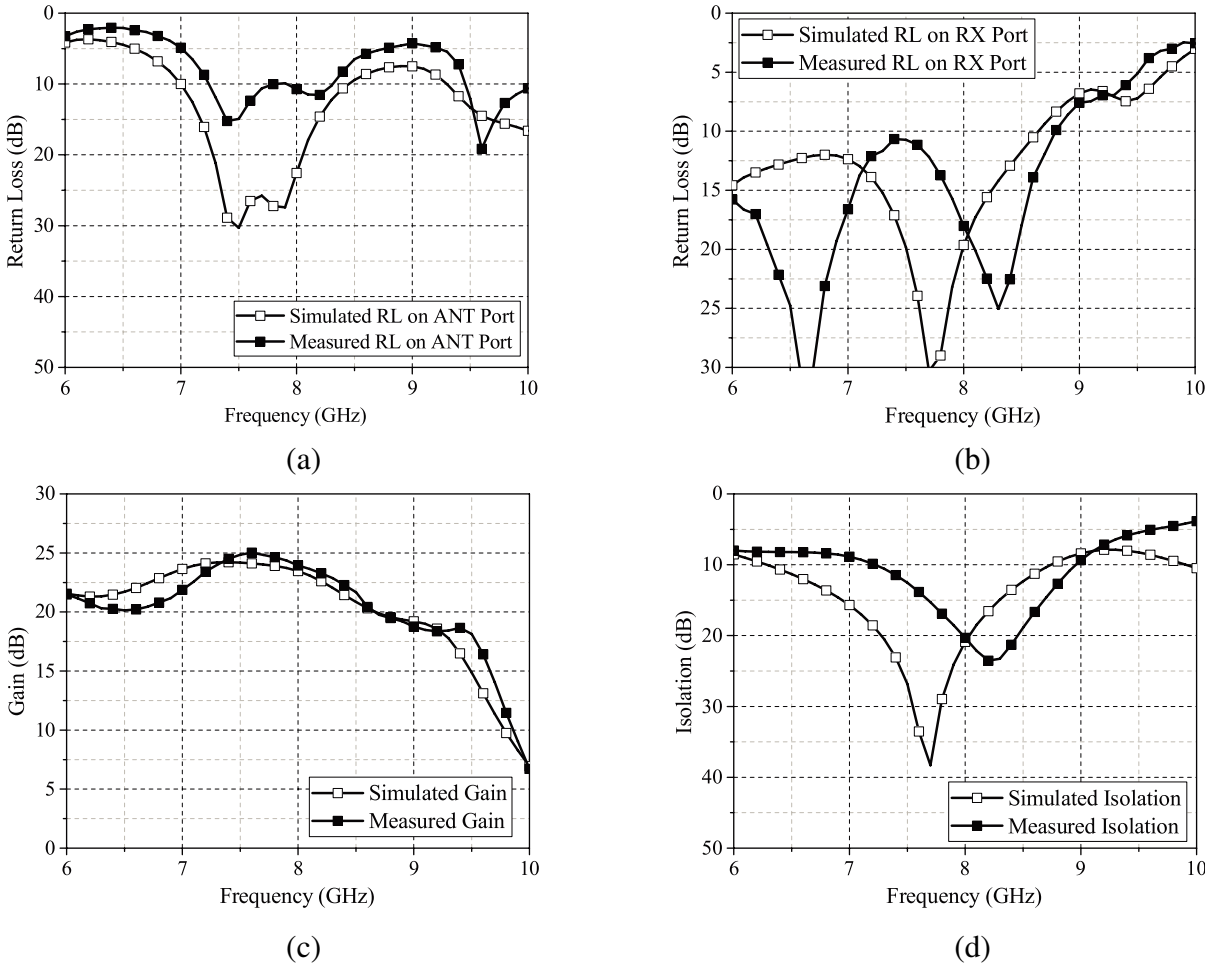

Figure 17. Simulated and measured S-parameters in receiving mode. (a) Return loss on ANT port. (b) Return loss on RX port. (c) Gain of ANT port to RX port. (d) Isolation of ANT port to TX port.

Table 2. Performance comparison among recently published SPDT switch and LNA of C-band and X-band.

Reference	Circuit Type	Technology	Freq. (GHz)	Gain (dB)	NF (dB)	IL/ISO/RL (dB)	Output P1 dB (dBm)
[2]	SPDT	PCB	4.6–4.8	—	—	0.5/20/15	—
[5]	SPDT+LNA	AlGaN/GaN MMIC	9–13	9.6	4.1	2.0/33/8	> 33
[6]	SPDT+LNA	SiGe BiCMOS	9–11	14	2.2	1.1/26/10	26.9
This work	SPDT+LNA	PCB	7.8–8.1	22	1.9	0.9/40/10	> 36

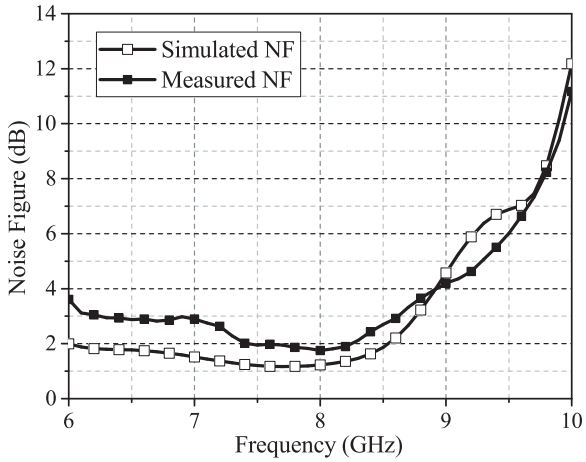

Figure 18. Simulated and measured noise figure in receiving mode.

4. CONCLUSION

An FEM consisting of an SPDT switch and an LNA is presented. This FEM is characterized by high performance, compact size, and has been successfully used in one radio transceiver for private network communication operating in X-band.

ACKNOWLEDGMENT

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