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# Design and Development of Millimeter Wave Interferometer Circuit for Real-Time Measurement of Plasma Density

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**Abstract**—A 3-mm wave interferometer is designed and developed to measure the electron density online at the central chord of Aditya tokamak, unambiguously. The scheme used for this has the advantages in operating the interferometer without a source frequency modulation and easy data processing. The central chord of a 3-mm wave homodyne interferometer system is modified to make a quadrature circuit by using phase shifters and magic tees. This is used to produce the sine/cosine fringe signals. These outputs are amplified and converted into pulses and passed to wired logic up/down fringe counter. Digital synchronous logic circuit is implemented in a Complex Programmable Logic Device (CPLD), followed by digital to analog converter (DAC) and scaler which produces a voltage proportional to increase or decrease in plasma density in real time. The paper presents about this technique and test results of the fringe counter with artificial signals. The chord averaged plasma density $n_e = 0.9 \times 10^{13}\,\mathrm{cm}^{-3}$ is measured online at Aditya tokamak using this interferometer.

## 1. INTRODUCTION

Tokamak is one of the major controlled nuclear fusion research devices. It is extremely important to measure the plasma density in tokamaks to set its operating regime. Online measurement of the plasma density is needed to control the gas feed system for long duration plasmas.

A 100 GHz homodyne interferometer is used to measure the averaged plasma density in Aditya tokamak by using fringe counting technique [1, 2]. The fringe data are processed after the plasma shot by using a software developed in MATLAB. However, decoding of information from the detector signal to phase information during a pulsed experiment is not unique, since the signal at the detector has a component proportional to the cosine of $\emptyset$ (i.e., phase). Many methods, by using source frequency modulation, are used to remove this ambiguity [3, 4]. The unambiguous technique described in the present paper, to measure the electron density, has the advantages in operating without a source frequency modulation and easy data processing for the Aditya tokamak. The central chord of 100 GHz interferometer is modified by using magic tees and phase shifters to measure the electron density unambiguously. A wired logic fringe counter is designed, developed and tested with artificial signal as well as with a real signal from plasma of Aditya tokamak.

This circuit will be utilized for providing real-time feedback control for the gas injection system for long-term stable operation. Therefore, the interferometer data should be processed such that the measured electron density is most reliable, error free and real time.

The next section describes the modified experimental setup and the 3-mm wave interferometer for Aditya tokamak. Section 3 presents a signal processing in interferometric measurements by using unique analog and digitally designed wired logic fringe counter. Section 4 describes results of testing of wired

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logic fringe counter with function generator and test results with moving Perspex wedge between the horns of interferometer in place of plasma. The system is finally tested with plasma at Aditya tokamak and chord averaged plasma density $n_e = 0.9 \times 10^{13}\,\mathrm{cm}^{-3}$ is measured, unambiguously.

## 2. 3-MM WAVE INTERFEROMETER SYSTEM

The schematic diagram of a 3-mm wave interferometer for Aditya tokamak is shown in Fig. 1. A 100 GHz Gun Oscillator with isolator (power output = 13 dBm) is used as a microwave source. Gunn Oscillator is used here due to its phase noise value of −75 dBc/Hz at 100-kHz offset from the center frequency. These oscillators are especially designed for low AM/FM noise characteristics. Phase locking method is not considered here since, in homodyne system, the measurement is done at 100 GHz, and phase noise introduce is very low. The output power of isolator is divided in three parts ($P_s, P_{r1}, P_{r2}$) by 10 dB and 3 dB directional couplers (D.C.). Two of them ($P_{r1}, P_{r2}$) were guided into magic tees via attenuator (ATT) and Phase Shifters (P.S.) as reference signals. Another part ($P_s$) was guided into Aditya tokamak and incident upon the plasma vertically through a transmitting horn. The wave transmitted through plasma was received by receiving horn, divided into two parts ($P_{s1}, P_{s2}$) and then guided into the magic tees. The distance between the receiving and transmitting horns is 1.05 m. These are placed at major radius of Aditya tokamak ($R = 75$ cm) in order to measure the central chord plasma density. Ceramic lenses are placed in front of the horns for good collimation of the wave.

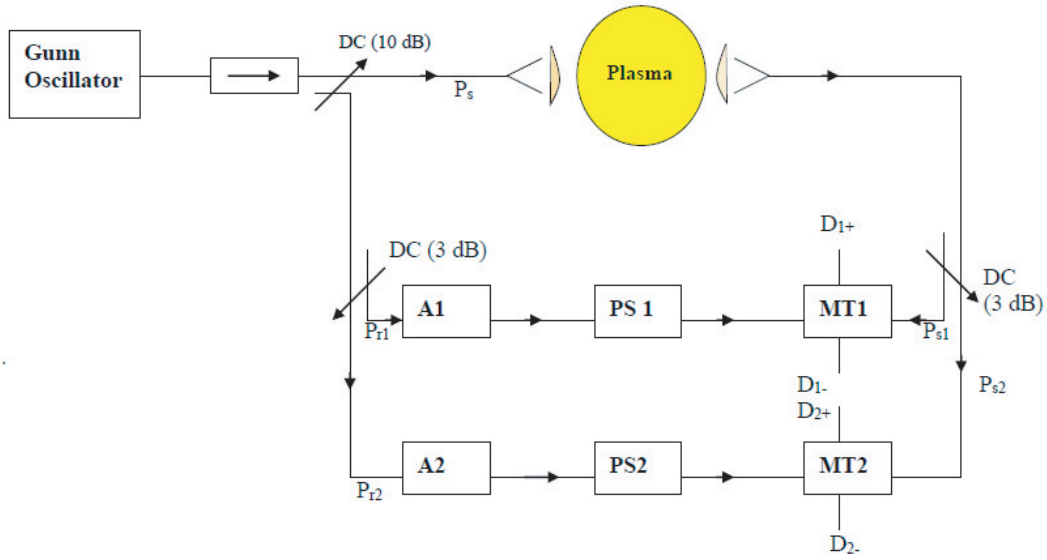


**Figure 1.** Schematic diagram of the 3 mm wave interferometer for the Aditya tokamak.

The mixed output signals $D_{1,2}$ from the diode detectors (Fig. 1) are

$$D^{+}_{1,2} = A_{+}\left|P_{r1,2} + P_{s1,2}\right|^2 \tag{1}$$

$$D^{-}_{1,2} = A_{-}\left|P_{r1,2} - P_{s1,2}\right|^2 \tag{2}$$

where, $A_{\pm}$ are the gain constants corresponding to the rectifying efficiency of the diodes.

To maximize the contrasts of these output signals, the attenuators were adjusted so as to equalize the amplitudes of $P_{s1,2}$. The idling terms $|P_{r1,2}|^2$, $|P_{s1,2}|^2$ of the signals $D_1$ and $D_2$ in Equations (1) and (2) were cancelled out with the AC coupled instrumentation amplifiers.

The Output Signals of the amplifiers (Fig. 2) can be written as

$$V_{1,2} = A_{1,2}\cos\theta_{1,2} \tag{3}$$

where $A_{1,2}$ are the constants depending on the total gain and $\emptyset_{1,2}$ the microwave amplitudes and are the total phase differences between $P_{r1,2}$ and $P_{s1,2}$.

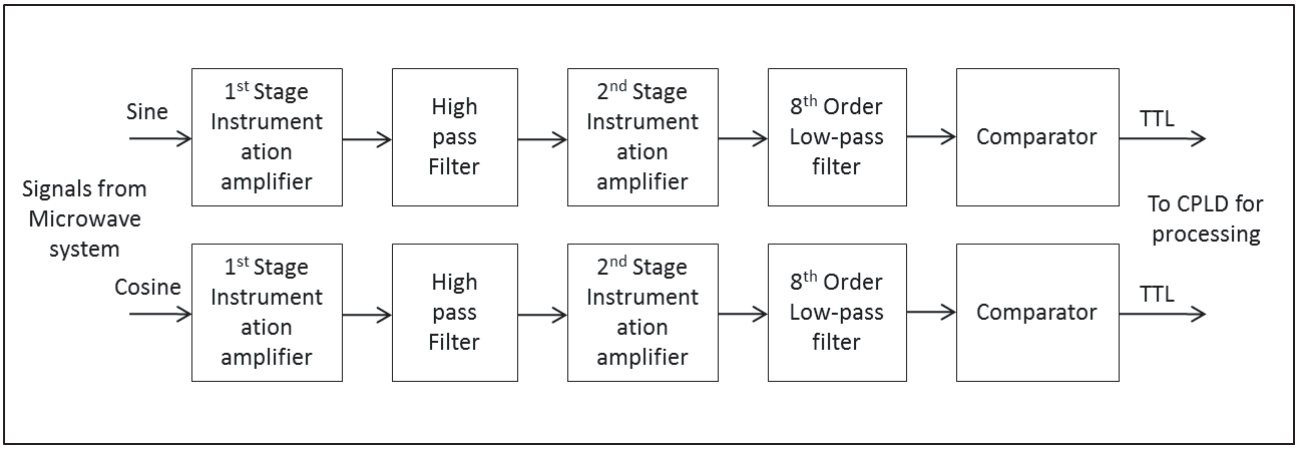


**Figure 2.** Analog section.

### 2.1. Principle of Phase Detection

The refractive index $\mu_P(s)$ of a plasma with an electron density $n_e\,(\mathrm{cm}^{-3})$ at a position $s$ is approximately expressed as

$$\mu_P(s) = \left[1 - (f_p^2/f^2)\right]^{\frac{1}{2}} \tag{4}$$

$$f_p = 8980 n_e^{1/2} \tag{5}$$

where $f$ is the frequency of the probing wave and $f_p$ the plasma frequency. In the case of $f_p^2 \ll f^2$, Equation (4) can be approximated as

$$\mu_P(s) \sim \left[1 - \frac{1}{2}\left(\frac{f_p^2}{f^2}\right)\right] \tag{6}$$

and then $1 - \mu_P(s)$ is proportional to $n_e$.

The total phase differences $\theta_{1,2}$ are expressed as

$$\theta_{1,2} = \emptyset_{1,2} + \varphi_{1,2} + (2\pi/\lambda) L_p\,(1 - \overline{\mu_P}) \tag{7}$$

$$\overline{\mu_P} = \frac{1}{L_p}\int \mu_P dS, \tag{8}$$

where $\lambda = \frac{c}{f}$ is the wavelength in the vacuum; $\varphi_{1,2}$ are the constant phase differences coming from the path differences between a measuring and reference paths of the interferometer; $\emptyset_{1,2}$ are the phasors shifted by the phase shifter; $\overline{\mu_P}$ is the average refractive index along a wave path in the plasma with a line element $dS$ of the wave path and the plasma length $L_p = \int dS$.

Choosing $\emptyset_{1,2}$ so as to be

$$\theta_1 - \theta_2 = (\varphi_1 + \emptyset_1) - (\varphi_2 + \emptyset_2) = \pi/2 \tag{9}$$

Equation (3) becomes

$$V_1 = A_1 \sin \Delta\theta(t) \tag{10}$$

$$V_2 = A_2 \cos \Delta\theta(t) \tag{11}$$

Here, the phase constant term in Equation (7) was practically neglected by adjusting appropriately the phase shifters, and $\Delta\theta(t) = (2\pi/\lambda)L_p(1 - \overline{\mu_P})$ is the phase shift due to plasma.

In the following circuit, a real-time processing method of the fringe signals $(V_1, V_2)$ with a hardware logic up/down counting-circuit converts them to $\Delta\theta(t)$ in units of $\pi$ radians. In this method, one of the signals $V_1$ or $V_2$ was used as a gate signal, and an up/down counting was performed when the other signal was crossing the zero level upward/downward. The time-evolution of the total up/down counting result $\Delta\theta(t)$ which was quantized by $\pi$ rad was displayed on an oscilloscope.

## 3. FRINGE COUNTER ELECTRONICS CIRCUIT

The electronics circuit of fringe counter is mainly divided to three sections such as analog section, digital logic section and output section. Each section is described in detail below.

### 3.1. Analog Section

A block diagram of the analog section is shown in Fig. 2. The blocks are described in the following sections.

#### *3.1.1. Two Stage Instrumentation Amplifier*

The amplitudes of the fringe signals are in the range of 200 to 400 μV over a DC offset voltage about 40 mV to 60 mV in sine channel and cosine channel, respectively. Two stages instrumentation amplifier is used to amplify these signals. The first stage has a fixed gain of 100. Further, a passive high pass filter with a cutoff frequency of $2H_Z$ is used to block the DC component. The signal is again amplified in second stage with an amplifier of variable gain. The gain of second stage amplifiers can be adjusted by means of selector switch. Presently it is fixed at 43. So the total gain is 4300.

A Low Noise, precision instrumentation amplifier AD524 which has a very high common mode rejection ratio [5] is used. Even though the input signal is a single ended, instrumentation amplifier will help to eliminate ground loop interference at the input side. The high input impedance of the AD524 keeps the detector always in the safe side.

#### *3.1.2. Eighth Order Low Pass Filter*

The bandwidth of the amplifier section is 250 kHz. Sometimes, Magneto Hydro Dynamics (MHD) activities are also observed in the fringe signal. To remove these activities, a low-pass filter is used after amplifiers. Monolithic switched capacitor filter provides very steep attenuation in the stop band. MAX296 Clock tunable filter is used. It is an eighth order Bessel low-pass filter with stopband attenuation of −50 dB at second octave and −80 dB at third octave. This makes the output signal noise band in the range of less than 10 mv after 4300 gain.

#### *3.1.3. Comparator*

The output of the low-pass filter is converted to rectangular TTL pulses. Because the fringe counting core logic is done digitally, an op-amp comparator is used as a zero cross detector for this purpose. However, to avoid jitters in the comparator due to ground noise, a fixed threshold voltage is set. For sine signal, the threshold is kept at +300 mV, and for cosine signal, the threshold has to be kept at −700 mV. The reason for negative threshold for cosine signal is that the cosine signal will fully shift to negative level after high-pass filter (differentiation).

### 3.2. Digital Logic Section

This is the core section of the circuit, which contains many subsections. Details are described in the following paragraphs.

A block diagram is shown in Fig. 3. All the digital logic circuits are implemented in a single CPLD (Complex Programmable Logic Device), XC95108. The coding is done using the Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) in Xilinx ISE design tools. This IDE (Integrated Development Environment) supports complete flow for system level design for VHDL Coding, synthesis, simulating and implementing the design to a single CPLD. The whole algorithm is developed with synchronous logic with sampling frequency of 2 MHz (0.5 μs). The flowchart of VHDL code is shown in Fig. 4. It consists of many parallel processes. All the processes will run with the reference trigger of the start of a plasma discharge. The different logic blocks implemented inside the CPLD are explained here.

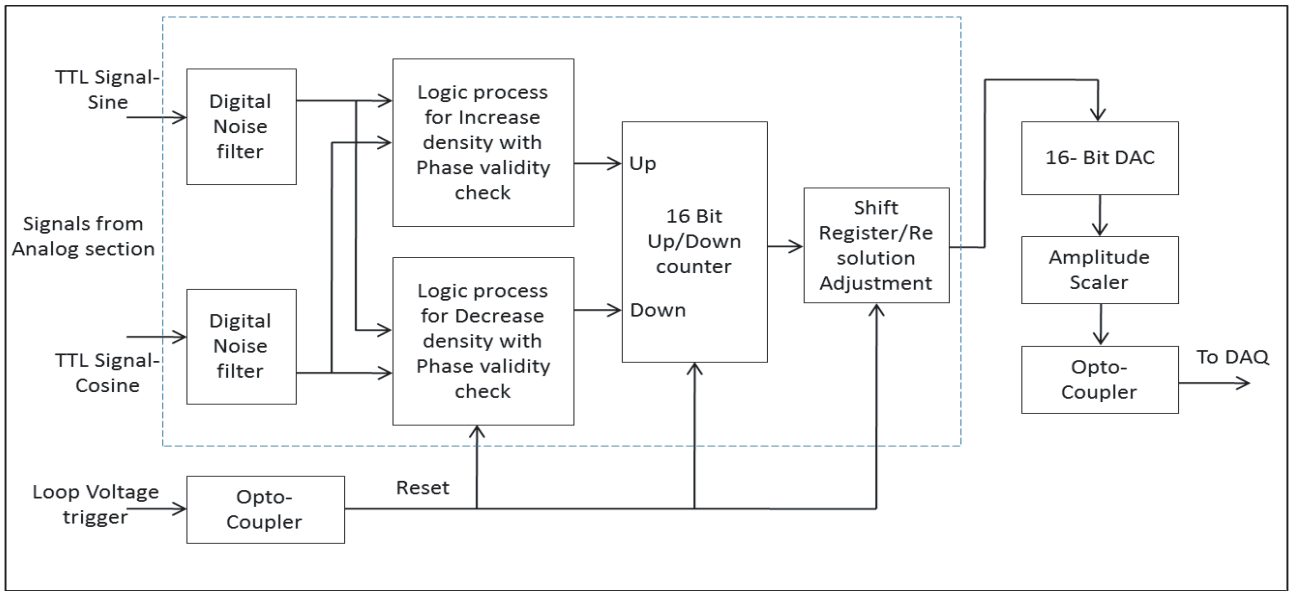


**Figure 3.** Block diagram of digital section and output section.

### *3.2.1. Digital Noise Filter*

The output of the comparator may contain switching noise like chatter. This noise often cause to happen random false count in the counter. To avoid all these kinds of unwanted spike noise, a delayed averaging filter is implemented. This removes all narrow glitches. The rectangular sine/cosine signals are passed through the cascaded shift-registers of the filter, and outputs of these shift-registers are averaged using AND gates and JK flip flops. TA glitch of particular width can be removed through programming. In the present scenario, the width is confined in 5 clock cycles, i.e., 2.5 µs. This can eliminate a noise with maximum period of 4 clock cycles, which 2 µs. This will remove any noise spike of duration less than or equal to 2 µs.

### *3.2.2. Phase Detection*

There will be always a phase difference of 90 degrees between the sine and cosine signals. The density increasing or decreasing is identified by the lead/lag of these signals dynamically. For an increase in density, sine will lead cosine, and during decrease in density, cosine will lead sine. There are four unique conditions for an increasing or decreasing density. These four conditions of an increasing density fringe signal is shown in Fig. 5. For a full fringe, i.e., for 360 degrees, the four unique conditions are monitored continuously at every 0.5 µs. For an increase in density sine signal will lead cosine by about 90 degrees. This process will monitor the first condition 'a' in figure, a rising edge in sine and low state in cosine, and will enable a temporary counter which is also clocked with the master clock at every 0.5 µs and wait for the second unique condition 'b' which is a static state of '1' at sine and rising edge in cosine. Once the condition 'b' is passed, the temporary counter is stopped and will check for the phase validity. So once state 'b' is passed in consequent after state 'a', a half fringe is obtained, and the main fringe data counter is incremented by one. This process will repeat for state 'c' and 'd'. In a full fringe, the main data counter will be incremented by two. The process is same for the decrease in density. The logic block will check for the validity as mentioned above. This is done to avoid false counts which occur due to noise and a cause to have narrow phase differences. The technique is designed to neglect such issues. Presently, the valid phase threshold is set at 15 µs, which is good enough to check valid phase shift of maximum fringe frequency of 15 kHz.

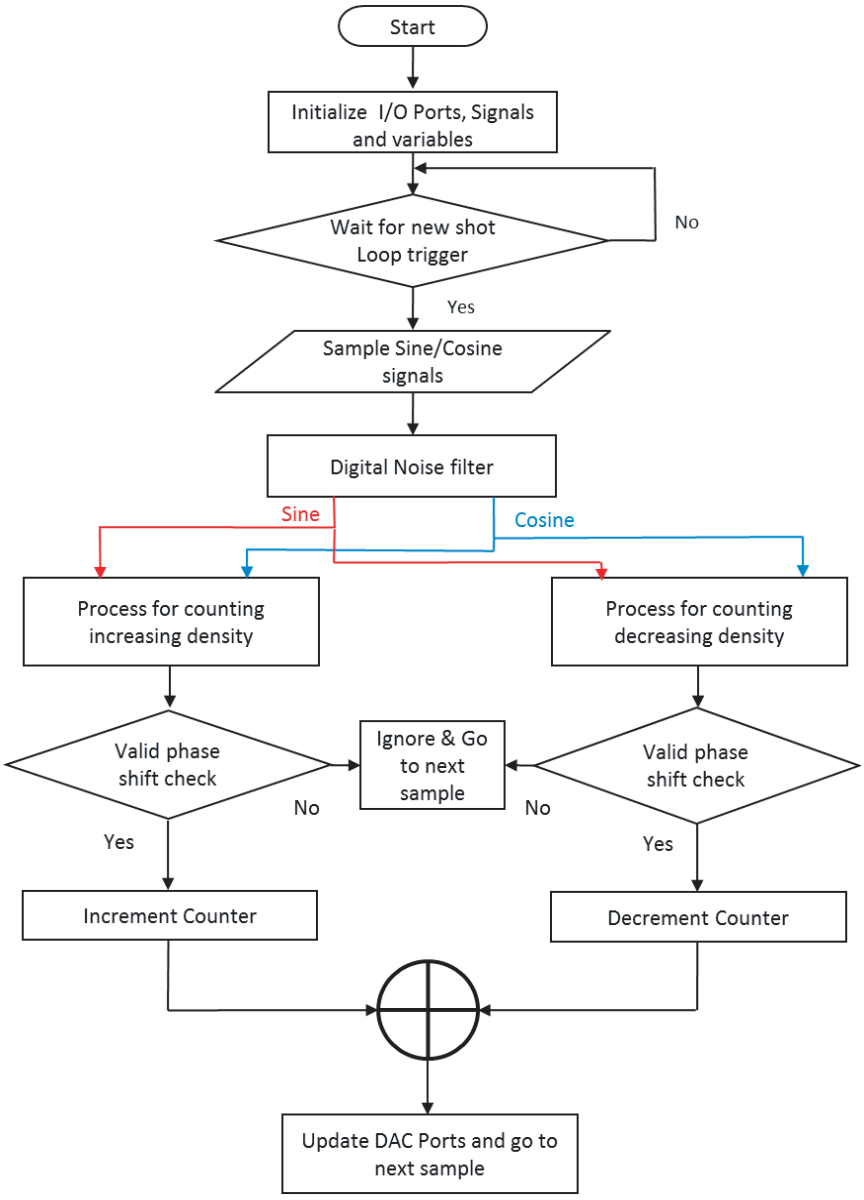


**Figure 4.** VHDL flow chart.

### *3.2.3. Binary Up/Down Counter*

A 16 bit up/down counter is used in this design. Depending on the sine/cosine lead/lag, this counter will increment or decrement. The modulus of the counter is chosen as per the external DAC is used.

### *3.2.4. Shift Register/Resolution Adjustment*

A 16 bit counter can count up to maximum of 32768 counts in both directions. However, in a typical plasma shot at the Aditya tokamak, there can be maximum of 32 counts. So it is necessary to shift the Least Significant Bits (LSBs) to the Most Significant Bits (MSBs) depending on the maximum fringes that can occur in a discharge. This shifting will result in optimum usage of the DAC full scale.

All of the above mentioned logic functions, such as phase validity check timing, width of noise filtering, DAC resolution and shifting, can be easily reconfigured using the Joint Test Action Group (JTAG) programmer.

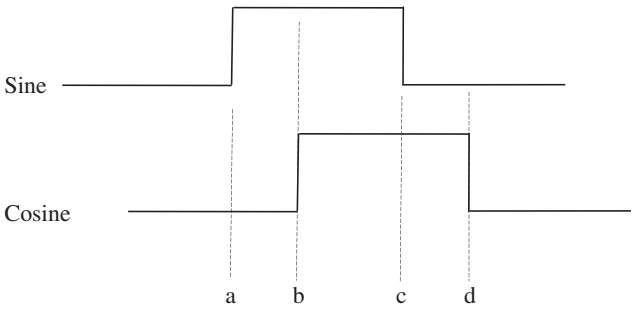


**Figure 5.** The unique four conditions of increasing density.

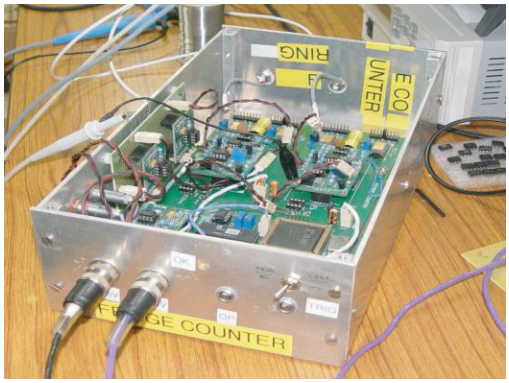

**Figure 6.** The fringe counter circuit.

### 3.3. Output Stage

*3.3.1. DAC and Scaler*

In this circuit DAC AD669 is used, which is a 16 bit DAC. It is configured in bipolar mode and uses offset binary. The output will swing to $+/-10$ V. The maximum input of CAMAC based DAQ system is $+/-5$ V. So the output of DAC is scaled to $+/-5$ V using an active attenuator and buffered to drive the cable to Data Acquisition. The final bit resolution is 312.5 per half fringe. By calculation, a step of 312.5 which is equivalent to $n_e = 0.75 \times 10^{12}\,\mathrm{cm}^{-3}$.

*3.3.2. Opto-Coupler and Driver*

The fringe counter circuit is kept in the Aditya tokamak hall, and Data Acquisition System is in the control room about 25 meters apart. To avoid channel loops among the different diagnostics channels, an analog Opto-coupler circuit is used followed by a line driver. The developed fringe counter circuit is shown in Fig. 6.

## 4. TESTING AND RESULTS

### 4.1. Testing of Digital Logic Section with Xilinx Simulator

The digital logic section is completely tested with Xilinx simulator. A typical snap of simulation window is shown in Fig. 7. Noise spikes are removed by the filters, and this can be seen in the simulation screen shot. Signals pr1 and pr2 show the output of digital filter. In the inputs there are two complete fringes; one for increased density and one for decreased density. We can see clearly that 4 increase counts and 2 decrease counts at the fringe counter output (one fringe corresponds two counts).

### 4.2. Testing of Fringe Counter with Function Generator

The assembled hardware is tested with a function generator. A two-channel function generator, Yokogawa FG300 with independent phase and frequency setting features, is used for testing. Here, the first channel is set as sine source and the second channel set as cosine with a phase shift of 90 deg. The generator is set in burst mode. When a manual trigger is applied, a preset number of bursts of sine and cosine signals will be produced. Typical scope images are shown in Fig. 8. For an increase in density there are four bursts, and correspondingly, there are eight up counts (Fig. 8(a)), and for decrease density five bursts and correspondingly 10 down counts (Fig. 8(b)).

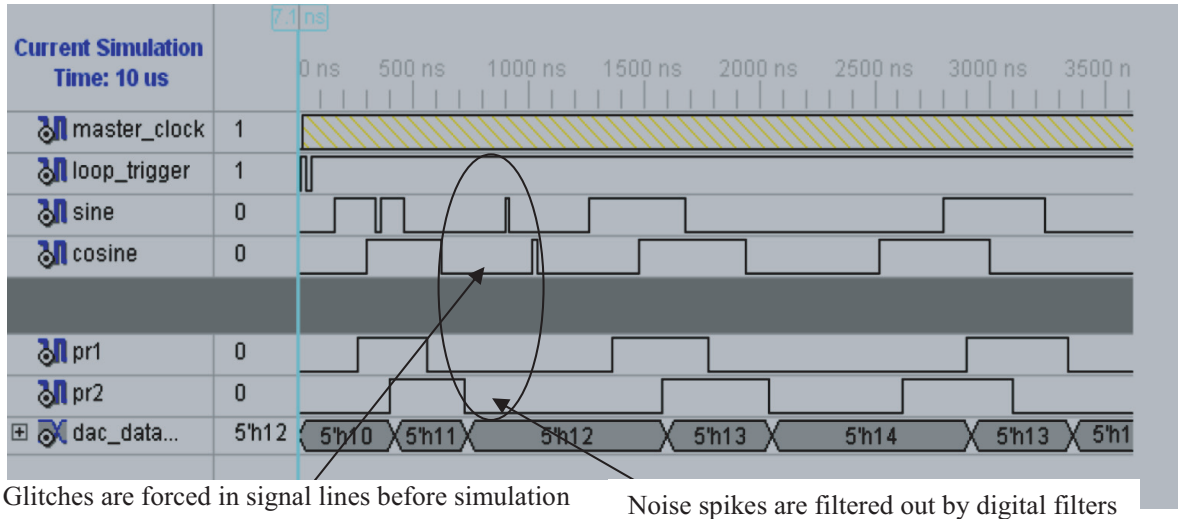


**Figure 7.** Simulation results showing glitches removed also counting for increasing and decreasing.

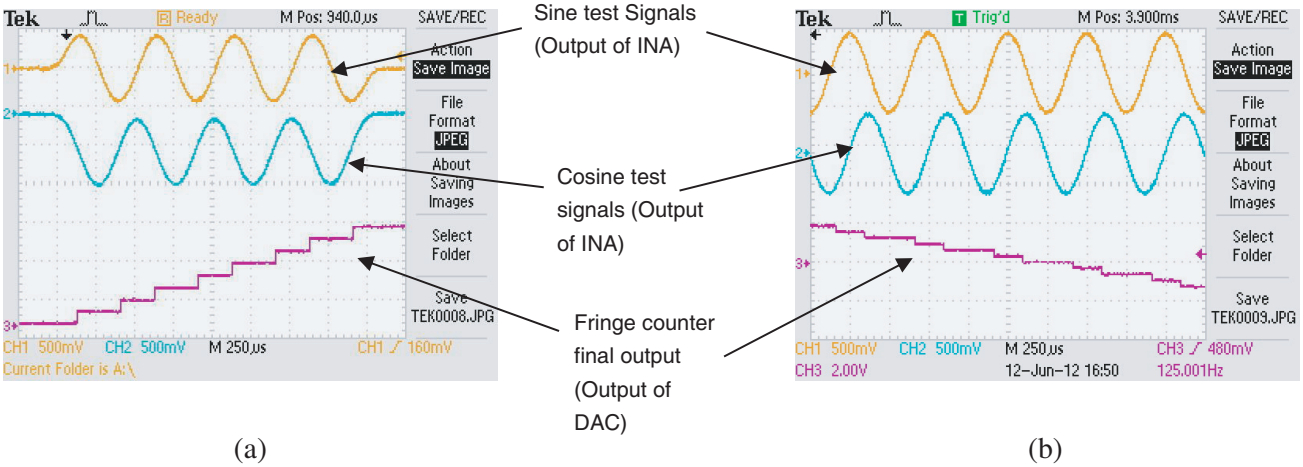


**Figure 8.** Sine/Cosine outputs and final fringe counter output for (a) increasing slope, (b) for decreasing slope.

### 4.3. Testing of Fringe Counter with Prototype of Quadrature Interferometer

The circuit is also tested with a prototype model interferometer setup in laboratory. A photograph of the test setup is shown in Fig. 9. Phase shift variations due to plasma are simulated by moving a Perspex wedge between the transmitting and receiving antennas. Slope of the wedge will introduce an increase or decrease of phase shift. Fringes and corresponding phase shift measured by fringe counter are shown in Fig. 10.

### 4.4. Testing at Aditya Tokomak

The fringe counter circuit is installed with the 3 mm wave interferometer at the Aditya Tokamak. The plasma density is measured online by using fringe counter electronics circuit. Fig. 11 shows (a) the plasma current, (b) fringes ($\sin \Delta\theta(t)$), (c) fringes ($\cos \Delta\theta(t)$) and (d) plasma density measured by fringe counter during discharge.

The measured peak density is $n_e = 0.9 \times 10^{13}\,\mathrm{cm}^{-3}$ in the discharge number 25510 in which the maximum plasma current is 74.3 kA.

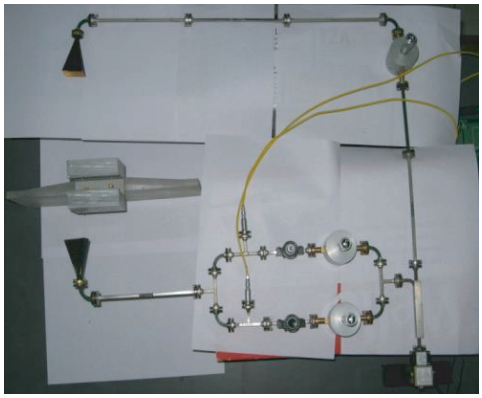

**Figure 9.** Prototype quadrature interferometer system.

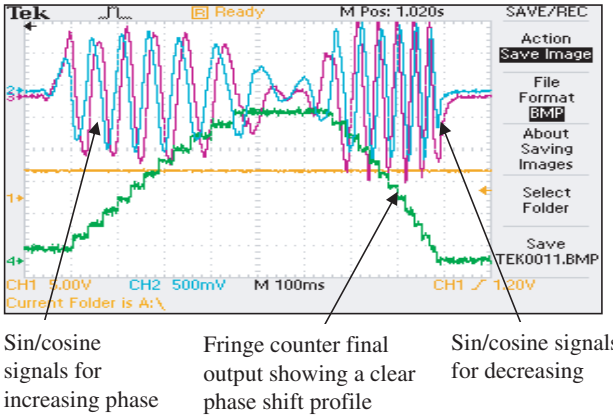


**Figure 10.** Fringes and corresponding phase shift measured by fringe counter.

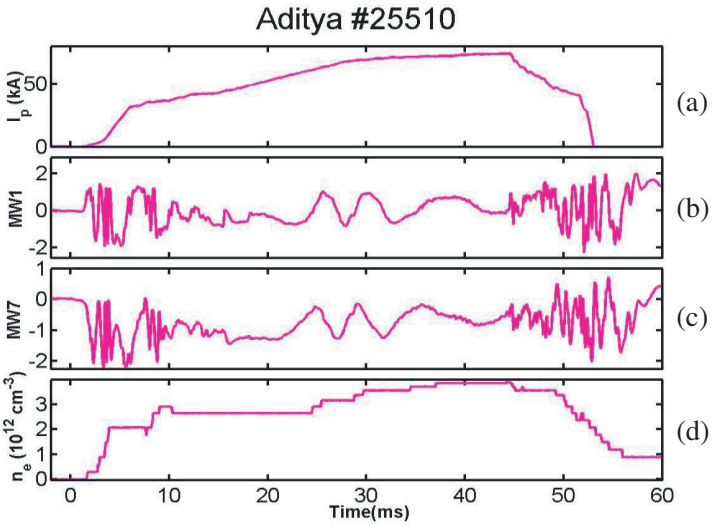


**Figure 11.** (a) The plasma current, (b) fringes ($\sin\Delta\theta(t)$), (c) fringes ($\cos\Delta\theta(t)$) and (d) the plasma density.

## 5. CONCLUSIONS

A 3-mm wave interferometer is designed and developed to measure the electron density online at the central chord of the Aditya tokamak, unambiguously. A real-time processing method of the fringe signals with a hardware logic up/down counting-circuit which converts them to phase shift in units of $\pi$ radians was developed. The microwave circuit of the central chord of a homodyne interferometer system is modified to make a quadrature circuit by using phase shifters and magic tees. It is used to produce the sine/cosine fringe signals. These outputs are converted into pulses and passed to wired logic up/down fringe counter. Digital synchronous logic circuit is implemented in a CPLD, followed by DAC and scaler which produce a voltage proportional to increase or decrease in plasma density in real time. The chord averaged plasma density $n_e = 0.9 \times 10^{13}\,\mathrm{cm}^{-3}$ is measured online at the Aditya tokamak. The output of this circuit will be used for density feedback control of the Aditya tokamak plasma discharges.

## ACKNOWLEDGMENT

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