

# The Analysis and Experimental Investigation of Electromagnetic Characteristics on High Speed Circuit PDN with Multislots

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**Abstract**—The electromagnetic characteristics of a high speed IC power distribution network (PDN) are of vital important with the rapid increasing of operation speed and scale down CMOS manufacturing size, in particular, the fundamental electromagnetic theory including impedance and loop inductance of various designed IC power-plane structures. In addition, the area occupancy ratio of slot (AOROS) of irregular parallel-plane structures with multi-slots plays a key role in PDN impedance and loop inductance, where the influence of AOROS on impedance and loop inductance is investigated for various structures. Moreover, experimental work is carried out to validate the influence of AOROS on impedance and loop inductance of the PDN. The simulation and measurement of impedance are performed up to 10 GHz, and a good agreement is obtained between the simulation and experiment.

## 1. INTRODUCTION

With the advancement of electronic technology, electronic products are developing towards lightweight, miniaturization, multifunction, with high reliability and high integration. High-speed interconnect effects such as signal integrity (SI), power integrity (PI) and electromagnetic compatibility (EMC) have become the dominant factors limiting the overall performance of high speed circuits and system on package. Power integrity problems have become one of the bottlenecks of restricting modern design of printed circuit board (PCB). The analysis of the impedance, loop inductance and parasitic parameters of power distribution network (PDN) is the key for solving power integrity problems. The analysis of PDN is based on the input impedance observed by the integrated circuit (IC) looking into the PDN, and the performance of PDN is evaluated by comparing the input impedance with the target impedance [1, 2].

The electromagnetic performance of PDN is essential in PCB design, where in a single plane pair, one plane is referred as reference plane and the other as the power plane. There are several different formulations used for modeling the electromagnetic performance of plane-pairs based on numerical methods such as transmission line modeling (TLM) approach like [3, 4], finite difference time domain (FDTD) models like [5] and the finite element method (FEM) [6]. These methods require long computing time and huge resources for calculating the electromagnetic radiation field, which cannot satisfy the needs of fast simulation in solving complex problems. Partial element equivalent circuit (PEEC) is able to model multi-level problems with fine mesh and leads to an efficient and accurate circuit solution in both the frequency domain and time domain in PCB PDN analysis [7].

In this paper, the method of PP-PEEC is used to analyze the impedance and loop inductance of PDN with multi-slot structures [8, 9]. Section 2 introduces the application and impedance analysis of the PP-PEEC method in an irregular parallel-plane structure with multi-slots. Section 3 presents the experimental validation of effects of the AOROS on impedance and loop inductance. Finally, Section 4 is conclusion.

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## 2. IMPEDANCE ANALYSIS OF PDN

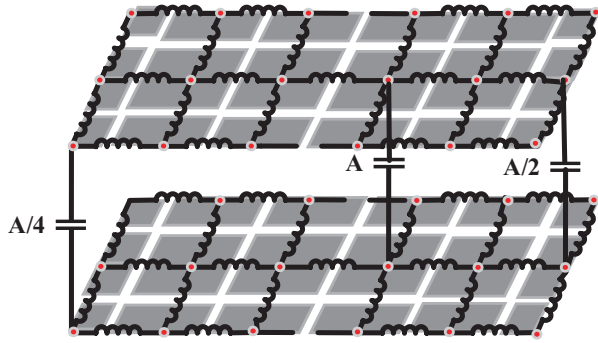
### 2.1. PP-PEEC Method in Irregular Parallel-Plane

The PP-PEEC method is a 2D PEEC methodology [10] which converts electromagnetic field problems into circuit problems. This method is widely used to analyze PDN of parallel-plane structure that can be subdivided into many cell pairs expressed by partial inductances as shown in Figure 1. These partial inductances are connected to the nodes through branches, and the branches correspond to the edge of the cells. The partial inductance between the cells can be computed analytically [6, 11, 12]. The equivalent interconnected capacitance between the corresponding nodes pairs in different planes also called partial capacitance is expressed by  $C_p = \varepsilon A/h$ , where  $A$  is the cell area,  $h$  the plane separation, and  $\varepsilon$  the permittivity of dielectric substrate. The capacitance plate is shown by the gray area where the capacitance is proportional to the full cell  $A$ , and the corner cell has area  $A/4$  while the side cells areas are  $A/2$ .

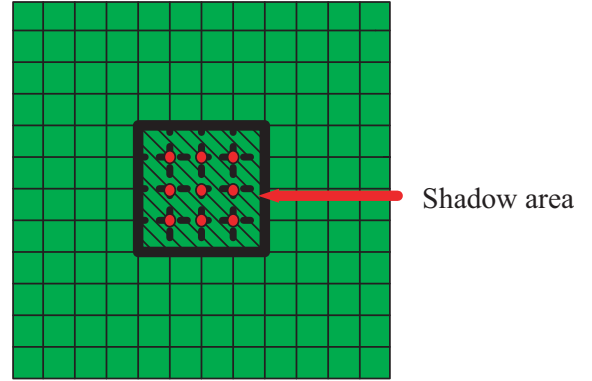
The equivalent circuit equation of the structure can be set up using a modified nodal analysis (MNA) matrix equation [11] which is composed of Kirchhoff's voltage law (KVL), Kirchhoff's current law (KCL), and partial inductance matrices. The circuit equation is solved using the MNA formulation which is given in Eq. (1)

$$\begin{bmatrix} B & A^T \\ A & G \end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix} = \begin{bmatrix} p \\ q \end{bmatrix} \quad (1)$$

The  $B$  matrix is zero if only independent sources are considered. The  $A$  matrix with only 0, 1 and  $-1$  elements is determined by the connection of the voltage sources. The  $G$  matrix is determined by the interconnections between the circuit elements. The  $v$  vector holds the unknown voltages. The  $i$  vector holds the unknown currents through the voltage sources. The  $p$  vector is the external current source into the corresponding node, and the  $q$  vector is equal to the corresponding independent voltage source. If there is no current source or no independent voltage source, the values of  $p$  and  $q$  are zero, respectively. By solving the matrix, the voltage at each node and the current in each branch, which are the unknowns, can be obtained.



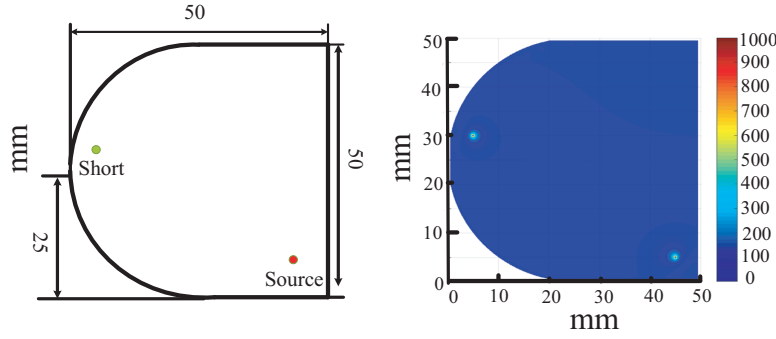
**Figure 1.** PP-PEEC circuit with inductances and capacitances.



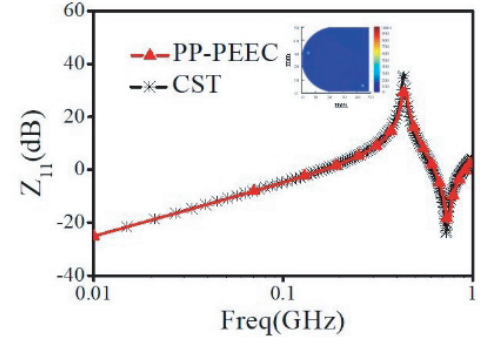
**Figure 2.** Uniform mesh model with deleted area (shaded areas).

Based on the principles described above, the PP-PEEC method can also be used in an irregular parallel-plane structure. As shown in Figure 2, shadow section denotes the deleted region, and red dot and dotted line denote related nodes and branches, respectively. When the shadow area in the middle of the structure is deleted, the red nodes as well as the relevant branches should be removed. The deleted area can be made up of arbitrary triangle and rectangle or any combination of two shapes.

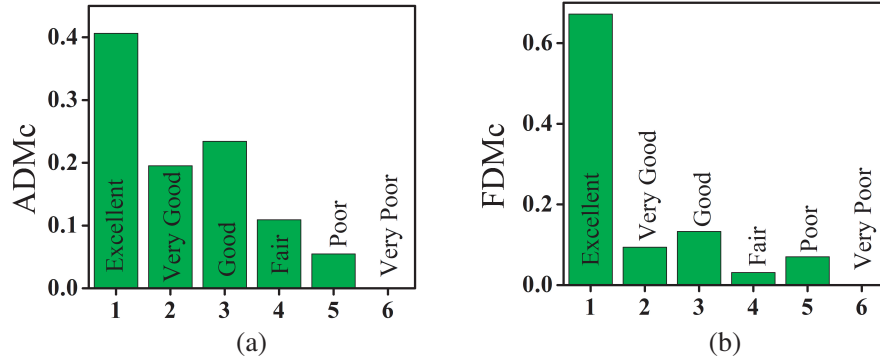
Figure 3 shows an irregular parallel-plane structure obtained by deleting many rectangles. The impedance parameter calculated by PP-PEEC method compared with Computer Simulation Technology (CST) [13] in frequency range from 0.1 GHz to 1 GHz is shown in Figure 4. It can be seen from Figure 3 that there is a very good agreement between CST and PP-PEEC method. According to the IEEE



**Figure 3.** Irregular parallel-plane structure with removed sections.



**Figure 4.** PDN impedance of the proposed structure.



**Figure 5.** Feature selective validation results between PP-PEEC and CST: (a) ADMc comparison for Figure 4 at grade = 4 and spread = 4, and (b) FDMc comparison for Figure 4 at grade = 3 and spread = 3.

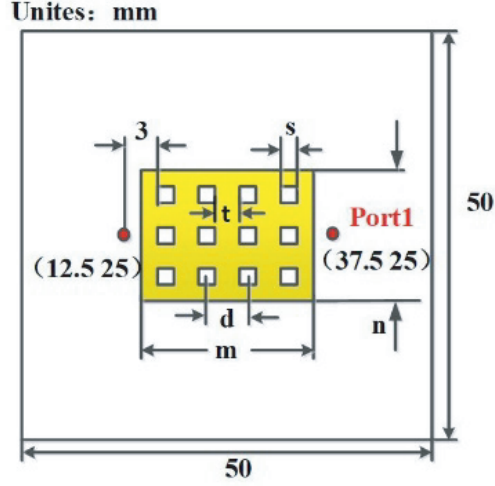
standard P1597.1 [14], the simulation and measurement results are quantified in Figure 5 by using the feature selective validation techniques [15, 16]. Both amplitude difference measure (ADM<sub>c</sub>) and feature difference measure (FDM<sub>c</sub>) show good agreement between CST and PP-PEEC with the associated values of grade and spread.

## 2.2. Analysis of PDN Impedance for Multislot Parallel-Plane

The top view of a parallel-plane structure with multi-slots is shown in Figure 6, and the shape of each slot is square. The area containing multi-slots is marked in yellow and placed in the middle of the board.

The board is designed with two vias. One is a source via for the power injection port, and the other is a short via connecting two planes. The length of the slot is  $s$ ; the spacing between two adjacent slots is  $t$ ; the center distance of two adjacent slots is  $d$ , and  $d$  is equal to  $s$  plus  $t$ . The size of the square yellow area is  $m \times n$ , and the area occupancy rate of all slots to the yellow square area is defined as AOROS.

In this work, the specific parameter values are listed in Table 1. The board is designed as 50 mm  $\times$  50 mm, and the size of the square yellow area is 21 mm  $\times$  16 mm. Table 2 shows the loop inductance of the model in Figure 5 at the frequency of 100 MHz. The AOROS calculation result is 14.29%, and the loop inductances calculated by PP-PEEC method and CST are 503 pH and 481 pH, respectively. The deviation in loop inductance calculated by PP-PEEC and CST is only 4.4%, which indicates that the PP-PEEC method has good accuracy for calculating loop inductance of parallel-plane structure with multi-slots.



**Figure 6.** The parallel-plane structure with multislot.

**Table 1.** Parameter of the structure.

Board size (mm)	$50 \times 50$
Source via (mm)	(37.5, 25)
Short via (mm)	(12.5, 25)
$m$ (mm)	21
$n$ (mm)	16
$s$ (mm)	2
$t$ (mm)	3
$d$ (mm)	5

**Table 2.** Loop inductance of the model in Figure 5 at the frequency of 100 MHz.

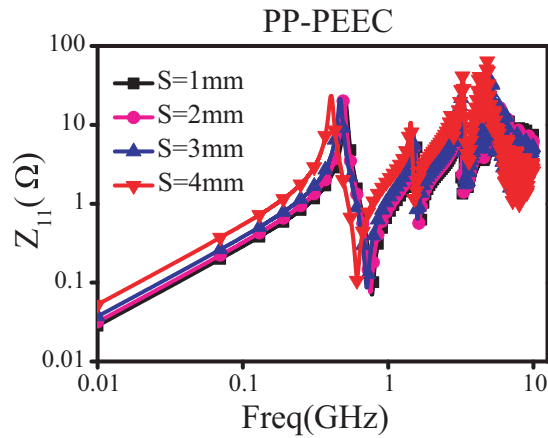
AOROS (%)		14.29
Loop inductance (pH)	PP-PEEC	503
	CST	481
Deviation of PP-PEEC and CST		4.4

**Table 3.** Loop inductance of different size slot at the frequency of 100 MHz.

$d$ (mm)	5	5	5	5
$s$ (mm)	1	2	3	4
AOROS (%)	3.57	14.29	32.14	57.14
Loop inductance (pH)	460	503	593	837

Table 3 shows the AOROS and loop inductance for slots with different sizes of the above structure at the frequency of 100 MHz. The conclusions obtained from the table are that if keeping “ $d$ ” as a constant with a value of 5 mm and changing the “ $s$ ” from 1 mm to 4 mm, the AOROS increases from 4% to 57%, and the loop inductance changes from 460 pH to 837 pH.

Figure 7 denotes the self-impedance  $Z_{11}$  curves of the structure with various “ $s$ ” calculated by PP-PEEC in frequency range from 0.01 GHz to 10 GHz. It shows that impedance value increases with



**Figure 7.** Comparison of the calculated input impedance by PP-PEEC method with different  $s$ .

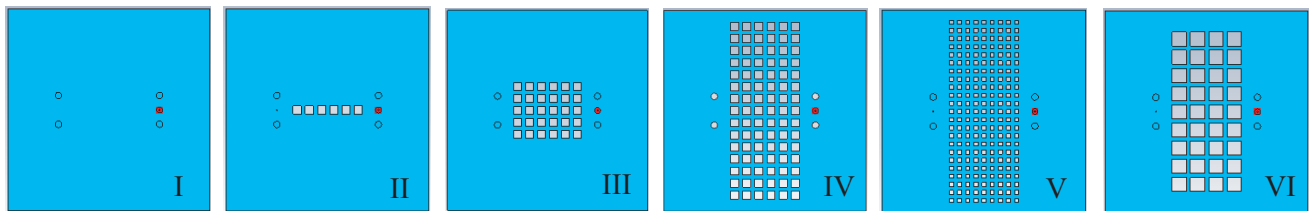
the increase of “ $s$ ” parameter.

As a consequence, it can be seen from Table 3 and Figure 7 that if keeping  $d$  as a constant, the AOROS increases with the increase of “ $s$ ” parameter, and the self-impedance  $Z_{11}$  and loop inductance increase rapidly with the increase of AOROS.

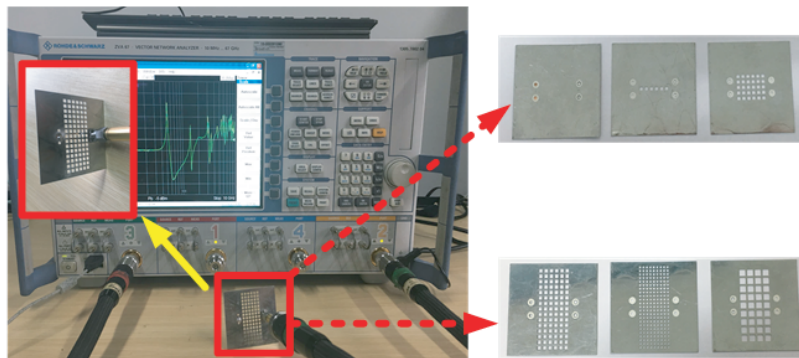
The above conclusions are all derived because slots prevent the current path from source to short via.

### 3. EXPERIMENTAL VALIDATION

In order to verify the effect of AOROS on self-impedance and loop inductance, different pattern test boards are designed and fabricated as shown in Figure 8. The designed test boards consist of two layers with a source via and a short via connected between power and ground. The dimensions of all the



**Figure 8.** The designed test structures with different pattern.

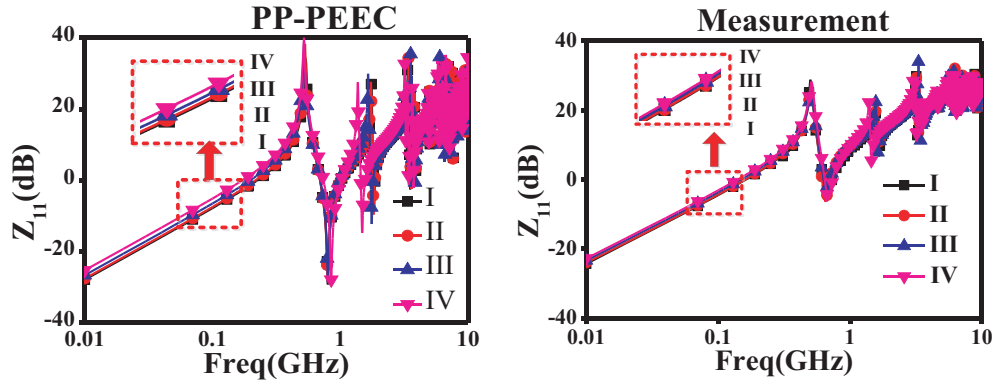


**Figure 9.** Test bench of the impedance measurement.

boards are 50 mm  $\times$  50 mm with thickness of 0.289 mm. The conductor planes are made of copper with thickness of 0.0175 mm. The dielectric substrate has relative permittivity  $\epsilon_r = 3.48$  and dielectric loss tangent  $\delta = 0.0037$  with thickness of 0.254 mm. The size of the square slot is 2 mm  $\times$  2 mm in II, III, IV models and 1 mm  $\times$  1 mm in V model, 3.5 mm  $\times$  3.5 mm in VI model. As depicted in Figure 6, the yellow square area is 19 mm  $\times$  45 mm in these models. The source via and short via are located at point (37.5 mm, 25 mm) and point (12.5 mm, 25 mm), respectively. The test frequency range is from 0.01 GHz to 10 GHz. The designed test boards are measured by VNA (R&S ZVA67) as shown in Figure 9. The influence of AOROS is analyzed in two situations: (1) The lengths of the slots are the same, and the spacings between two adjacent slots are also the same, i.e., with the same “ $s$ ” and the same “ $t$ ”. (2) The lengths of the slots are different, and the spacings between two adjacent slots are the same, i.e., with different “ $s$ ” and the same “ $t$ ”.

### 3.1. Case 1: The Boards with the Same “ $s$ ” and Same “ $t$ ”

The impedance curves of test boards I, II, III, and IV with the same “ $s$ ” and “ $t$ ” calculated by PP-PEEC method and measured results in frequency range from 0.01 GHz to 10 GHz are depicted in Figure 10. As shown in Figure 10, the impedance magnitudes with more slots are higher than that with fewer slots in low frequency, and the first peak resonant frequencies for all the cases are not changed. Additionally, the conduction current density of test boards I, II, III and IV can also be determined from the PP-PEEC modeling as shown in Figure 11. It can be seen that as the number of slots increases, the current flow paths become larger which results in a greater loop inductance.



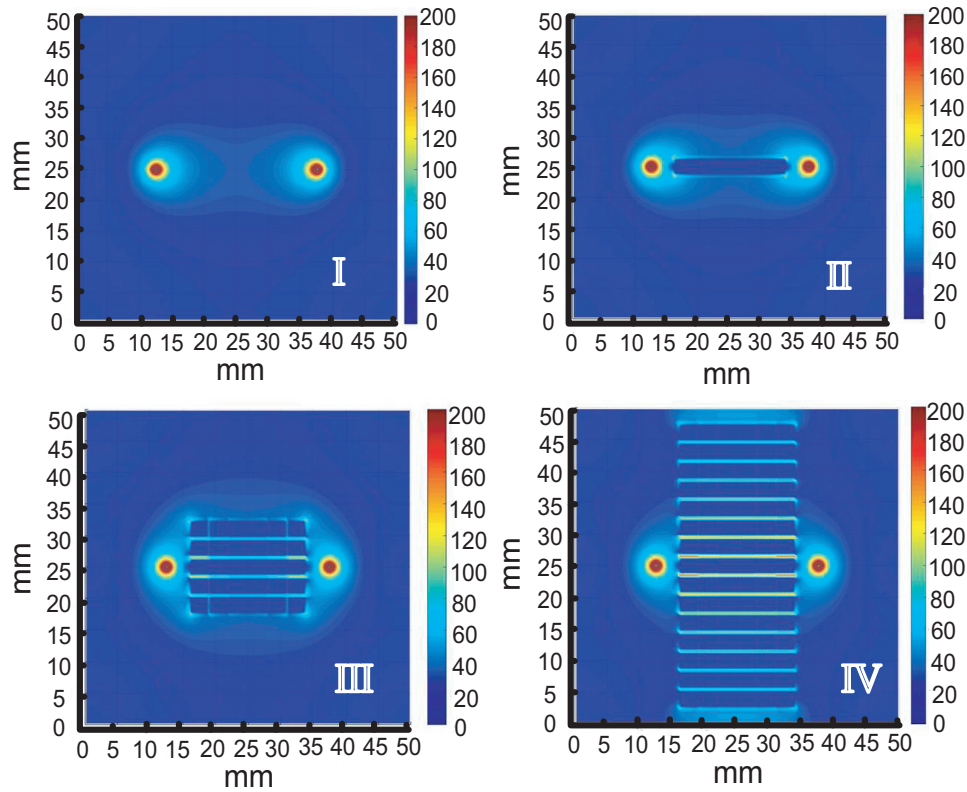
**Figure 10.** The variation of impedance for test structure I, II, III, IV by PP-PEEC method and measurement.

Table 4 shows the loop inductance of test boards I, II, III, and IV calculated by PP-PEEC, CST and measurement at the frequency of 100 MHz. It can be seen obviously from the data in the table that if the boards have the same “ $s$ ” and same “ $t$ ”, loop inductance increases with the increase of AOROS. Thereby, it can be concluded that the changing of loop inductance depends on AOROS. In addition, Table 4 shows that the deviations of the test boards calculated by CST and PP-PEEC are only 6.5%, 8.8%, 3.8%, 6.2%, respectively.

The comparison of the results obtained from PPPEEC, CST and measurement for test boards I, II, III and IV are shown in Figure 12. The results obtained by measurement show a good consistency with those obtained by the PP-PEEC and CST.

### 3.2. Case 2: The Boards with Different “ $s$ ” and Same “ $t$ ”

The impedance curves of test boards IV, V and VI with different  $s$  and same  $t$  calculated by PP-PEEC method and measured results in frequency range from 0.01 GHz to 10 GHz are depicted in Figure 13. The conduction current density of test boards IV, V, VI can also be determined from the PP-PEEC modeling as shown in Figure 14.



**Figure 11.** The current density over the area fill from PP-PEEC modeling.

**Table 4.** Loop inductance of case1calculated by PP-PEEC, CST and measurement at the frequency of 100 MHz.

Board Type		I	II	III	IV
$t$ (mm)		1	1	1	1
$s$ (mm)		0	2	2	2
AOROS (%)		0	3.1	15.7	47.1
Loop Inductance (pH)	PP-PEEC	637	662	740	867
	CST	681	726	769	813
	Measured	963	1004	1078	1157
Deviation of PP-PEEC and CST (%)		6.5	8.8	3.8	6.2

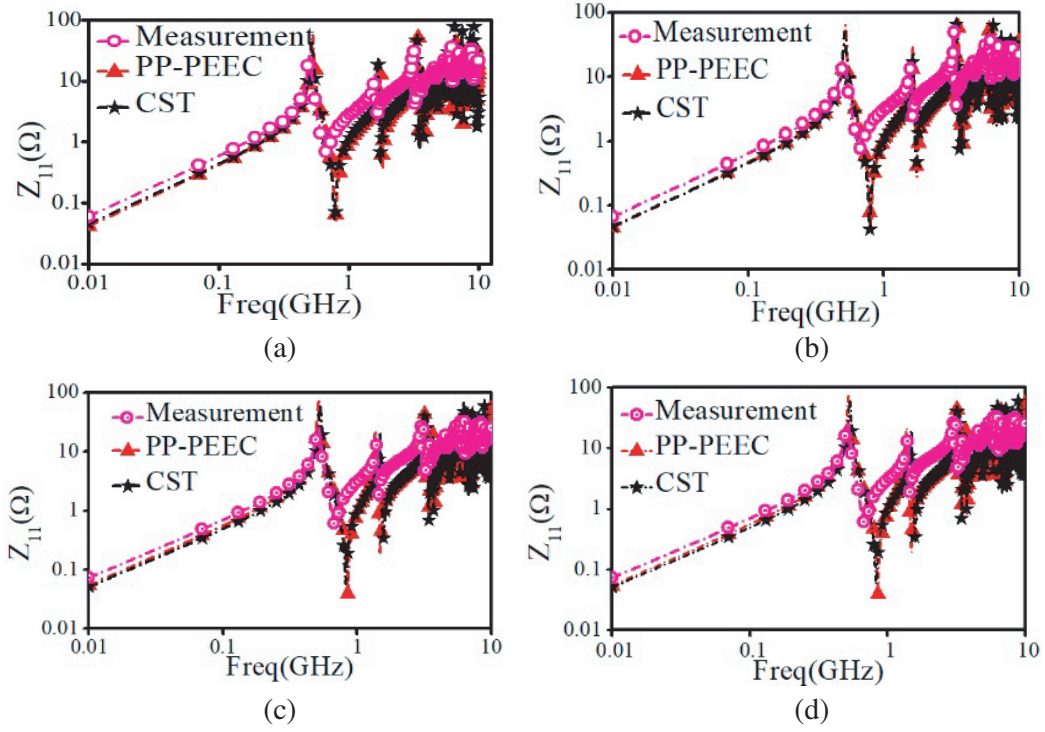
As shown in Figure 13, the impedances of test boards IV, V and VI increase with the increase of AOROS and have the same first peak resonant frequencies. As can be seen from Figure 14, if keeping “ $s$ ” unchanged, the loop inductance will increase with the increase of slot size.

Table 5 shows the comparison of loop inductances of test boards IV, V and VI calculated by PP-PEEC, CST and measurement at the frequency of 100 MHz. The variation in loop inductance with AOROS is the same as that of case 1, and the deviations of the boards are 4.3%, 6.2%, 2.2%, respectively. Figure 14 shows the comparison of the results obtained from PP-PEEC, CST and measurement for test boards IV, V and VI, and shows a good agreement among PP-PEEC, CST and measurement.

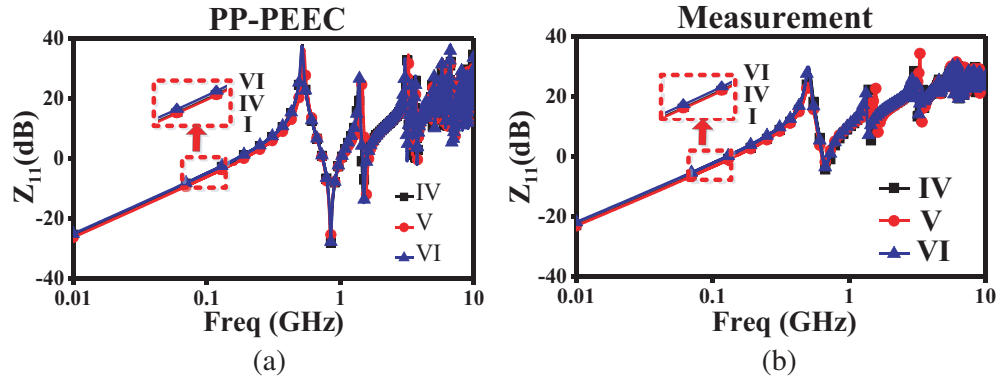
Figure 15 depicts the comparison of the results obtained from PP-PEEC, CST and measurement for test boards IV, V, and VI.

It can be seen from Figure 13 and Figure 15 that taking the manufacturing errors and the measuring errors into account, the measured results match well with the results of CST and PP-PEEC.

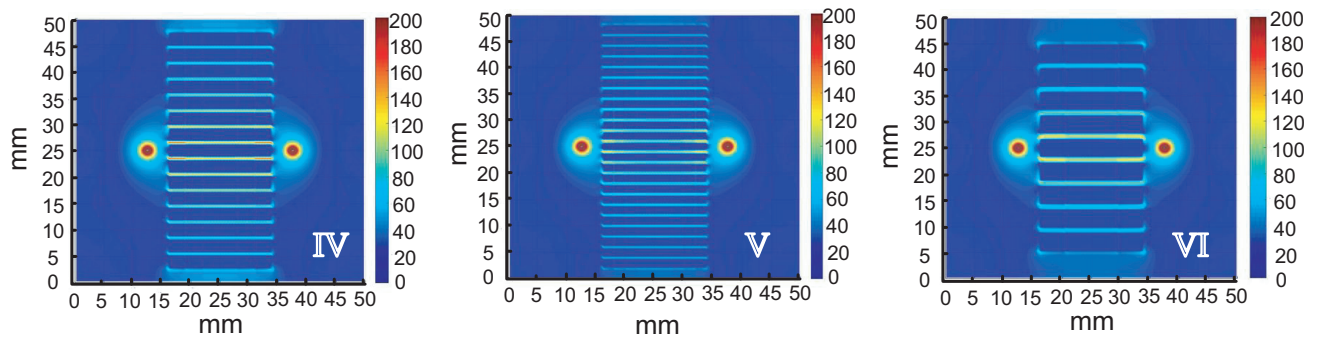




**Figure 12.** Simulated and measured results for test structure. (a) Structure I. (b) Structure II. (c) Structure III. (d) Structure IV.



**Figure 13.** The variation of impedance for test structures IV, V, VI by (a) PP-PEEC method and (b) measurement.

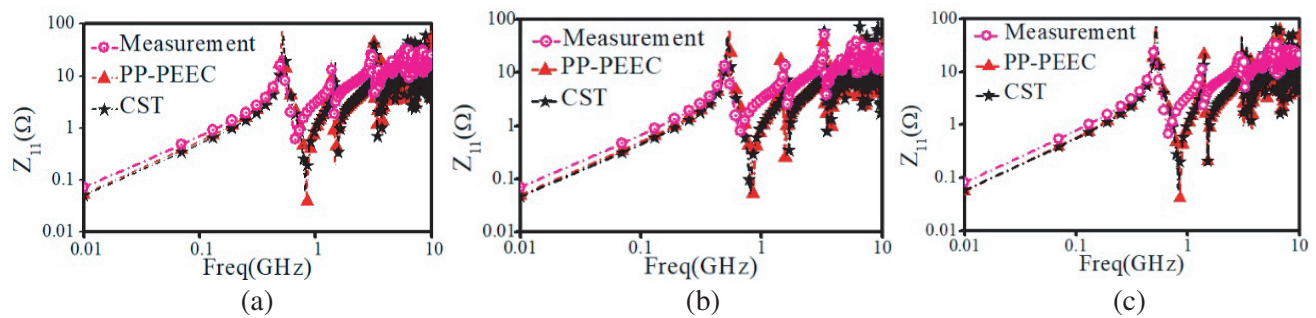


**Figure 14.** The current density over the area fill from PP-PEEC modeling.



**Table 5.** Loop inductance of case 2 calculated by PP-PEEC, CST and measurement.

Board Type		V	IV	VI
$t$ (mm)		1	1	1
$s$ (mm)		1	2	3.5
AOROS		27.1%	47.1%	57.6%
Loop Inductance (pH)	PP-PEEC	785	867	897
	CST	751	813	917
	Measured	1125	1157	1297
Deviation of PP-PEEC and CST		4.3%	6.2%	2.2%

**Figure 15.** Simulated and measured results for test structure. (a) Structure IV. (b) Structure V. (c) Structure VI.

#### 4. CONCLUSIONS

The electromagnetic key parameters, impedance and loop inductance of high speed IC and Circuit irregular parallel-plane structures are theoretically investigated, and various electromagnetic characteristics are presented. The influence of AOROS on the electromagnetic parameters impedance and loop inductance are also analyzed and experimentally verified. The results demonstrate the impedance and loop inductance increasing with the increase of AOROS for parallel-plane structure with multi-slots. This research work further demonstrates that the field-circuit PP-PEEC method is an accurate and efficient approach to calculate the parallel-plane impedance and loop inductance, and helpful for modeling and analyzing the high speed IC and circuit PDN performance.

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