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Design Technique for Varactor Analog Phase Shifters with Equalized Losses

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Abstract—The paper presents a novel design technique for reflection-type varactor analog phase shifters based on tunable reflective loads. The reflective load comprises two similar tuning stubs with incorporated varactor diodes, where each varactor can be tuned independently. It is shown that by an appropriate losses equalization method applied together with a specific independent varactors control algorithm it is possible to achieve the desired 360° phase shift with stabilized losses, which are significantly lower compared to the well-known single-channel design. We derive and discuss in details main design relations arisen from the complex plane reflection coefficient consideration. The presented technique is first verified by circuit simulation in ADS, and comparison with the classical single-channel design is also considered. Next, we develop experimental prototypes of a reflective load and a full phase shifter based on a packaged silicon varactor diode for operation in C-band with 5.8 GHz central frequency. Experimental and theoretical results are in perfect agreement. Moreover, we have found that the bandwidth of the proposed phase shifter can be greatly enhanced if the reflective loads are tuned at each sub-band using a unique optimal tuning path. The suggested reflective load demonstrates the total bandwidth of 10.3% and the instantaneous bandwidth of 1.7% (sub-band), where inside each sub-band measured ripple at the central frequency is around 0.5 dB, and the maximum overall ripple is below 0.8 dB.

1. INTRODUCTION

Today analog phase shifters (PSs) are widely employed in a variety of microwave and mm-wave radio electronic systems. In particular, analog PSs are very attractive for front end modules of phased antenna arrays, phase modulators, phase-locked loops and a lot of other applications [1]. Analog PSs usually compete with their discrete (digital) counterparts, which possess more stable electrical performance due to digital control [2, 3]. However, for many applications where such requirements as low losses and precise phase adjustment are imposed on the system, developers usually employ analog PS architecture [1, 4]. Another important advantage of analog PSs is a compact size required to achieve 360° (full-cycle) phase shift. This enables direct integration of the analog PS with radiating elements of phased antenna arrays [5–7], providing a compact array unit cell design. A comprehensive set of requirements is usually demanded from the analog PS in terms of matching, transmission losses variation (ripple), average losses and achievable phase shift.

In this paper we consider the passive analog PS based on tunable varactor diodes. Generally, there are several types of varactor PSs most extensively used in modern microwave circuits. One of them, the simplest and the most compact, is a filter-type varactor PS [4, 8]. Despite its advantages, this

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PS type suffers from mismatching with a feeding line and non-linearity of phase-frequency response. Another well-known implementation is a reflection-type PS based on quadrature hybrid coupler (HC) with reflective loads (RLs) connected to coupler's (or circulator's) shoulders [9–18]. A pervasive study of 360° reflection-type PS was first given by Garver in [9] where the technique for losses equalization was presented. The main drawbacks of the aforementioned PS design are narrow bandwidth and relatively high insertion losses caused by two equalization resistors. Next, in subsequent works, authors widely considered and improved Garver's design [10–15]. In [11], Garver's approach was extended by introducing a HC with impedance transformation but only for a single-varactor RL, with a total phase shift being less than 360°. In [12] authors replicated a full-cycle PS employing an impedance transforming HC. In [13, 14] researchers focused on co-design of a non-equal coupler and the classical RL with a goal to achieve a wider bandwidth and a more compact size. For this purpose, authors in [13] suggested to use a non-quarter-wave coupler, and work [14] employs a specific vertically installed coupler structure. Unfortunately, despite the wideband performance by 10 dB return loss level, these structures are unequalized and demonstrate considerable transmission ripple of more than 1.5 dB at central frequencies in S-band, even if using high performance GaAs varactors [13]. Another technique, pursuing a goal to achieve a frequency stabilized phase response, is based on the application of a RL with two parallel varactor-loaded stubs [15–17]. The main drawback of this approach is unequalized transmission losses, especially considerable for PSs with a wide relative phase shift. A useful PS design was suggested in [18], where authors explored a reflection-type PS based on an impedance transforming HC and a reflecting π-network with three varactors. Presented results evidence achieved losses improvement. Nevertheless, no equalization technique was employed, and the measured ripple level is about 1.2 dB in S-band.

In this study, we concentrate on the reflection-type PS with a conventional 3-dB quadrature coupler and propose a novel equalized RL design comprising two varactor diodes with independent tuning capability. Previously, the idea of an independent varactors control was considered in [19], where authors showed that at the central frequency a specifically designed RL can have zero transmission ripple, with average insertion losses being significantly lower compared to the RL from [9]. Below we will generalize the presented approach, showing the analytical derivation of main relations, and enhance the approach for a wideband RL operation. We should mention that somewhat similar idea was discussed earlier in [20] for the lumped π-network, where authors demonstrated the technique for PS losses equalization. However, the RL itself was not equalized, and the suggested technique employed four independent control channels.

The presented paper is organized as follows. In Section 2, we discuss the classical single-channel design of RL and consider a generalized equalization technique. In Section 3, a topology of a novel RL structure and a varactors control algorithm are studied in details. In Section 4, we present and discuss measured results for the fabricated RL and the full PS. Here, the frequency performance of the RL is also addressed, and we show that RL bandwidth can be drastically enhanced if a specific control algorithm is applied at each frequency sub-band. Finally, Section 5 summarizes main conclusions of this paper.

2. THE CLASSICAL DESIGN OF REFLECTIVE LOAD AND A NOVEL EQUALIZATION TECHNIQUE

First, we will consider the classical design of RL from [9] and will generalize the approach for a full varactor equivalent circuit. In Fig. 1, the common block diagram of the reflection-type PS is depicted, where two RLs are connected to two ports of a quadrature HC. Both RLs are tuned simultaneously by applying control DC voltage to the control port. Fig. 2 reveals a circuit diagram of the corresponding RL. The RL comprises two similar tuning stubs, where each stub is a series connection of a varactor diode $VD_{1,2}$ and a short-circuited inductance $L_{s1,2}$. Two tuning stubs are connected through a quarter-wavelength transmission line TL_0. Each stub may optionally have an equalization circuit with admittance Y_{eq} connected in parallel. To alleviate the circuit diagram, a filter decoupling microwave and control ports is not depicted in Fig. 2. Also, in the further consideration we assume all transmission lines lossless. Before moving to the full RL structure, it is reasonable to examine electrical performance of the single tuning stub.

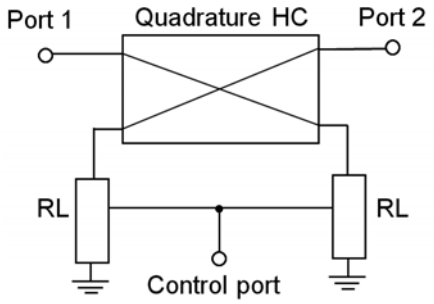


Figure 1. Block diagram of the considered reflection-type PS with a single control channel.

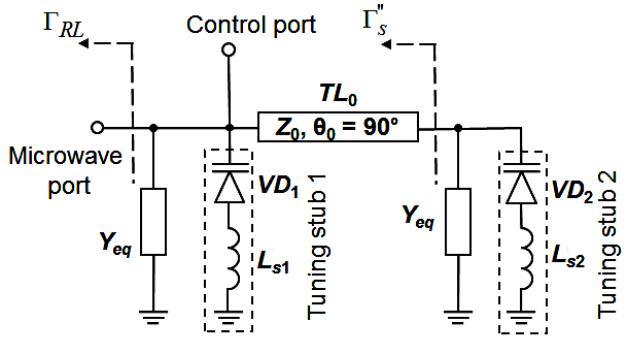
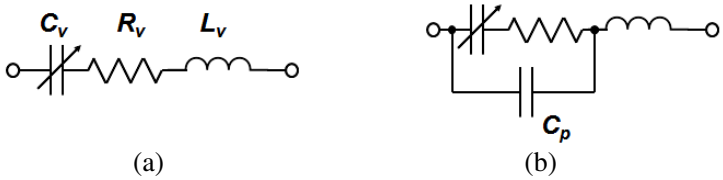


Figure 2. Circuit diagram of the RL with a single control channel.



(a) (b)

Figure 3. Varactor diode circuit representation: (a) the simplified and (b) the full equivalent circuits.

At the relatively low frequencies, varactor diode can be represented by a simplified equivalent circuit (Fig. 3(a)), where capacitance C_v is varied from $C_{v\min}$ to $C_{v\max}$, R_v — diode resistance, L_v — packaging inductance. Next, we will consider the PS performance at a central frequency f_0(ω_0 — its angular equivalent). For the given reference impedance Z_0, the stub input reflection coefficient Γ_s has the form

$$\Gamma_s(C_v) = \frac{Y_0 - Y_s(C_v)}{Y_0 + Y_s(C_v)}, \tag{1}$$

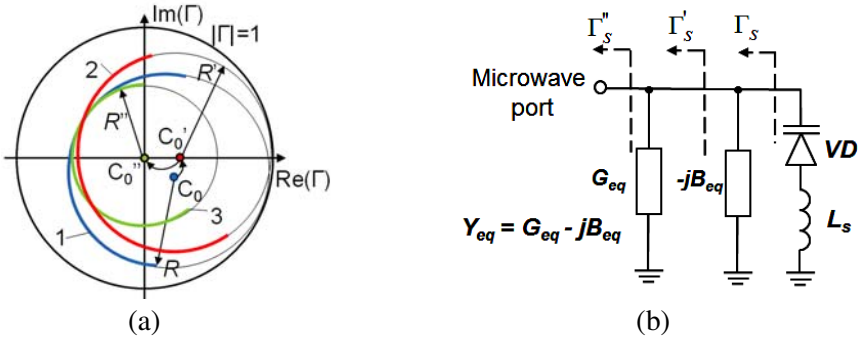
where $Y_s(C_v)$ — a full complex admittance of the stub, $Y_0 = 1/Z_0$. We can find from Eq. (1) that, if the stub comprised only a varactor diode with a relatively low parasitic L_v, the phase variation of Γ_s would always be lower than 180° [5, 9]. For this reason, an additional series inductance is usually employed to achieve 180° total phase shift. To find the required value of L_s, the following equation should be resolved [9]:

$$\left(-\frac{1}{\omega_0 C_{v\min}} + X\right) = -Z_0^2 / \left(-\frac{1}{\omega_0 C_{v\max}} + X\right), \tag{2}$$

$$X = \omega_0 (L_v + L_s). \tag{3}$$

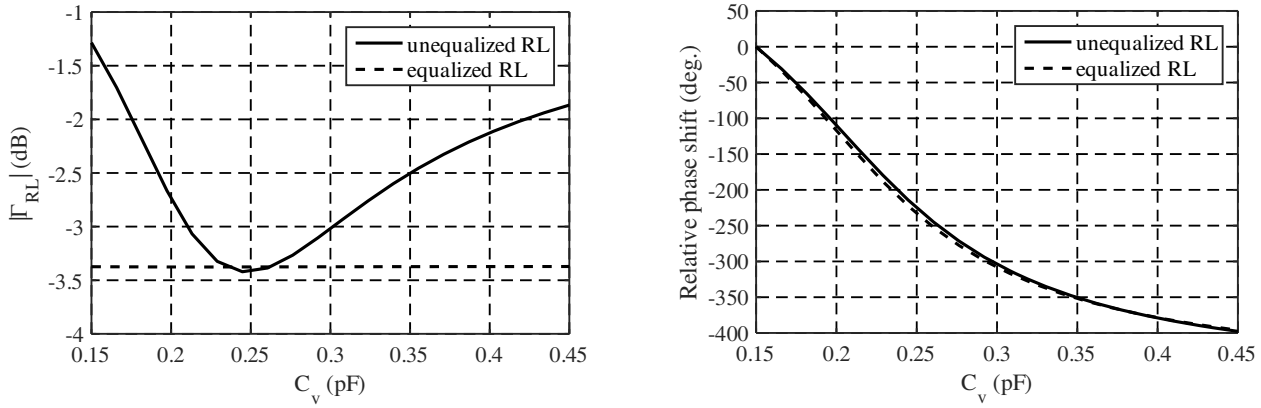
In Eq. (2) we assume that $R_v \ll Z_0$. In practice, a value of L_s is chosen slightly higher than computed from Eq. (2) to get a 360° total phase shift for the full PS in a desired bandwidth. When the full varactor equivalent circuit, employing a packaging capacitance C_p, is used (Fig. 3(b)), it is reasonable to substitute $C_{v\min} + C_p$ and $C_{v\max} + C_p$ in Eq. (2) instead of the corresponding values of capacitances.

One of the crucial problems arising in the reflection-type PS development is transmission ripple caused by a $|\Gamma_s|$ variation during varactor tuning. To overcome this issue, previously researchers have used an equalization resistor R_{eq} [9, 11]. This technique is useful only at low frequencies where the simplified varactor equivalent circuit can be used. However, at higher frequencies a packaging capacitance C_p shifts a center of $\Gamma_s(C_v)$ circle to the capacitive region of the Smith chart. For this case, we developed the generalized equalization technique based on the complex plane consideration of $\Gamma_s(C_v)$ and employment of linear fractional transformation (LFT) [21]. The main idea of the equalization approach is depicted in Fig. 4(a), while Fig. 4(b) demonstrates the corresponding circuit implementation.



(a) (b)

Figure 4. The proposed stub equalization technique. (a) Complex plane representation of $\Gamma_s(C_v)$ transformation. (b) Circuit diagram of the tuning stub with the parallel equalization admittance Y_{eq}.



(a) (b)

Figure 5. Simulated performance of the RL with a single control channel at 5.8 GHz as a function of varactor capacitance for both unequalized and equalized designs. (a) $|\Gamma_{RL}|$, (b) relative phase shift.

In short, we can say that the equalization complex admittance $Y_{eq} = G_{eq} - jB_{eq}$ transforms $\Gamma_s(C_v)$ circle to $\Gamma''_s(C_v)$ circle with the center C''_0 coinciding with the complex plane center. The detailed consideration of the proposed technique is given in Appendix A.

Finally, to achieve a full 360° phase shift, two tuning stubs are connected using the quarter-wavelength TL_0 in a manner shown in Fig. 2 [9]. In this case, input port impedance should be chosen as $Z_{port} = Z_0/2$ [9]. Despite the elegance and the simplicity of this technique, RL losses increase substantially due to the relation for the RL input reflection coefficient $\Gamma_{RL}(C_v) = \Gamma''^2_s(C_v)$ [9].

The proposed equalization technique was applied to a test RL development with the central frequency $f_0 = 5.8$ GHz. We used varactor with $C_{v\,\min} = 0.15$ pF, $C_{v\,\max} = 0.45$ pF, $C_p = 0.05$ pF, $R_v = 5$ Ohm. According to the presented design relations, the RL structure is characterized by the following set of parameters: $L_s + L_v = 2.6$ nH, $Z_0 = 35$ Ohm, the parallel equalization inductance $L_{eq} = 12.4$ nH, the parallel equalization resistance $R_{eq} = 362$ Ohm. RL electrical performance was computed in ADS circuit simulator and demonstrated in Fig. 5 at 5.8 GHz for the unequalized and equalized structures. From Fig. 5 we can see that the structures realize the same total phase shift of 400°, and equalized losses equal to the worst losses of the basic RL. It is interesting to note that, if we neglect the equalization inductance L_{eq}, the minimal achievable ripple value is around 0.5 dB. Concluding the consideration of the classical RL, we dwell on the question of RL bandwidth performance. In Fig. 6, the frequency dependencies of equalized $|\Gamma_{RL}|$ are depicted, while C_v varies from 0.15 pF to 0.45 pF with a step of 0.05 pF. The observable frequency behavior is typical for this type of RL — there is only a single frequency point with ideal zero ripple. A ripple value constantly increases with increase of the frequency deviation from f_0. Thus, a RL bandwidth is limited by a ripple level growth.

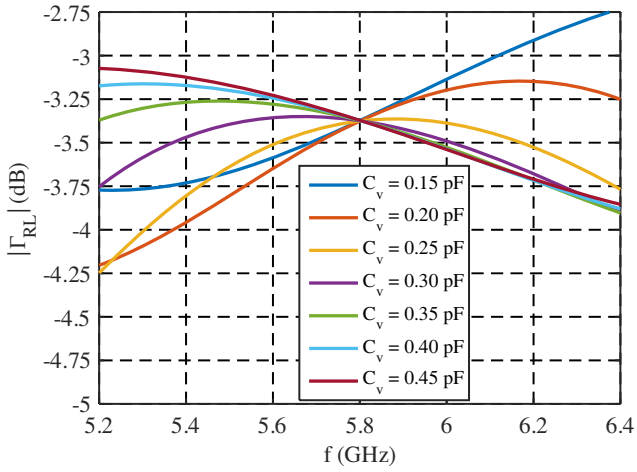


Figure 6. Simulated frequency dependencies of $|\Gamma_{RL}|$ for the equalized RL with a single control channel, where C_v varies from 0.15 pF to 0.45 pF with a step of 0.05 pF.

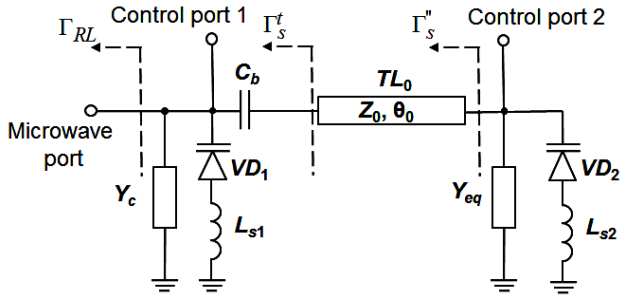


Figure 7. Circuit diagram of the novel RL structure with two independent control channels.

3. A NOVEL REFLECTIVE LOAD DESIGN

As we have discussed in Section 2, one of the main drawbacks of the classical RL design is high reflection losses caused by multiplication of two equalized $\Gamma''_s(C_v)$. For some applications, where the PS is used in microwave system front ends [5, 22], such losses degrade system energy potential and sensitivity, and hence should be minimized. To resolve this problem, we propose a novel RL structure depicted in Fig. 7. The RL again comprises two similar tuning stubs with varactors $VD_{1,2}$ and series short-circuited inductances $L_{s1,2}$. The crucial difference of the novel design is varactors independent control, realized using two control channels decoupled by a blocking capacitance C_b. Besides that, only the tuning stub # 2 is equalized in the manner described in Section 2, whereas a fully reactive compensating admittance Y_c is connected in parallel to the tuning stub # 1. Tuning stubs are connected through TL_0 with characteristic impedance Z_0 and electrical length θ_0, which is not necessary 90°. Below, we discuss in details circuit performance and a control algorithm.

At the first stage of operation capacitance C_{v2} is varied from $C_{v\max}$ to $C_{v\min}$ value, while capacitance C_{v1} is kept maximal. Tuning stubs parameters are chosen from the same relations that we considered in Section 2. Thus, the tuning stub # 2 is equalized and has the input reflection coefficient $\Gamma''_s(C_v)$ with a constant magnitude (for reference impedance Z_0). Next, $\Gamma''_s(C_v)$ is transformed through TL_0 to the stub # 1 input, preserving its circular form on the complex plane. We will denote it as $\Gamma^t_s(C_v)$. The tuning stub # 1 is connected in parallel with the compensating stub, with parameters chosen to maintain a parallel resonance with the stub # 1:

$$\mathrm{Im}\left(Y_c + Y_s\left(C_{v\max}\right)\right) = 0, \quad \mathrm{Re}\left(Y_c + Y_s\left(C_{v\max}\right)\right) = G_p, \tag{4}$$

where G_p — parallel resonance conductance. Parallel connection of G_p to TL_0 input leads to LFT

(A1) of function Γ_s^t. As a result, the center of the input reflection coefficient curve (for the reference impedance Z_0) is shifted along the real axis on the complex plane. Appropriately choosing the input port impedance Z_{port}, we return the center of the RL input reflection coefficient $\Gamma_{RL}(C_{v1} = C_{v\max}$, $C_{v2})$ back to the complex plane center. Eventually, RL losses are fully equalized. The required Z_{port} value can be found from the LFT symmetry principle [21]:

$$Z_{port} = Z_0 \sqrt{\frac{1 - \left|\Gamma_s^t \left(C_{v2} = C_{v\max}\right)\right|^2}{\left(1 + \bar{G}_P\right)^2 - \left|\Gamma_s^t \left(C_{v2} = C_{v\max}\right)\right|^2 \left(1 - \bar{G}_P\right)^2}}. \tag{5}$$

After this, a final $|\Gamma_{RL}|$ can be evaluated:

$$|\Gamma_{RL}(C_{v1} = C_{v\max}, C_{v2})| = 4\left|\Gamma_s^t \left(C_{v2}\right)\right| \frac{Z_{port}}{Z_0} \frac{1}{\left(1 + \left(\bar{G}_P + 1\right) \frac{Z_{port}}{Z_0}\right)^2 - \left(1 + \left(\bar{G}_P - 1\right) \frac{Z_{port}}{Z_0}\right)^2 \left|\Gamma_s^t \left(C_{v2}\right)\right|^2}. \tag{6}$$

Analysis of Eq. (6) shows that for typical varactor parameters $\left|\Gamma''^2_s\right| < |\Gamma_{RL}| < |\Gamma''_s|$. This inequality determines the benefit of using the novel RL design compared to the classical one.

At the second stage, C_{v1} is varied from $C_{v\max}$ to $C_{v\min}$ value, while capacitance C_{v2} remains minimal. We should keep in mind that the tuning stub # 2 is already equalized. Now, the only condition to be enforced for $\Gamma_{RL}(C_{v1}, C_{v2} = C_{v\min})$ equalization is

$$\Gamma_s^t \left(C_{v\min}\right) = \Gamma''_s \left(C_{v\max}\right). \tag{7}$$

Expression (14) means that TL_0 should translate $\Gamma''_s \left(C_{v\min}\right)$ to the $\Gamma''_s \left(C_{v\max}\right)$ position. This condition is employed to find the required TL_0 electrical length θ_0. In this case, the total input admittance Y_{RL} can be written as

$$Y_{RL} \left(C_{v1}, C_{v2} = C_{v\min}\right) = Y_s \left(C_{v1}\right) + Y_{eq} \; + Y_s \left(C_{v\max}\right) + Y_c. \tag{8}$$

Analyzing Eq. (8), we can see from the resonance condition in Eq. (4) and the aforementioned considerations that the RL is automatically equalized during stub # 1 tuning. Eventually, by realization of the suggested algorithm, the RL total phase shift reaches 360°.

4. EXPERIMENTAL PROTOTYPE STUDY AND RESULTS DISCUSSION

To demonstrate the proposed technique applicability, we designed an RL and a PS based on silicon packaged Skyworks SMV2201-040LF varactor diode for operation in C-band ($f_0 = 5.8$ GHz). According to the equivalent circuit from Fig. 3(b) varactor parameters were extracted as $C_{v\min} = 0.145$ pF (20 V), $C_{v\max} = 0.505$ pF (5 V), $C_p = 0.05$ pF, $L_v = 0.9$ nH, $R_v \; = 4.5$ Ohm. The RL was designed in microstrip topology on Rogers RO4003C substrate (0.203 mm thick). The initial design was developed in ADS circuit simulator, whereas the final topology optimization was done in HFSS. The structure of the RL microstrip layout is depicted in Fig. 8. The RL was designed to have 50 Ohm input (pos. {1} in Fig. 8). Two similar tuning stubs {2}, {3} comprise varactors and series inductances, which are realized using short-circuited microstrip stubs with characteristic impedance of 48 Ohm and electrical length of 45°. A U-shaped microstrip line {4} forms TL_0 with $Z_0 = 36$ Ohm and $\theta_0 = 98°$. To achieve the required equalization admittance $Y_{eq} = 2.7 - j5.8$ mS, similarly to [19], we used 13 Ohm resistor {5} connected to the stub # 2 input through a microstrip line {6} with characteristic impedance of 69.5 Ohm and electrical length of 71°. The compensating admittance $Y_c = j18$ mS was realized using an open-circuited microstrip stub {7}. The stub peripheral part is slotted for possibility to perform the experimental tuning of Y_c value by cutting stub's "fingers". A quarter-wavelength transformer {8} with characteristic impedance of 37 Ohm is employed to match 50 Ohm input with the required $Z_{port} = 27.4$ Ohm. Two control ports {9}, {10} are connected to the structure using parallel quarter-wavelength open-circuited stubs {11}, {12}. Control ports are decoupled by a blocking capacitor {13} with $C_b = 5$ pF. The RL comprises an additional shielding belt {14} purposed to improve isolation between two RLs in PS.

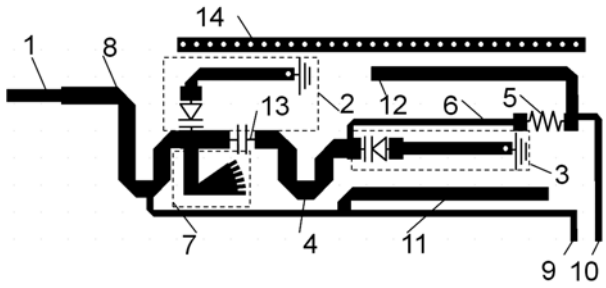


Figure 8. Microstrip layout of the novel RL.

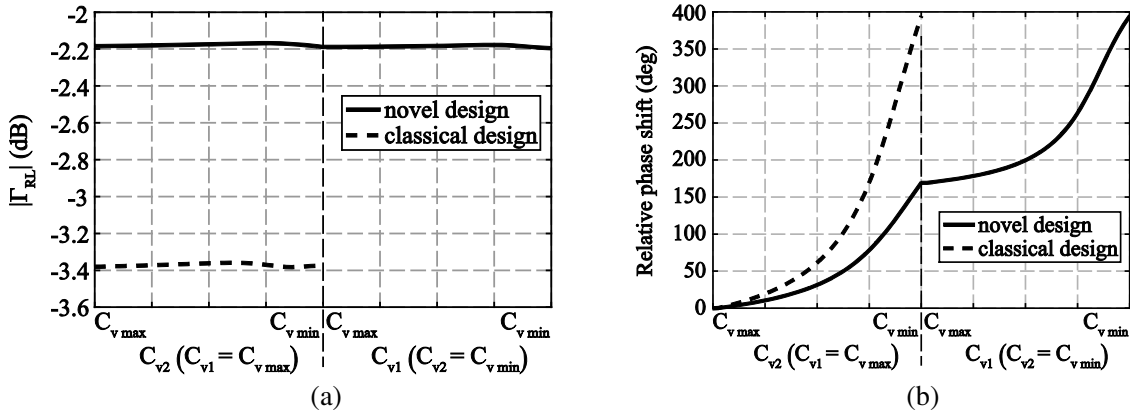


Figure 9. Comparison of simulated performance for the novel RL design and the classical design at 5.8 GHz. (a) $|\Gamma_{RL}|$, (b) relative phase shift.

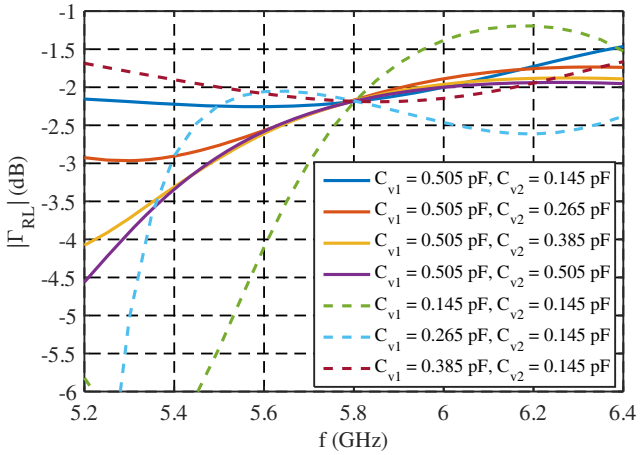
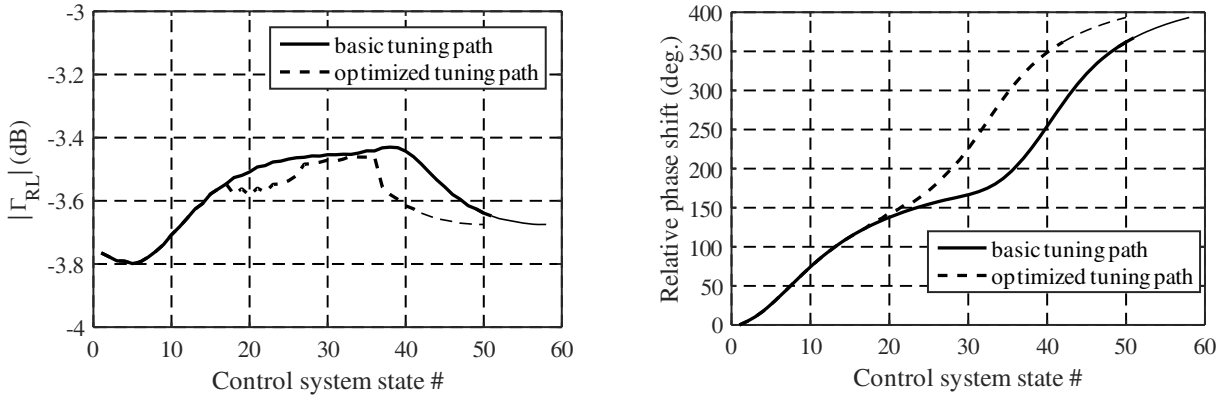


Figure 10. Simulated frequency dependencies of the novel RL $|\Gamma_{RL}|$. Solid curves correspond to C_{v2} variation from 0.505 pF to 0.145 pF with a step of 0.12 pF, while $C_{v1} = 0.505$ pF. Dashed curves correspond to C_{v1} variation from 0.505 pF to 0.145 pF with a step of 0.12 pF, while $C_{v2} = 0.145$ pF.

Figure 9 demonstrates performance of the novel RL simulated in ADS at 5.8 GHz. For the purpose of comparison, the similar simulated characteristics are presented here for the RL with a single control channel, which is based on the same tuning stub and the equalization circuit with $Z_0 = 36$ Ohm. The results evidence that for the total phase shift of 400° the proposed structure provides more than 1 dB losses improvement. Simulated frequency dependencies of the novel RL $|\Gamma_{RL}|$ are depicted in Fig. 10, where the RL is tuned along the aforementioned tuning path. It can be seen that RL bandwidth

(a) (b)

Figure 11. Photographs of the fabricated RL (a) and the full PS (b).



(a) (b)

Figure 12. Measured RL performance at 5.8 GHz as a function of control system state #. The corresponding tuning paths are depicted in Fig. 13. (a) Reflection coefficient magnitude, (b) relative phase shift.

by 0.5 dB ripple level is rather narrow. Below, we will come back to the problem of the bandwidth enhancement.

A photograph of the fabricated RL prototype is depicted in Fig. 11(a). RL measurements were elaborated using 6-bit digital-to-analog converter (DAC) with DAC code "0" corresponding to 0 V, DAC code "48" corresponding to 24 V (0.5 V step). Input microwave power level was set at 0 dBm. Based on measured characteristics, we slightly changed the RL tuning path compared to the theoretical path. As a result of some errors in the varactor equivalent circuit parameters extraction the value of $C_{v\,\max}$ (5 V) turned out to be lower than expected. To compensate this error and maintain the resonance condition (4) we had to lower the channel 1 minimal voltage to 4 V. At the same time, the minimal voltage of the channel 2 is kept unchanged (5 V), because $C_{v\,\max}$ of the tuning stub # 2 does not affect the ripple performance. The maximum voltage of both channels was set at 18.5 V. Another possible reason for these corrections is the dependence of varactor R_v on applied control voltage, which is the most significant at low voltages [23]. Measured at 5.8 GHz Γ_{RL} is depicted in Fig. 12 (solid curves). Results evidence that the desired 400° total phase shift was achieved with 0.35 dB ripple level.

As we have seen above, the classical and the proposed RLs both demonstrate a relatively narrow bandwidth limited by a ripple level growth. In particular, a bandwidth of the considered design, estimated by 0.5 dB ripple level, at 5.8 GHz is around 100 MHz (1.7%). It is very important to find some technique for RL bandwidth enhancement, thus making the design suitable for wider range of applications. Obviously, the narrowband nature of the RL structure comes from the fact that Equations (A1)–(A5), (4), (5) and (8) are fulfilled only at the single frequency f_0. Nevertheless, we can suppose that at other frequencies the tuning path can be modified to compensate changes in circuit elements impedances. For this purpose, we consider 2D maps of $|\Gamma_{RL}|$ as a function of two control

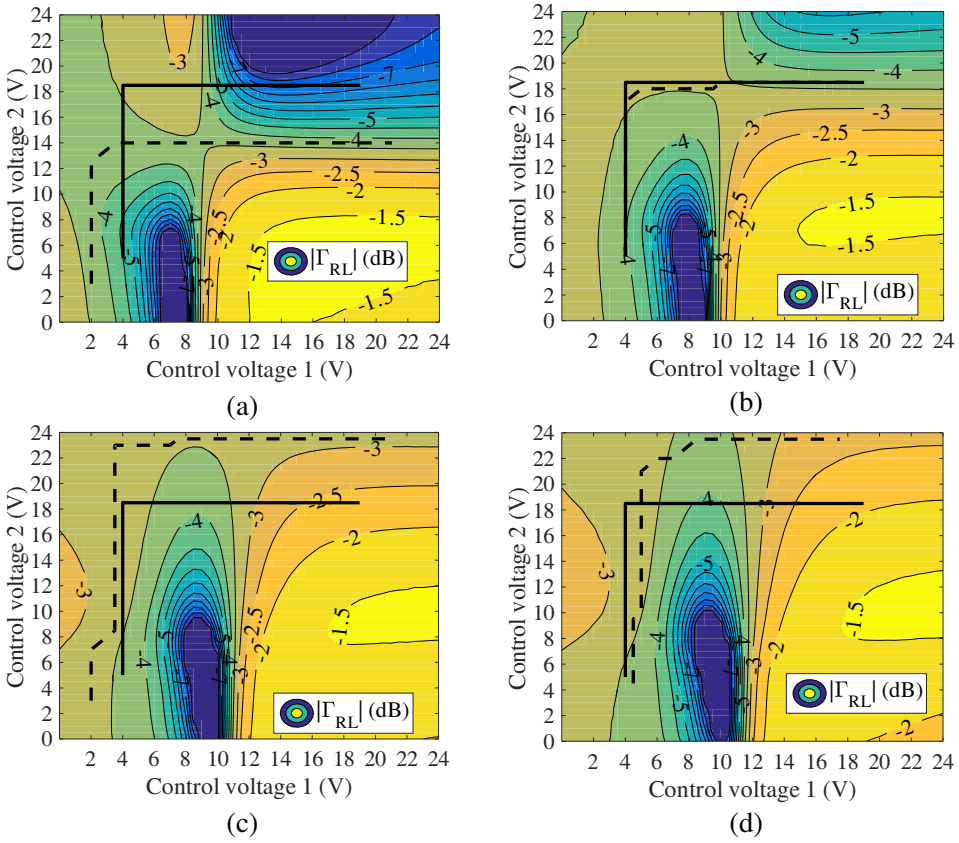


Figure 13. Measured 2D maps of $|\Gamma_{RL}|$. The basic tuning path is depicted by solid line, whereas optimized paths are shown by dashed lines. (a) 5.6 GHz, (b) 5.8 GHz, (c) 6.0 GHz, (d) 6.1 GHz.

voltages. Measured maps at different frequencies are presented in Fig. 13, where the solid line shows the basic tuning path. From Figs. 13(a), (c) it is clear that the basic path leads to high ripple levels, but it is possible to find an optimal tuning path for each frequency. This idea was realized by setting the start and end points on each map and applying Dijkstra's graph optimization algorithm [24] in order to get a final tuning path with a minimal ripple level. The directional graph was built by coupling each point on the 2D map with three adjacent points in the first quadrant, where each graph edge has a weight that equals to an absolute value of the difference (in dB) of adjacent points $|\Gamma_{RL}|$. The optimized paths are depicted in Fig. 13 by dashed lines. Measured $|\Gamma_{RL}|$ along the optimized tuning path at 5.8 GHz is also shown in Fig. 12. As it was expected, the basic path at 5.8 GHz is very close to the optimized path in terms of ripple level. Of course, the employed optimization algorithm is not the only one suitable for the considered task. However, from our experience it usually generates paths with ripple levels below 0.5 dB, as can be seen from the presented results.

In Fig. 14 we demonstrate measured RL performance at different central frequencies from 5.6 GHz to 6.0 GHz with 100 MHz instantaneous bandwidth. In this figure, at each central frequency the optimal path is synthesized according to the aforementioned algorithm, and only at 5.8 GHz we used the basic tuning path. Note that in Figs. 12, 14 curves are plotted bold for the path parts where the relative phase shift varies from 0° to 360°. From the presented results we can see that inside (5.6–6.0) GHz band the RL demonstrates the maximum ripple of 0.8 dB for 1.7% instantaneous bandwidth. Next, we tried to determine the maximal achievable frequency range for operation with the aforementioned ripple level and the instantaneous bandwidth. We have found that the central operating frequency can be successfully extended up to 6.1 GHz. The possibility of bandwidth expansion to the higher frequency region is caused by the smooth behavior of $|\Gamma_{RL}|$ at frequencies above f_0 (see Fig. 10). The measured 2D map of $|\Gamma_{RL}|$ at 6.1 GHz is depicted in Fig. 13(d), and the corresponding performance along the

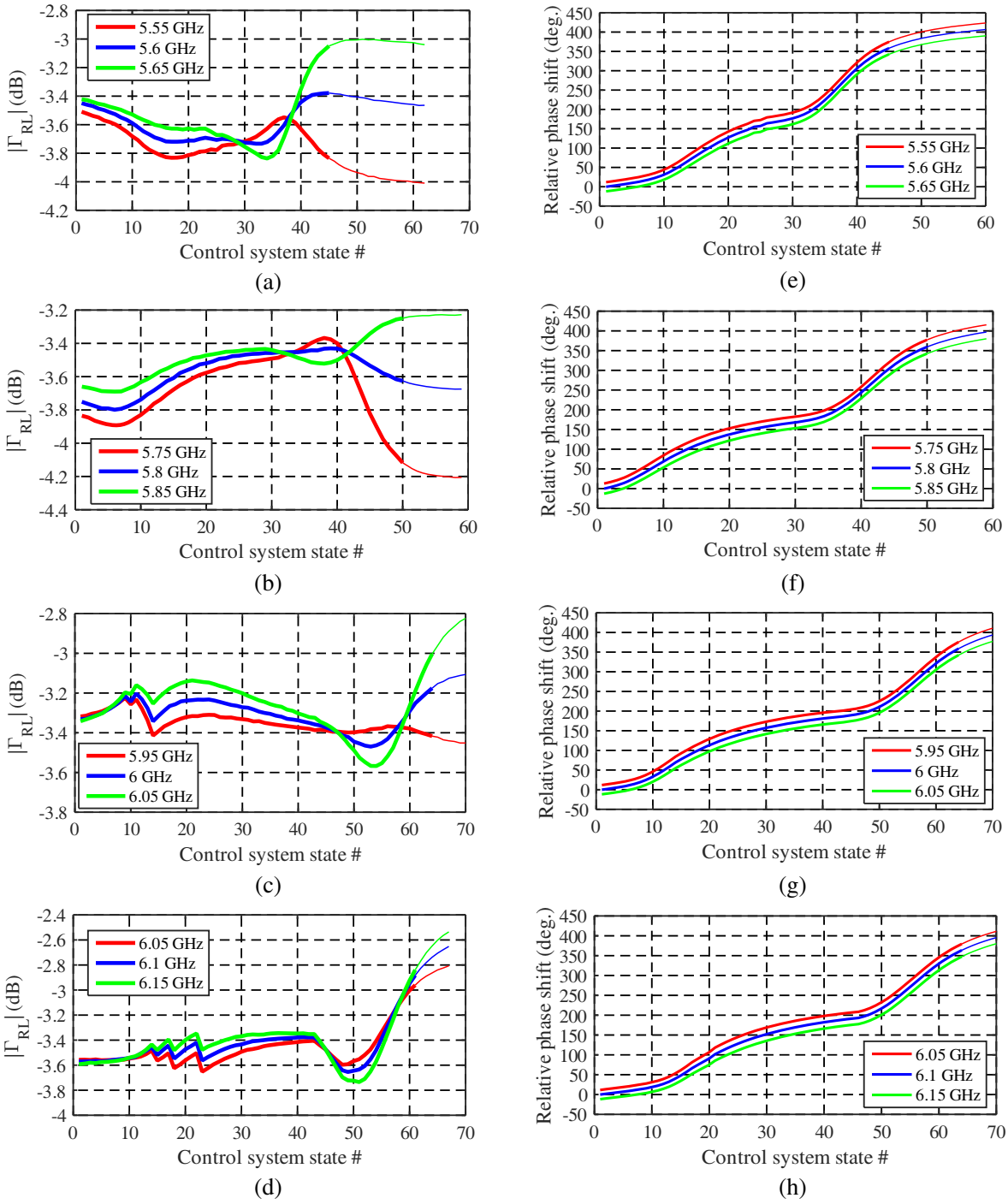


Figure 14. Measured RL performance at different central frequencies from 5.6 GHz to 6.1 GHz with 100 MHz instantaneous bandwidth. $|\Gamma_{RL}|$ — left, relative phase shift — right.

optimized path is given in Figs. 14(d), (h). Total RL operating frequency range now extends between 5.55 GHz and 6.15 GHz, and we can reassign the RL central frequency as $f_0 = 5.85$ GHz. Thus, the proposed RL can operate in 10.3% total bandwidth with the very low ripple, if at each sub-band the appropriate optimized tuning path is employed.

Finally, we will consider performance of the full PS. The fabricated PS prototype is presented in Fig. 11(b). Compact Anaren C5060J5003AHF HC was used in this design. The full PS footprint area is

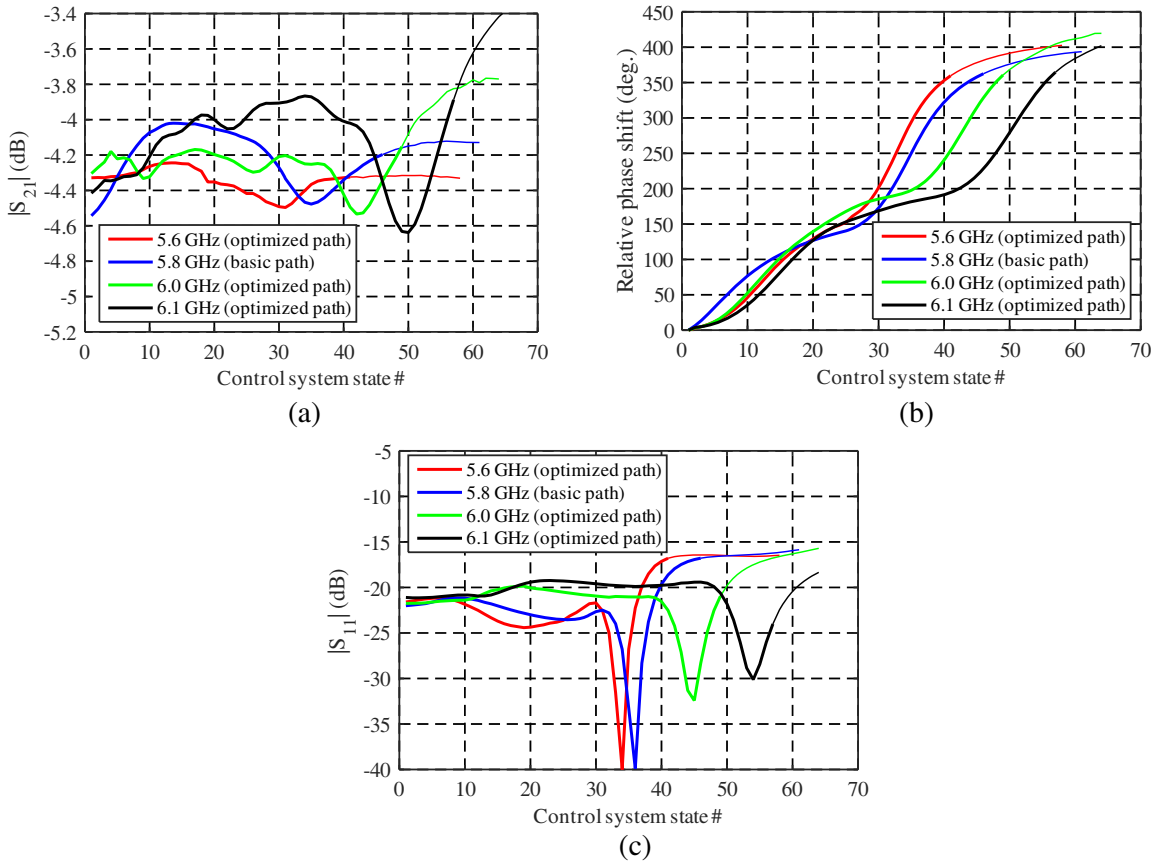


Figure 15. Measured PS performance at different frequencies as a function of control system state #. (a) transmission coefficient magnitude, (b) relative phase shift, (c) input matching.

$22\times11\,\text{mm}^2$, or $0.43\times0.21\lambda_0^2$, where λ_0 is a free space wavelength at the central frequency $f_0 = 5.85\,\text{GHz}$. Thus, the considered design is suitable for integration into a low-profile antenna array unit cell. Due to imperfect electrical characteristics of the HC and some parasitic electromagnetic coupling between the RLs, the basic tuning path of the PS at 5.8 GHz was slightly changed compared to the RL tuning path. As a result, channel 1 voltage is varied from 4.5 V to 21.5 V, whereas channel 2 voltage is varied from 5.5 V to 18 V. A similar slight modification was done for the graph optimized paths at all central frequencies. Measured results for 5.6 GHz, 5.8 GHz 6.0 GHz, and 6.1 GHz are presented in Fig. 15, where the basic path is used for 5.8 GHz. Frequency characteristics of the PS and the RL are identical, and the maximum $|S_{21}|$ ripple level is below 0.8 dB. The input reflection coefficient magnitude of the full PS is depicted in Fig. 15(c), where we can see that $|S_{11}|$ does not exceed $-16\,\text{dB}$. In Fig. 16 we demonstrate PS performance in the frequency domain. In this case the PS operates at the sub-band with 5.8 GHz central frequency. PS performance at other sub-bands is similar and was not depicted here. It is important to note that measured PS $|S_{21}|$ (Fig. 16(a)) and simulated $|\Gamma_{RL}|$ (Fig. 10) demonstrate identical frequency domain behavior. From Fig. 16(d) we can conclude that phase-frequency responses are linear inside the operating sub-band. This fact is very important when PS is used in beam steering antenna arrays [4]. We also examined PS linearity by measuring output-referred P_{1dB} and $IIP3$. For all phase states inside the operation bandwidth the worst values were determined as $P_{1\text{dB}} = 13.6\,\text{dBm}$, $IIP3 = 21.5\,\text{dBm}$.

Summarizing the results, in Table 1 we compare the main characteristics of the prior art designs and the proposed PS. Prior art designs employ modified couplers, double-layer PCB or even 3D assemblies. On the other hand, the proposed PS has the simple single-layer footprint and employs the standard quadrature hybrid coupler. This feature severely simplifies the PS design procedure, allowing either

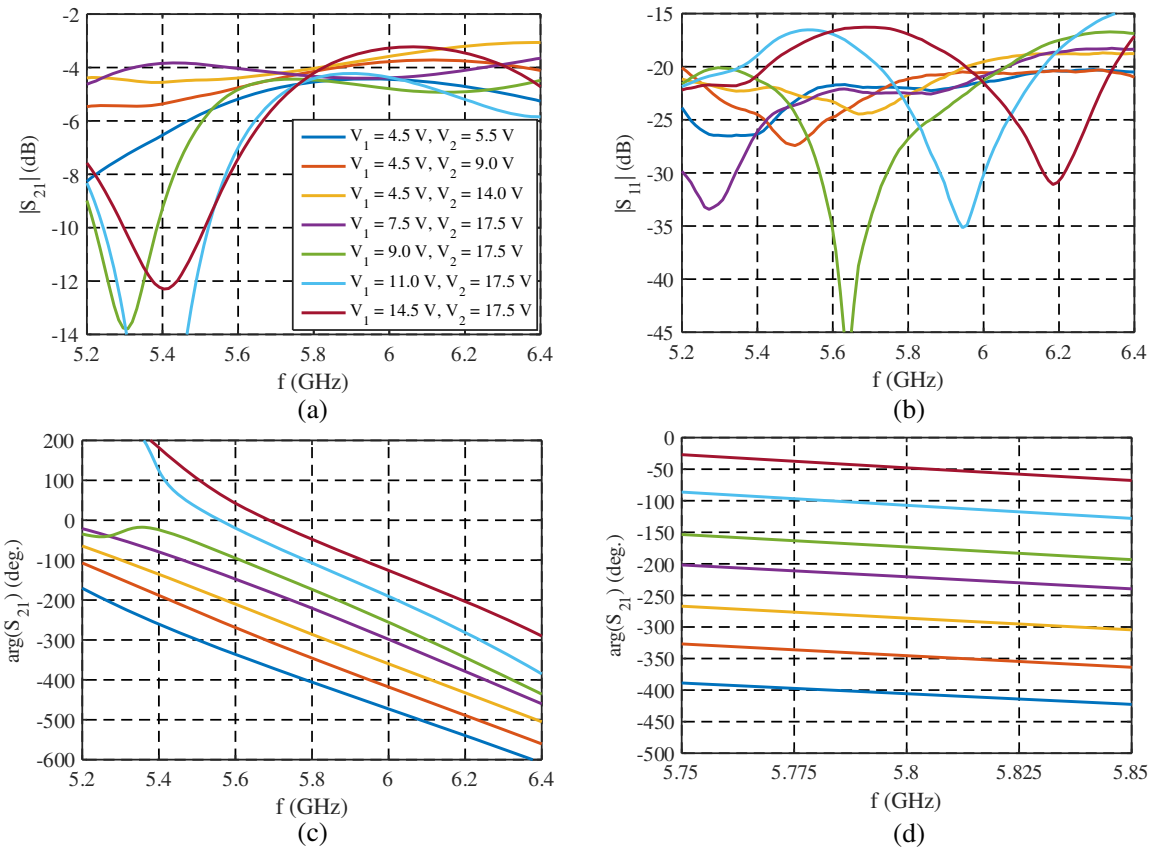


Figure 16. Measured PS performance at different phase states as a function of frequency for operation at 5.8 GHz along the basic tuning path. (a) Transmission coefficient magnitude, (b) input matching, (c) transmission coefficient phase, (d) transmission coefficient phase (inside the operating sub-band).

using standard HC footprints or employing of-the-shelf surface-mount 50 Ohm couplers. To characterize the varactor diode, in Table 1 we presented quality factor (QF) computed for the minimal capacitance as $QF = 1/(2\pi f_0 C_{v\,\min} R_v)$. It is important to emphasize that the goal of this work was not to develop a particular PS with the best performance in terms of losses, but rather to propose a novel low-losses equalization technique applicable for a wide frequency band. Due to this, we employed the low-cost silicon varactor diode at C-band, whereas designs from the table were developed for operation in more than 2 times lower frequency range. Nevertheless, achieved PS losses are comparable with losses of the equalized PSs from [11, 12]. At the same time, the ripple level across the bandwidth is significantly lower for the proposed design. The design from [18] demonstrates great insertion losses performance and relatively low ripple level. However, it should be noticed that the RL in [18] is based on three high-quality varactor diodes with $QF = 177$. In Table 1, the most confusing comparison parameter is bandwidth. In [13, 14] authors claimed very wide bandwidths by PS $|S_{11}| < -10$ dB, whereas a ripple level is not controlled and exceeds 3 dB. Due to this, in Table 1 we introduced bandwidth determined by two different criterions. The first criterion is a given matching level. And the second one (the most important for our study) is a given ripple level. In Table 1, it can be seen that the proposed design has more than two times wider bandwidth by 0.8 dB ripple level compared with the bandwidth of the equalized design from [12]. At the same time, ripple levels in [13, 14], and [18] are always higher than 0.8 dB, and consequently ripple bandwidths of these designs are 0% (N/A).

If we examine approaches for further RL and PS performance enhancement, it should be said that, according to simulation results, using of higher QF varactors leads not only to average losses improvement, but also to a ripple level decrease inside a fixed instantaneous bandwidth.

Table 1. Performance comparison of different reflection-type PSs.

	[12]	[13]	[14]	[18]	This work
Design type	Single-layer PCB, $\varepsilon_r = 3.25$	Double-layer PCB, $\varepsilon_r = 10.2$	3D PCB assembly, $\varepsilon_r = 3.55, 2.2$	Single-layer PCB, $\varepsilon_r = 3.55$	**Single-layer PCB, $\varepsilon_r = 3.55$**
Transverse footprint	$0.42\times0.2\ \lambda_0^2$	$0.15\times0.13\ \lambda_0^2$	$0.26\times0.16\ \lambda_0^2$	$0.39\times0.27\ \lambda_0^2$	**$0.43\times0.21\ \lambda_0^2$**
Coupler type	Impedance transforming quadrature HC	Non-equal, non-quarter-wave coupler	Non-equal quadrature coupler	Impedance transforming quadrature HC	**Quadrature HC**
Equalization	Equalized	Unequalized	Unequalized	Unequalized	**Equalized**
Varactor type, QF, R_v (Ohm)	Silicon, 28, 2	GaAs, N/A	Silicon, 79, 1.8	Silicon, 177, 1	**Silicon, 42, 4.5**
Central frequency (GHz)	2	2.2	1.5	2	**5.85**
Bandwidth (Matching)	10% ($\lvert S_{11}\rvert$ < -14 dB)	36% ($\lvert S_{11}\rvert$ < -10 dB)	67% ($\lvert S_{11}\rvert$ < -10 dB)	10.9% ($\lvert S_{11}\rvert$ < -11 dB)	**10.3% ($\lvert S_{11}\rvert$ < -16 dB)**
Bandwidth (ripple<0.8 dB)	4%	N/A	N/A	N/A	**10.3%**
Maximum/ minimum ripple inside matching bandwidth (dB)	1.6/0.6	3/2	5.4/2.5	1.3/1.1	**0.8/0.3**
Total phase shift inside matching bandwidth (deg.)	407	335–375	280–407	380	**360**
Average losses (dB)	4.4	3	3	1.2	**4.3**

5. CONCLUSIONS

The problem of reflection-type PS transmission losses equalization was thoroughly considered in this study. First, we discussed the general equalization technique and derived main relations that can be applied to tuning stubs with arbitrary varactor diodes. Next, the novel RL structure with two independent control channels and the corresponding control algorithm were proposed. We showed that average RL losses are significantly lower compared to losses of the classical RL design with a single control channel. Moreover, simulations predict that for higher frequencies the losses improvement will be more notable. This low losses advantage allows to use packaged silicon varactor diodes for many applications where previously, due to high efficiency requirements, developers had to use GaAs components. We have also discussed the method for the proposed RL bandwidth enhancement, which

assumes using a unique varactors control algorithm inside each frequency sub-band. This approach was successfully verified by development of the RL and the PS prototypes that realized 10.3% total operating bandwidth, with ripple level being less than 0.8 dB inside 1.7% instantaneous bandwidth. Authors adhere to the conviction that the idea of two independent control channels can find its application for other varactor-based RL structures and, probably, may lead to even further losses improvement.

APPENDIX A. MAIN RELATIONS FOR THE GENERALIZED TUNING STUB EQUALIZATION TECHNIQUE

Here we will derive the general equalization circuit structure for the full varactor equivalent circuit by considering the single tuning stub performance on the complex plane. From the basic Smith chart properties we know that $\Gamma_s(C_v)$ curve of the simplified equivalent circuit has a circular form with a center lying on the positive part of the real axis [9]. Next, when we introduce a packaging capacitance C_p, $\Gamma_s(C_v)$ preserves a circular form but its center moves to the capacitive region. This property follows from the fact that adding a parallel (or series) admittance to any reflecting structure leads to its reflection coefficient LFT:

$$\Gamma'_s(C_v) = \frac{A\Gamma_s(C_v) + B}{C\Gamma_s(C_v) + D}, \tag{A1}$$

where A, B, C, D — some constants depending only on the parallel (series) admittance. From the general LFT properties, we can say that any circle on the complex plane preserves its shape after LFT, with only a position and a radius being changed [21]. Therefore, $\Gamma_s(C_v)$ of the full equivalent circuit is a part of a circle with a center $C_0 = a_0 + jb_0$ and a radius R — curve 1 in Fig. 4(a).

The idea of the equalization technique is to align a center of a final reflection coefficient circle with the complex plane center. To do this, we introduce an additional parallel complex admittance $Y_{eq} = G_{eq} - jB_{eq}$, as it is shown in Fig. 4(b). Thus, the equalization technique can be considered comprised of two steps:

1) Adding a parallel inductive susceptance $-B_{eq}$ to locate $\Gamma'_s(C_v)$ center on the real axis with a center at $C'_0 = a'_0$. For this case, $A = 2Y_0 + jB_{eq}$, $B = jB_{eq}$, $C = -jB_{eq}$, $D = 2Y_0 - jB_{eq}$. Substituting these coefficients into (A1) and using the symmetry principle of LFT [21], we can find the required susceptance by imposing the zero imaginary part of C'_0 condition:

$$\frac{1}{\bar{B}_{eq}} = -\frac{(a_0+1)^2 + b_0^2 - R^2}{2b_0}, \tag{A2}$$

where upper dash symbol means susceptance normalization to Y_0. In Fig. 4(a), $\Gamma'_s(C_v)$ is depicted as curve 2, with the center position a'_0 and the radius R':

$$a'_0 = -1 + \frac{(a_0+1)\left((a_0+1)^2 - R^2 + b_0^2\right)}{(a_0+1)^2 - R^2}. \tag{A3}$$

$$R' = R\left(1 + \frac{b_0^2}{(a_0+1)^2 - R^2}\right). \tag{A4}$$

Considering the fact that $a_0 > 0$, from (A3) we can see that always $a'_0 > 0$.

2) Adding a parallel conductance G_{eq} to get a circle $\Gamma''_s(C_v)$ with the center $C''_0 = 0$ and the radius R''. For this case, $A = 2Y_0 - G_{eq}$, $B = -G_{eq}$, $C = G_{eq}$, $D = 2Y_0 + G_{eq}$. Again, by using the symmetry principle of LFT and the expressions for LFT coefficients, we can find the required conductance:

$$\frac{1}{\bar{G}_{eq}} = \frac{1}{2}\sqrt{\frac{\left(a'^2_0 - R'^2 - 1\right)^2}{4a'^2_0} + \frac{(a'_0+1)^2 - R'^2}{a'_0}} - \frac{a'^2_0 - R'^2 - 1}{4a'_0}. \tag{A5}$$

The expression for the radius R'' of the equalized $\Gamma''_s(C_v)$ has the following form:

$$R'' = \sqrt{\frac{\left((1+a'_0)^2 - R'^2\right)^2}{4R'^2} + 1} - \frac{(1+a'_0)^2 - R'^2}{2R'}. \tag{A6}$$

From Eq. (A5) we can conclude that $G_{eq} > 0$, which means that it can be realized using passive components only. The final $\Gamma_s''(C_v)$ is depicted in Fig. 4 as curve 3. It is interesting to point out that for the simplified equivalent circuit Eq. (A5) gives the value of G_{eq} similar to one obtained in [11]. Moreover, if we assume $Z_0 \gg R_v$, Eq. (A5) is reduced to the well-known expression from [9]:

$$1/G_{eq} \approx Z_0^2/R_v. \tag{A7}$$

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