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Performance Enhancement of 60 GHz CMOS Band Pass Filter Employing Oxide Height Virtual Increase

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Abstract—A high selectivity compact size coupled open-loop resonator (OLR-) band pass filter (BPF) in 0.18 µm TSMC Complementary Metal Oxide Semiconductor (CMOS) with low insertion (IL) is presented in this manuscript. First, shape optimization and folding are used to guarantee compact size. Then, high performance of the proposed BPF is obtained by virtually increasing the height of the oxide between the OLR's traces and their ground plane. This virtual increase in the oxide height is realized by etching large slot areas below each of the OLRs. Consequently, the traces are characterized by wider width which in return exhibit lower attenuation constant and hence lower IL. The simulated and measured responses have a very good agreement. The fabricated BPF shows an IL of 3.5 dB at 59 GHz with a return loss of 15 dB and a fractional bandwidth of 16.5%. The fabricated chip has an area of $378 \times 430\,\mu m^2$ including the measurements pads.

1. INTRODUCTION

The millimeter wave frequency band at 60 GHz offers a wide bandwidth between 7 GHz and 9 GHz depending on the country. This wide bandwidth allows it to be a satisfactory candidate for enabling high data rate applications like high definition multimedia interface. Moreover, at 60 GHz, the free space wavelength is only 5 mm, opening the door for on-chip passive components and device integration. Besides, due to cost efficiency of the complementary metal oxide semiconductor (CMOS) technology, it is the time for realizing affordable and fully integrated wireless communication systems on chip (SoC) at the millimeter wave 60 GHz frequency band [1, 2]. Bandpass filters (BPF) are critical components for enhancing the performance of the RF front-end circuits. The function of a BPF is to allow the propagation of an in-band signal (signal of interest) and to reject or attenuate the other signal (undesired signals or noise). BPFs can be grouped into active and passive ones. Passive BPFs, by their nature, have high linearity, low noise figure and zero DC power consumption [3].

The interest of this paper is the passive BPF design. Improving the performance of millimeter wave on-chip passive BPFs has been intensively studied by several researchers [4–10] to improve their characteristics including insertion loss (IL), fractional bandwidth (FBW), and compact size. Patterned Ground Shields and resonator folding have been used in [4] to guarantee low IL of 2.77 dB. Even though the chip area was large, an FBW of 24% was still large for 60 GHz applications [4]. In [5], Franc et al. utilized high optimized coplanar-waveguide (CPW) lines to realize a high selectivity BPF (FBW = 17%). However, this BPF suffered from a poor IL of 4.1 dB and a large occupied chip area [5]. Besides, a compact size multimode BPF was designed with two transmission zeros to guarantee a quasi-elliptic response [6]. However, poor IL and FBW of 4 dB and 38%, respectively, were obtained [6]. Moreover, coupled grounded quarter-wave length resonators were applied to realize a miniaturized 77 GHz BPF [7]. Nevertheless, employing a stepped impedance configuration [7], the optimized IL and

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FBW were 2.9 dB and 27%, respectively. Additionally, the present authors have implemented three high performance on-chip passive BPFs [8–10]. In [8], we employed the multilayer nature of the CMOS process to create a compact size BPF by overlapping the open loop resonators (OLR). This overlapped configuration together with defected ground structure (DGS) guaranteed 2.85 dB of IL and 26% of FBW [8]. Moreover, an H-shaped resonator is used in [9, 10] to ensure high unloaded quality factor (Q_u) due to the reduced losses by coupling through two branches instead of one branch in conventionally coupled line filters [9, 10]. By this, the BPF exhibited an IL and FBW of 2.5 dB and 21% with the addition of open circuit stubs for transmission zeros realization at the out of band [9]. Also, the same BPF showed an IL and FBW of 2.1 dB and 34% without open circuit stubs [10]. The overlapped OLRs and patterned ground shield employed in [11] exhibited good selectivity response but had a large size and considerably high insertion loss [11]. The ground pedestal stepped impedance stubs technique used to enhanced the selectivity and reached an ultra-compact size, for BPF in [12]. The selectivity was improved for this BPF. Still, it suffered from large size and relatively high IL. The ring resonator BPF in [13] had a perfect selectivity, but it suffered from increased size and high IL. Finally, the three-line coupled structure used in [13] exhibited low IL and compact size. Nevertheless, it suffered from low selectivity [13].

In this paper, we propose a novel technique to improve a 60 GHz on-chip OLR-BPF by virtually increasing the oxide height. In Section 2, we discuss the internal and external coupling structure of the conventional square OLR-BPF. The configuration of the proposed on-chip tapped-line square shape OLR-BPF and area optimization are introduced in Section 3. Additionally, we elaborate the benefits of physically increasing the oxide height in the same section. After that, in Section 4, we introduce two large slots below the OLRs to virtually increase the height of the oxide; hence, a similar improvement in the IL close to the one with physical oxide height increase can be realized. Moreover, Section 5 presents the fabricated structure using the 0.18 µm TSMC CMOS process and the measurements of this fabricated structure. Finally, the manuscript concludes the main results in Section 6.

2. COUPLING STRUCTURE BETWEEN SQUARE OLRS

Microstrip square OLR is one of the most used structures for filter applications due to its compact size of approximately ($\lambda g/4$) by ($\lambda g/4$) [14–17], where λg is the guided wavelength at the mid-band frequency. Microstrip OLR filters are much simpler in structure; they require no grounding and coupling apertures compared with dual-plane multi-coupled line filters.

At resonance, each of the OLR has the maximum electric field density at the edges and maximum magnetic field density at the center. In the case of electric coupling, the pair of resonators shown in Fig. 1(a) interact mainly through their electric fields. The configuration of Fig. 1(b) produces, in turn, magnetic coupling. Otherwise, a mixed coupling is realized because neither electric fields nor magnetic fields dominate the interaction between the resonators as depicted in Fig. 1(c) [18, 19].

2.1. Electric Coupling Coefficient E_k

Electric coupling can be obtained if the open sides of two coupled resonators are proximately placed as in Fig. 1(a). When two resonators are coupled to each other, they resonate together at two frequencies f_e and f_m, that are, in general, different from their original resonant frequency f_o, and their difference increases as the coupling between the resonators increases. The resonance frequencies f_e and f_m are given by [16]:

$$f_e = \frac{1}{2\pi\sqrt{L\,(C + C_m)}} \tag{1}$$

$$f_m = \frac{1}{2\pi\sqrt{L\,(C - C_m)}} \tag{2}$$

where f_m and f_e are the magnetic and electric resonance frequencies, respectively. L and C are inductance and capacitance per unit length of each of the OLRs, while C_m is the mutual capacitance due to electric coupling.

According to Hong and Lancaster [16, 18], f_e is lower than that of an uncoupled single resonator ($1/2\pi\sqrt{LC}$) where the coupling effect enhances the capability to store charge of the single resonator

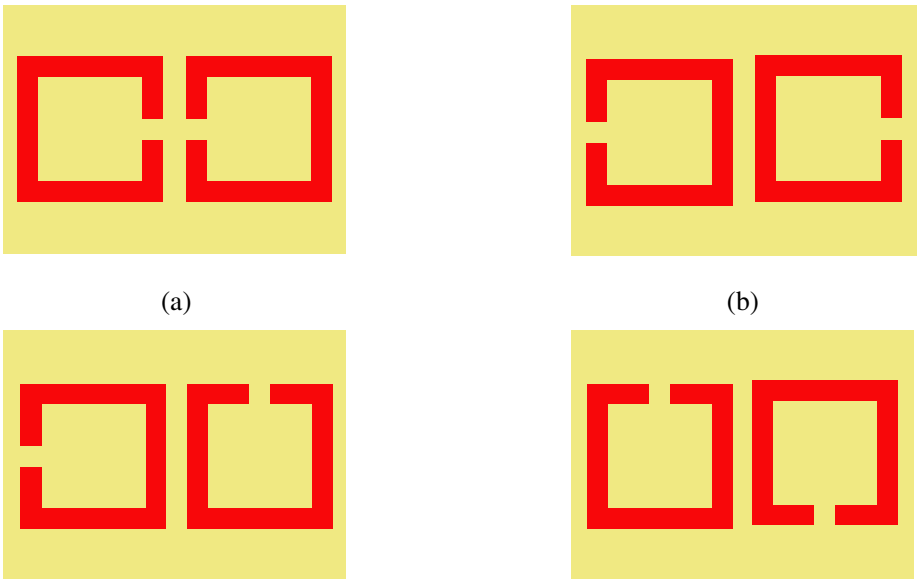


Figure 1. Different possible configurations of the conventional OLR-BPF. (a) Electric coupling. (b) Magnetic coupling. (c) Mixed coupling.

when the electric wall is inserted in the symmetrical plane of the coupled structure. Similarly, replacing the symmetry plane by a magnetic wall results in a single resonant circuit having a resonant frequency f_m, where the coupling effect reduces the capability to store charge so that the resonant frequency is increased. Equations (1) and (2) can be used to find the electric coupling coefficient K_E as follows:

$$K_E = \frac{f_m^2 - f_e^2}{f_m^2 + f_e^2} \tag{3}$$

which is identical to the definition of the ratio of coupled electric energy to stored energy of the single uncoupled resonator [16].

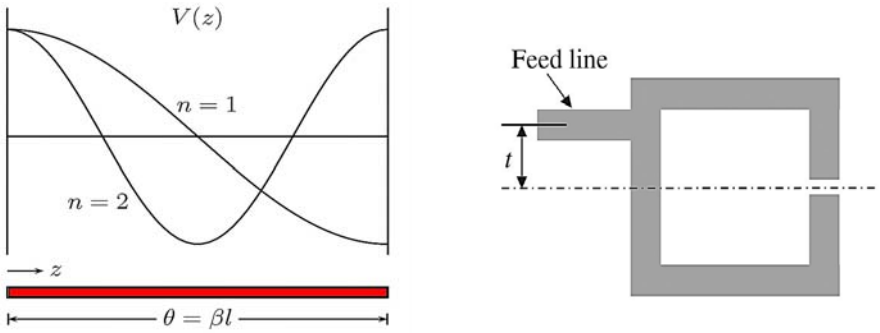
2.2. External Coupling and the External Quality Factor

Figure 2(a) shows the voltage distribution at the first two resonant modes ($n = 1, 2$) of the straight open resonator. For both modes, the maximum voltage is attained at the open ends of the resonator, and zero current is enforced. Hence, only these two modes are allowed. In the first mode, a null exists at $\pi/2$, while in the second mode there are two nulls at $\pi/2$ and $3\pi/2$. The location of these nulls is important since the resonator cannot be excited there.

The coupling or external quality factor (Q_{ex}) is controlled by the location of the tapped line t as illustrated in Fig. 2(b). On the one hand, when the tapped line is located at the center of the resonator, i.e., when $t = 0$, Q_{ex} is very large since the resonator cannot be excited at that position, which results in a weaker coupling and higher insertion loss. On the other hand, increasing t gradually decreases the external quality factor and hence improve the external coupling, which implies more coupling periphery between the feeding line and resonator [20].

3. ON-CHIP TAPPED-LINE SQUARE SHAPE OLR-BPF

Figure 3 shows the geometry and CMOS Die structure for the conventional coupled square shape OLRs-BPF. We have used the 0.18 µm CMOS technology for this BPF implementation. This BPF is composed of two electrically coupled square OLRs implemented on the top thick metal layer (M6). The ground plane is designed on the lowest metal layer (M1). Each of the OLRs has a total length about half of the



(a) (b)

Figure 2. Typical I/O coupling structure for coupled resonator filters. (a) Voltage distribution for a $\lambda/2$ straight open resonator [11]. (b) Tapped-line coupling [18].

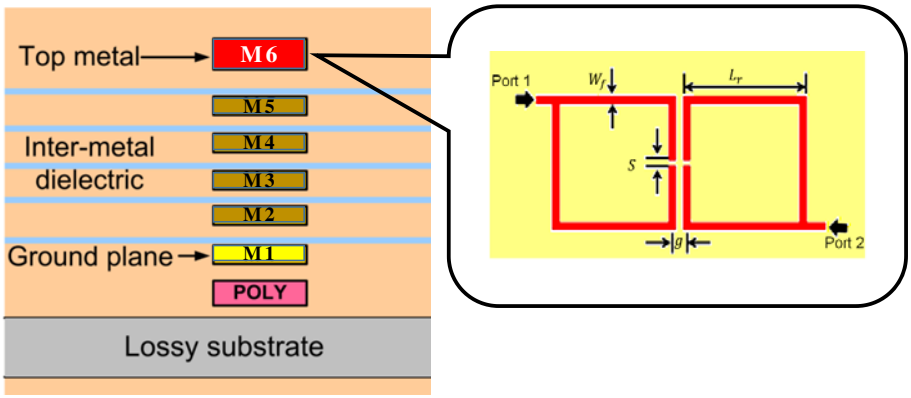


Figure 3. Structure of levels of the metal in the a CMOS process and the layout of the conventional coupled square shape OLRs-BPF.

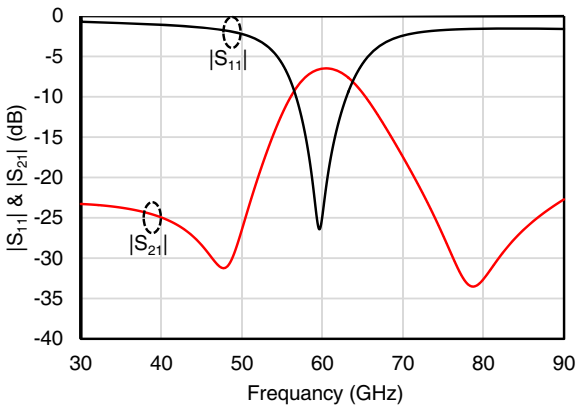


Figure 4. Simulated |*S*-Parameters| of the conventional coupled square OLRs-BPF.

guided wavelength at the center frequency of 60 GHz. The feed line positions are selected to ensure that the resonance modes are excited [18]. The separation gap (g) controls the coupling strength between the OLRs and hence the corresponding bandwidth and IL. Each of the square OLRs has a trace width, $W_f = 6\,\mu$m, and side length, $L_r = 340\,\mu$m and $S = 1.5\,\mu$m. The corresponding area of this BPF is $0.23\,\text{mm}^2$ without feeding lines. The coupling gap (g) is selected to be $6.7\,\mu$m to have a 3-dB FBW of 13.6% which will be fixed for the BPFs hereafter to fairly compare their IL performances. Fig. 4

shows the simulated results of $|S_{11}|$ and $|S_{21}|$ versus frequency of the BPF which illustrates that the IL of the BPF is more than 6 dB with the desired 3-dB bandwidth of 8.2 GHz (FBW = 13.6%). Through this manuscript, we perform electromagnetic (EM) modeling and simulations using the commercially available simulation software ANSYS High-Frequency Structure Simulator (HFSS®).

3.1. Area Reduction Using Folding and Shape Optimization

To reduce the size of the proposed filter, the shape of coupled resonators was replaced by a rectangular shape resonator. Moreover, the open ends were folded inside the resonators to increase the capacitance between them, which in turn contributes to filter miniaturization. This optimized BPF structure is shown in Fig. 5, and its dimensions are $L_1 = 530\,\mu m$, $L_2 = 40\,\mu m$ and coupling gap, $g = 5.3\,\mu m$ with a total area of $0.07\,mm^2$ without feeding lines. This structure leads to 70% area miniaturization compared to the square shape resonators in the previous subsection. Also, this BPF achieves a similar IL and bandwidth as the square, as can be seen from its simulated |S-Parameters| displayed in Fig. 6.

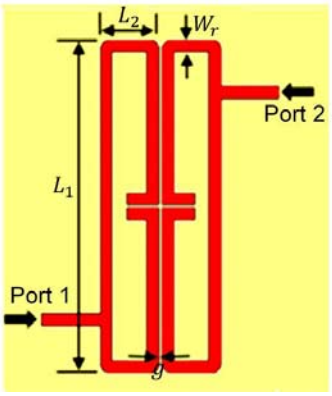


Figure 5. Top view of the optimized OLR-BPF.

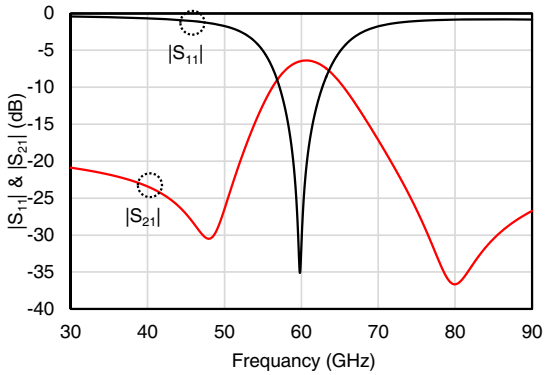


Figure 6. Optimization OLR-BPF simulated |S-Parameters|.

3.2. Parametric Study on Oxide Physical Height

A major limitation of the 60 GHz on-chip BPF's IL performance is the close proximity of its resonators to the ground plane. This low profile about 8 µm leads to high capacitance per unit length. In return, narrower width lines are required to realize the microstrip lines with the target characteristic impedance [21]. Consequently, the attenuation constant increases, and the corresponding losses become higher leading to a degraded IL. In this subsection, we perform a parametric study on the Oxide height (h) in order to clarify this effect. We maintained FBW to 13.6% for a fair comparison between different cases as noted in the previous subsections. Fig. 7 shows the $|S_{21}|$ characteristics of the BPF with different values of h. Clearly, better $|S_{21}|$ performance can be achieved when h increases. We summarize the dimensions and performance of each case in Table 1. The trace width, W_r, becomes wider to achieve the same characteristic impedance. The IL is improved from 6.3 dB to 2.6 dB (3.7 dB enhancement with the same FBW) by increasing h from 8 µm to 18 µm.

4. VIRTUAL INCREASE IN OXIDE HEIGHT FOR BETTER INSERTION LOSS PERFORMANCE

In the preceding section, we discussed an OLR-BPF IL improvement by physically increasing the height of the Oxide. However, in a standard CMOS process, this approach cannot be realized due to the nature of the fixed process parameters which are limited by the technology and fabricating foundry. Instead, in this section, we propose a novel method to virtually increase the oxide height. This virtual increase in the oxide height is possible by etching two large slots at the ground plane (M1) below each of the OLRs as shown in Fig. 8.

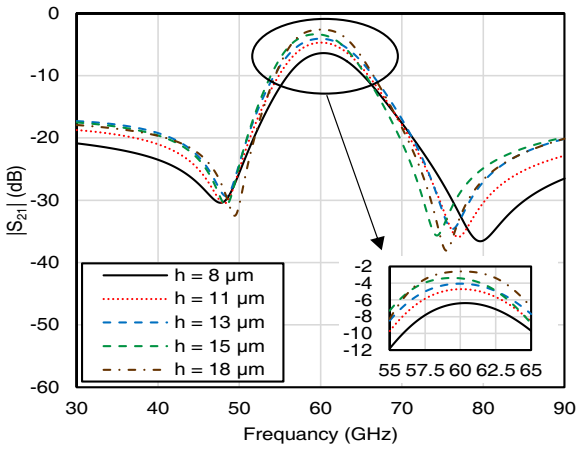
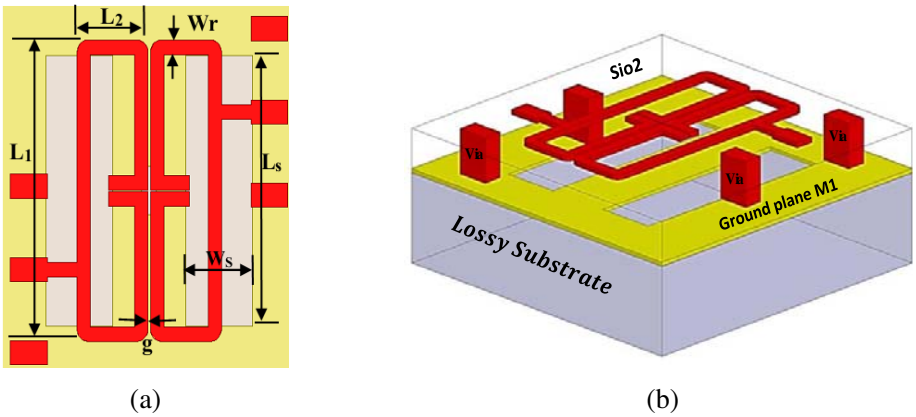


Figure 7. Simulated $|S_{21}|$ versus frequency at different oxide height.



(a) (b)

Figure 8. The simulation layout of the proposed BPF with slots for virtual oxide height increase. (a) Top view. (b) Three-dimensional view of the proposed BPF.

Table 1. Insertion loss at different SiO_2 thicknesses.

Dimensions (µm)					FBW (%)	IL (dB)
h	g	L_1	L_2	W_r		
8	5.3	545	100	12	13.6	6.3
11	6.9	542	100	14	13.6	4.6
13	7.5	535	100	14	13.6	4
15	8	530	100	20	13.6	3.3
18	7.3	520	100	30	13.6	2.6

This slot underneath a transmission line affects the electric field distribution between the resonators traces and ground plane. As the effective transverse height between the resonators and ground plane increases, the capacitance per unit length of the line decreases. Hence less power is coupled to the ground plane. Moreover, the resonators can be realized with wider trace widths and lower attenuation constant leading to lower losses.

On the other hand, this section (the slot and transmission line above the slot) can be represented as an inductor which improves the matching and filter external quality factor. Consequently, more power

coupled to the resonators from the external feeding circuit and less power coupled to the ground plane which leads to an improvement in the filter insertion loss without affecting the filter bandwidth. These characteristics are identical to that we achieve when we actually increase the oxide height.

In order to optimize the size of the proposed slots, we performed a parametric study that utilizes Q_u, calculated using Eq. (4) [18], to analyze the performance variation of the proposed BPF due to the change in slot dimensions, where g_i is the ith coefficient of the prototype filter that is Butterworth in our design, and n is the filter order.

$$Q_u = 4.343 \times \frac{\sum_{i=0}^{2n-1} g_i}{BW \times IL} \tag{4}$$

Figures 9 and 10 present the extracted Q_u variation with the slot width (W_s) and slot length (L_s), respectively. As the slot width and length increase, Q_u improves. The peak Q_u is achieved when $W_s = 60\,\mu\text{m}$ and $L_s = 335\,\mu\text{m}$. Beyond these values, Q_u drops due to increased coupling to the lossy CMOS substrate due to its low resistivity. The optimized BPF dimensions, employing the slots for virtual height increase, are listed in Table 2.

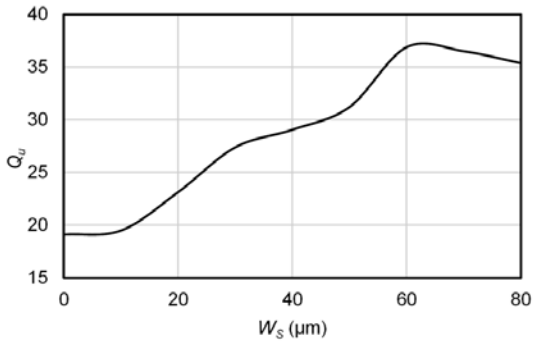


Figure 9. Effect of slot width (W_s) variation on Q_u at $L_s = 335\,\mu\text{m}$.

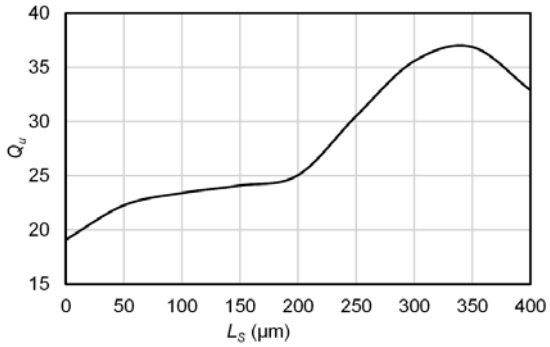


Figure 10. Effect of slot length (L_s) variation on Q_u at $W_s = 60\,\mu\text{m}$.

Table 2. Dimensions* of the optimized BPF with the slots.

h	g	L_1	L_2	W_r	W_s	L_s
8	3.4	370	100	18	60	335

*all dimensions are in μm

Then, we compared the simulated |S-parameters| performance of the proposed BPF with the BPF without any slots as shown in Fig. 11. The proposed BPF has an improved IL from 6.4 dB to 3.3 dB which is 3.3 dB improvement while maintaining the same FBW of 13.6%. Additionally, as shown in Fig. 12, the simulated |S-parameters| of the proposed BPF with virtual height increase is almost identical to that of the one with physical height increase of 15 μm. From these comparisons, we can interpret that the proposed technique has virtually increased the oxide height from 8 μm to 15 μm.

5. FABRICATION AND MEASUREMENTS

A prototype BPF is fabricated using the 0.18 μm TSMC CMOS process. Fig. 13 shows the chip micrograph of the fabricated BPF. The chip size is $0.378 \times 0.43\,\text{mm}^2$ including measuring pads. We have performed measurements using Keysight Vector Network Analyzer (PNA-E8361C) which allows characterization up to 67 GHz. Then, we compare the simulated and measured |S-parameters| in Fig. 14 in which good agreement for the transmission ($|S_{21}|$) and reflection characteristics ($|S_{11}|$) is realized. The fabricated BPF's measured IL is 3.6 dB at 59 GHz. The shift in the center frequency between

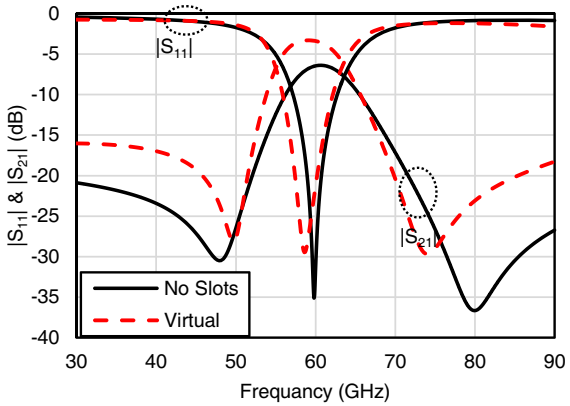


Figure 11. Simulated |*S*-parameters| performance of the proposed BPF with virtual oxide height increase (with slots) compared with the BPF without slots.

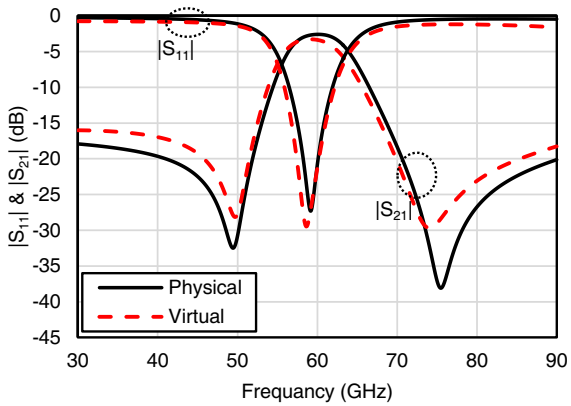


Figure 12. Simulated |*S*-parameters| performance of the proposed BPF with virtual oxide height increase (with slots) compared with the BPF with physical height ($h = 15\,\mu$m).

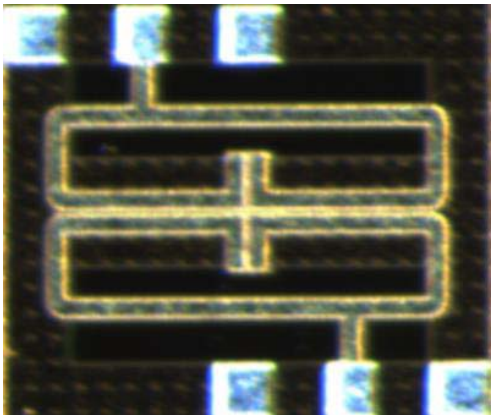


Figure 13. Microphotograph of the fabricated BPF.

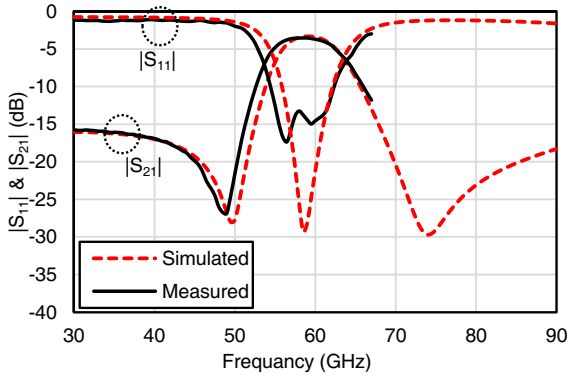


Figure 14. Simulated and measured |*S*-parameters| of the fabricated BPF.

Table 3. Performance summary and comparison with literature BPFs.

Reference	CMOS Technology	f_0 (GHz)	Area (λ_g^2)	IL (dB)	FBW (%)
[4] (2011)	0.18 µm	57.5	0.068	2.77	24
[5] (2012)	0.13 µm	60	0.04	4.1	17
[6] (2013)	0.18 µm	60	0.028	4	38
[7] (2014)	0.18 µm	77	0.018	2.9	27
[8] (2016)	0.18 µm	59	0.015	2.85	26
[9] (2016)	0.18 µm	60	0.024	2.5	21
[10] (2017)	0.18 µm	60	0.024	2.1	34*
[13] (2018)	0.13 µm	60	0.015	2.03	47
This work	**0.18 µm**	**59**	**0.025**	**3.5**	**16.5**

*Simulated

the measured and simulated results is due to the tolerance in the fabrication parameters such as the metal trace width and dielectric thickness that have a tolerance of 10%. Finally, we summarize the performance of the fabricated BPF and compare it with other recently published BPFs in Table 3 to further verify the potential of the used approach in BPF performance enhancement.

The fabricated BPF has the best selectivity (lowest FBW) so far in CMOS technology except for [5] which exhibits slightly higher bandwidth. However, the proposed BPF is superior in terms of better IL and has nearly half of the occupied area by [5]. Besides, the proposed BPF has the smallest area except compared to [7, 8, 13] which have slightly smaller areas. Nevertheless, the fabricated BPF has much higher selectivity. Finally, the same occupied area is found as [9] and [10] with higher selectivity performance. However, these designs [9, 10] have better IL performances. This comparison is an additional proof to the potential of the proposed technique in realizing small size high-performance CMOS millimeter-wave 60 GHz BPFs.

6. CONCLUSION

In this paper, we have presented a high selectivity 60 GHz on-chip OLR-BPF with low IL. We have applied shape optimization to miniaturize the size of that OLRs-BPF while producing the same characteristics as conventional OLR-BPF. After that, we have applied a virtual increase in the oxide height in order to improve this BPF's IL which has been realized by etching large slots below these BPF resonators that enables resonators to have wider trace width. Correspondingly, the attenuation coefficient of the BPF resonator traces have been reduced, and the IL has been improved. The simulated and measured responses are in good agreement. The fabricated BPF using 0.18 µm TSMC CMOS process shows an insertion loss of 3.5 dB, return loss of 15 dB, center frequency of 59 GHz, fractional bandwidth of 16.5%, and chip area including pads of $378 \times 430\,\mu m^2$.

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