*Progress In Electromagnetics Research C, Vol. 91, 227–239, 2019*

# A Frequency Agility Synthesizer with Low Phase Noise for Fully Electronic Millimeter Wave Imaging

**Chunhui Fang[1, 2], Bing Huang[1, 2], Liang Wu[1], and Xiaowei Sun[1, *]**

**Abstract**—A wide Ka-band frequency agility synthesizer with low phase noise and high frequency stability is presented in this paper, which serves as the emission source of transmitter and the local oscillator (LO) of receiver in fully electronic millimeter wave (MMW) imaging system. In order to improve operating frequency and shorten hopping time, a novel method is proposed in this synthesizer. By mixing direct digital synthesis (DDS) with multiple phase locked loops (PLLs) and multiplying the mixed signal, a high output frequency with low phase noise and rapid frequency hopping is realized. The experimental results show that the frequency synthesizer achieves frequency resolution of 1 MHz from 27 to 32 GHz and phase noise of −95 dBc/Hz at 10 kHz carrier offset. In addition, the frequency switching time is 2 µs, and broadband spurs do not exceed −60 dBc.

## 1. INTRODUCTION

At present, MMW imaging system for personal screening application is in strong demand [1, 2]. The quality and speed of imaging rely much on the performance of frequency synthesizer [3]. For instance, cross-range resolution is approximately proportional to the wavelength of transmitting signal, while range resolution is nearly inversely proportional to the bandwidth of transmitting signal. Furthermore, imaging time is partly related to frequency switching time, and imaging range depends on output power to some extent. Additionally, one dominant noise source in MMW imaging system is phase noise of frequency source [4]. The lower the phase noise of frequency source is, the lower the average noise power is, and the better the imaging performance is. In order to realize a real-time MMW imaging system with relatively long imaging distance, fine imaging resolution, and wide dynamic range, a wide frequency agility synthesizer with low phase and high spurs suppression is indispensable.

The approaches to realize MMW frequency synthesis mainly include utilizing traditional PLL [5], DDS driving PLL [6], and combining DDS with multiplier chain [7]. Using conventional PLL can acquire high frequency signal with wide frequency rage, but relatively long switching time and coarse resolution limit its application. On the contrary, DDS has the advantages of fine resolution, extremely fast frequency hopping, and low phase noise, while its comparatively narrow bandwidth, low output frequency, and poor spurious suppression are undesired [8, 9]. Therefore, it is difficult to obtain simultaneously wide bandwidth, low phase noise, fine resolution, and fast frequency hopping by single frequency synthesis method.

In this paper, an original hybrid frequency synthesizer is proposed by incorporating the superiority of DDS, PLL, and direct analog synthesis such as up-conversion and multiplier chain, which operates from 27 to 32 GHz with step of 1 MHz and possesses great performance in phase noise and frequency hopping time. Moreover, the broadband spurious suppression is better than −60 dBc.

*Received 20 December 2018, Accepted 25 March 2019, Scheduled 4 April 2019*

* Corresponding author: Xiaowei Sun (xwsun@mail.sim.ac.cn).

[1] Key Laboratory of Terahertz Solid-State Technology of Chinese Academy of Sciences, Shanghai Institute of Microsystem and Information Technology (SIMIT), Shanghai 200050, China. [2] University of Chinese Academy of Sciences, Beijing 100049, China.

This paper is organized as follows. In Section 2, the architecture of this frequency synthesizer is presented. The implementations of critical components of the synthesizer are demonstrated in Section 3, while the measurement results are given in Section 4. Finally, the conclusions follow.

## 2. DESIGN OF KA-BAND FREQUENCY SYNTHESIZER

The simplified diagram of radio frequency (RF) front end for one imaging array in fully electronic imaging system is presented in Fig. 1. It integrates 20 channels for transmitting and 20 channels for receiving. Each of two S-band signal sources is divided to 20 paths, and the signal frequency in each path is multiplied by 8 to obtain Ka-band frequency sources. The difference between transmitting signal and receiving signal is intermediate frequency (IF) signal [7]. Because of the identical architecture of every channel, the following discussion takes one transmitting channel as an example to demonstrate the design and implementation of Ka-band frequency synthesizer.

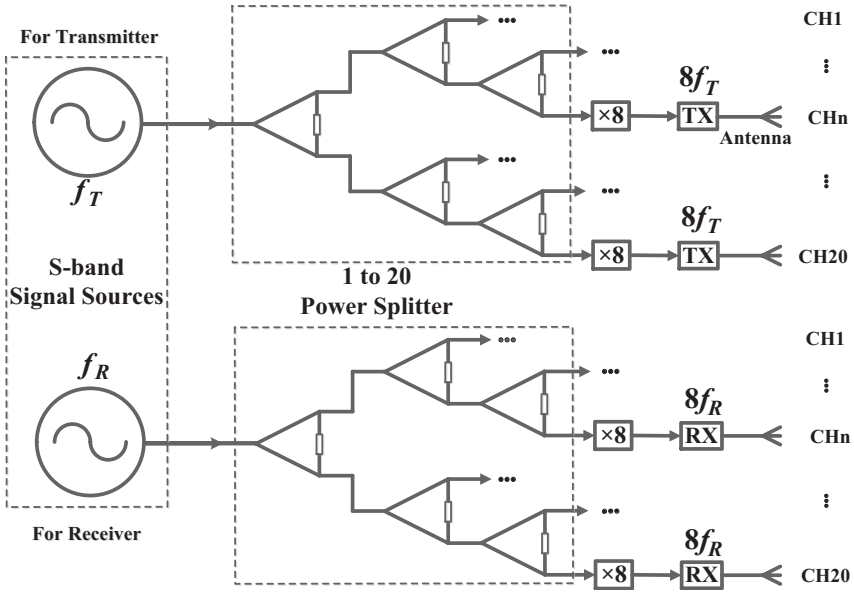



**Figure 1.** The Ka-band signal source for fully electronic MMW imaging.

In order to meet the requirements of fully electronic MMW imaging system, a novel frequency synthesis method is presented in Fig. 2. The Ka-band frequency synthesizer primarily consists of an S-band agile frequency synthesizer and a frequency multiplier (×8). The S-band frequency synthesizer is achieved by filtering and amplifying the RF signals, which are obtained by mixing IF signals from DDS with different LO signals from four PLLs, respectively. Switching between different LO signals is realized by two single-pole double-throw (SPDT) switches (SPDT1 and SPDT2). Moreover, the external oven-controlled crystal oscillator (OCXO) provides reference signals for all PLLs, and the changeable reference signal of DDS is created by PLL0. Finally, the Ka-band frequency source with broad bandwidth is achieved by multiplying the output signal from S-band frequency synthesizer.

In Fig. 2, the final output frequency of the frequency synthesizer can be written as

$$f_o = M_2 \times (F_N + M_1 \times f_{DDS}) \tag{1}$$

where $M_1$ is the multiplication factor of DDS; $M_2$ is the final multiplication factor of Ka-band frequency synthesizer; $F_N(F_1, F_2, F_3$ or $F_4)$ is the output signal of PLL (PLL1, PLL2, PLL3 or PLL4). Similarly, the resolution of the frequency synthesizer can be expressed as

$$f_{res} = M_1 \times M_2 \times f_{DDS_{res}} \tag{2}$$

where $f_{DDS_{res}}$ is the resolution of DDS. In this proposed architecture $M_1$ is 2, and $M_2$ is 8. The detailed frequencies of LO signals, IF signals, and mixed output signals are summarized in Table 1.

**Table 1.** The detail frequency of LO signals, IF signals and mixed output signals.

| LO (MHz) | IF (MHz) | RF (MHz) |
|---|---|---|
| $F_1$= 3135 | 240–396.375 | $f_1$ (3375–3531.375) |
| $F_3$= 3291.5 | 240–396.375 | $f_3$ (3531.5–3687.875) |
| $F_2$= 3448 | 240–396.375 | $f_2$ (3688–3844.375) |
| $F_4$= 3604.5 | 240–396.375 | $f_4$ (3844.5–4000.875) |

## 3. ANALYSIS AND IMPLEMENTATION OF KA-BAND FREQUENCY SYNTHESIZER

### 3.1. Analysis of Frequency Hopping Time

In a conventional hybrid synthesizer, the switching-time is limited by the long locking time of PLL. In this architecture, as shown in Table 2, all PLLs (PLL0 to PLL4) are locked when the circuit is initialized (state0). In frequency-sweeping mode, once PLL1 is mixed with signal from DDS, the outputs of PLL2 and PLL4 are disabled, but they are locked by muting the VCO output buffers, while the output of PLL3 is enabled and ready to be mixed with signal from DDS (state1). When signal mixing for PLL1 and DDS is finished, the SPDT3 switches to Mixer2, and SPDT2 switches to PLL3, ensuring signal mixing for PLL3 and DDS. Meanwhile, the output of PLL1 and PLL4 is disabled, and PLL2 is enabled and prepares for mixing (state2). The operating principles for PLL2 and PLL4 are shown in state3 and

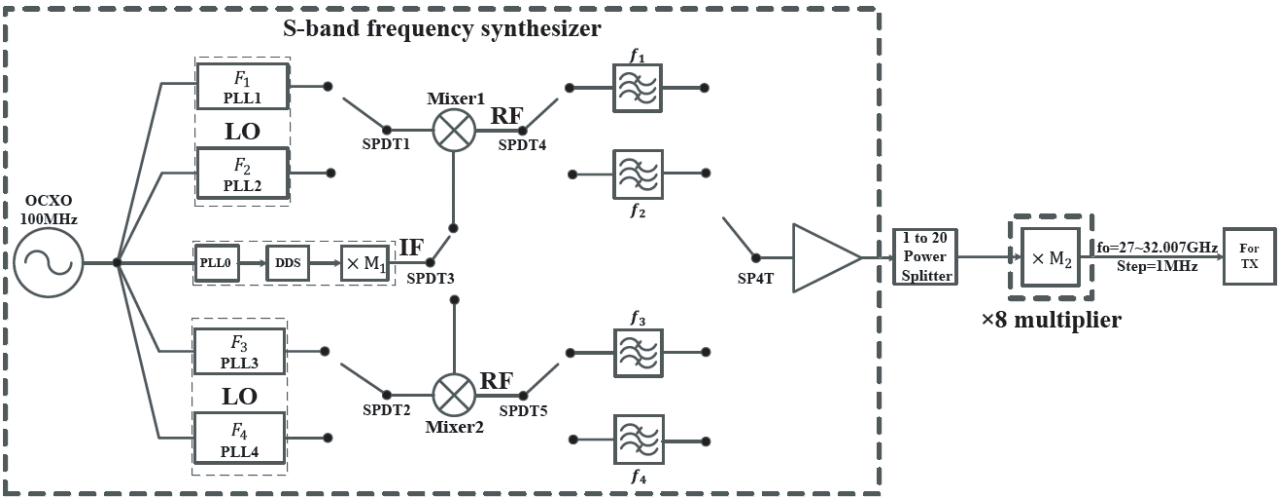



**Figure 2.** Simplified block diagram of Ka-band frequency synthesizer for one channel of transmitter.

**Table 2.** The detail operation states of four PLLs under different frequency range in frequency-sweeping mode.

| states | frequency range (MHz) | PLL1 | PLL2 | PLL3 | PLL4 |
|---|---|---|---|---|---|
| State0 | Initialization | locked | locked | locked | locked |
| State1 | $f_1$ | enabled | disabled | enabled | disabled |
| State2 | $f_3$ | disabled | enabled | enabled | disabled |
| State3 | $f_2$ | disabled | enabled | disabled | enabled |
| State4 | $f_4$ | enabled | disabled | disabled | enabled |

state4, and Table 2 shows the detailed operating states of PLLs in one period. The operating state of the frequency synthesizer is switched orderly among the five states, and the process is circulated. Not only can this method avoid long locking time of PLL, but also the interference between different LO signals and power consumption are both reduced, compared to the case that four LO signals are enabled simultaneously. In this case, the frequency hopping time is completely determined by the switching time of DDS and switches as well as the response time of filters, of which the sum approximately reaches nanosecond level. Therefore, the frequency synthesizer can achieve frequency agility.

### 3.2. Analysis of Phase Noise

The elements related to mixing are primarily composed of four PLLs generating LO signals, a DDS generating IF signals, three SPDT switches, and two mixers. Taking the limitation of low output frequency for DDS into account, this synthesizer employs four LO signals to expand frequency bandwidth. In order to eliminate the time of waiting PLLs to lock when the operating state is switched between different frequency ranges and avoids interference between different LO signals, this method employs four PLLs rather than two PLLs to generate four LO signals. Additionally, four PLLs are divided into two sections to avoid the overlap between LO signal from leakage and mixed signal at output. Each LO signal is produced by a fractional-$N$ PLL with integrated VCO and superior noise floor. The IF signal is created by multiplying the output signal from DDS.

Since the phase noise of DDS is low enough, the noise performance of PLL is dominated. The phase noise model of PLL is shown in Fig. 3. It includes a phase frequency detector (PFD&CP) with gain of $K_d$, a loop filter (LPF) with transfer function of $F(s)$, a voltage-controlled oscillator (VCO) with transfer function of $\frac{K_{VCO}}{s}$, and a divider $(1/N)$ with divider ratio of $N$. The sources of phase noise of PLL are from the reference signal ($\varphi_{REF}$), charge pump ($\varphi_{CP}$), $N$ divider ($\varphi_N$), and VCO ($\varphi_{VCO}$). Assuming that $\varphi_{REF}, \varphi_{CP}, \varphi_N$ and $\varphi_{VCO}$ are uncorrelated, the output phase noise $\varphi_o(f)$ from each noise source can be evaluated respectively [10].

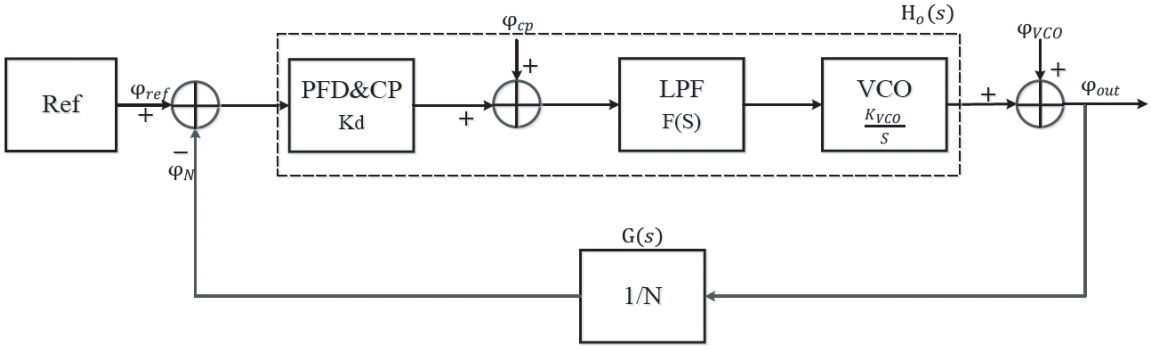



**Figure 3.** The phase noise model of PLL.

The closed loop transfer function can be written as [11]

$$H(s) = \frac{H_o(s)}{1 + H_o(s)G(s)} = \frac{K_d F(s)\dfrac{K_{vco}}{s}}{1 + \dfrac{1}{N}K_d F(s)\dfrac{K_{vco}}{s}} \tag{3}$$

where $H_o(s)$ is the open loop transfer function, and $G(s)$ is the reverse loop gain.

The output phase noise contributed by $\varphi_{REF}$ and $\varphi_N$ is given by

$$\varphi_{o,REF\&N} = H(s) \cdot (\varphi_{REF} + \varphi_N) = (\varphi_{REF} + \varphi_N) \cdot \frac{K_d F(s)\dfrac{K_{vco}}{s}}{1 + \dfrac{1}{N}K_d F(s)\dfrac{K_{vco}}{s}} \tag{4}$$

The output phase noise contributed by $\varphi_{CP}$ is represented as

$$\varphi_{o,CP} = \frac{H(s)}{K_d} \cdot \varphi_{CP} = \frac{\varphi_{CP} F(s) \dfrac{K_{vco}}{s}}{1 + \dfrac{1}{N} K_d F(s) \dfrac{K_{vco}}{s}} \tag{5}$$

The output phase noise contributed by $\varphi_{VCO}$ can be formulated as

$$\varphi_{o,VCO} = \frac{H(s)}{H_o(s)} \cdot \varphi_{VCO} = \frac{\varphi_{VCO}}{1 + \dfrac{1}{N} K_d F(s) \dfrac{K_{vco}}{s}} \tag{6}$$

Therefore, the phase noise of PLL can be approximately written as the sum of output phase noises from the reference signal, $N$ divider, charge pump, and VCO. Therefore, the output signal is

$$\begin{aligned}
\varphi_o &= \varphi_{o,REF\&N} + \varphi_{o,CP} + \varphi_{o,VCO} \\
&= (\varphi_{REF} + \varphi_N) \cdot \frac{K_d F(s) \dfrac{K_{vco}}{s}}{1 + \dfrac{1}{N} K_d F(s) \dfrac{K_{vco}}{s}} + \varphi_{CP} \cdot \frac{F(s) \dfrac{K_{vco}}{s}}{1 + \dfrac{1}{N} K_d F(s) \dfrac{K_{vco}}{s}} + \varphi_{VCO} \cdot \frac{1}{1 + \dfrac{1}{N} K_d F(s) \dfrac{K_{vco}}{s}} \\
&= (\varphi_{REF} + \varphi_N) \cdot N \cdot C_L(s) + \varphi_{CP} \cdot \frac{N}{K_d} \cdot C_L(s) + \varphi_{VCO} \cdot [1 - C_L(s)]
\end{aligned} \tag{7}$$

where $C_L(s) = \frac{\frac{1}{N} K_d F(s) \frac{K_{vco}}{s}}{1 + \frac{1}{N} K_d F(s) \frac{K_{vco}}{s}} = \frac{1}{N} \cdot H(s)$.

The final output phase noise of PLL can be expressed as

$$\varphi_o(f) = \left[ \varphi_{REF}(f) + \varphi_N(f) + \frac{\varphi_{CP}(f)}{K_d^2} \right] \cdot N^2 \cdot |C_L(f)|^2 + \varphi_{VCO}(f) \cdot |1 - C_L(f)|^2 \tag{8}$$

where $\varphi_{REF}(f), \varphi_N(f), \varphi_{CP}(f)$ and $\varphi_{VCO}(f)$ are the phase noises from the reference signal, N divider, charge pump, and VCO, respectively. In order to achieve good performance of near-end phase noise, the reference signal with low phase noise and high phase comparison frequency are essential. The far-end phase noise of PLL is mainly dependent on VCO. Additionally, the optimum loop bandwidth is critical to phase noise of PLL.

The phase noise within loop bandwidth of LO signal can be estimated as [12].

$$PN(f) = PN_{1Hz} + 10 \log(f_{pfd}) + 20 \log(n) \tag{9}$$

where $PN_{1\,\mathrm{Hz}}$ is 1 Hz normalized phase noise of phase detector, and $f_{pfd}$ is the phase comparison frequency while $n$ is the dividing ratio. Referring to [13], when the output frequency is 3605 MHz with loop bandwidth of 250 kHz and phase detecting frequency of 50 MHz, the closed loop fractional phase noise is $-110$ dBc/Hz. In the worst case, when LO signal switches to the highest frequency of 3604.5 MHz with loop bandwidth of 200 kHz and phase detect frequency of 100 MHz, the phase noise can be estimated by Equation (9) and could be calculated as

$$PN(3604.5\,\mathrm{MHz}) \approx PN(3605\,\mathrm{MHz}) + 20 \log\left(\frac{3604.5}{3605}\right) - 3\,\mathrm{dB} = 113\,\mathrm{dBc/Hz@10\,kHz} \tag{10}$$

The simulation result of phase noise by Advance Design System is presented in Fig. 4. According to this figure, the reference phase noise is low-pass filtered, and the VCO phase noise is high-pass filtered, which is in accord with Equation (8). Therefore, in order to make a tradeoff between noise suppression of reference signal and VCO, the loop bandwidth of every PLL (PLL1 to PLL4) is optimized to about 200 kHz to obtain the best phase noise performance, which is approximately the frequency of crossover of VCO phase noise and $N$-multiplied reference phase noise curves [14].

The frequency of IF signals produced by DDS [15] is lower than forty percent of reference signal frequency. The deterioration of phase noise because of multiplication can be estimated as $20 \log N$, where $N$ is multiplication times. In this case, since $N$ is less than one, the phase noise of IF signals is at least 8 dB better than reference signal. In the worst case, when the reference frequency reaches the

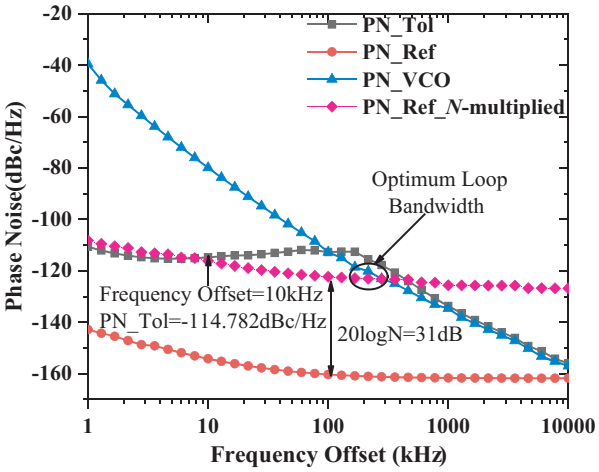



**Figure 4.** The simulation result of phase noise at 3604.5 MHz.

peak of 1200 MHz, and the output frequency of DDS is 198.1875 MHz which is then be multiplied to 396.375 MHz, the phase noise of DDS can be predicted by Equation (9) and [16].

$$PN(1200\,\text{MHz}) = -227 + 10\log\left(10^8\right) + 20\log\left(\frac{1200}{100}\right) = -125.4\,\text{dBc/Hz@10\,kHz} \tag{11}$$

$$PN(396.375\,\text{MHz}) = PN(1200\,\text{MHz}) + 20\log\left(\frac{396.375}{1200}\right) = -135\,\text{dBc/Hz@10\,kHz} \tag{12}$$

Assume that the LO signal is not related to IF signal. The phase noise of up-conversion signal is always near the worse one of LO and IF which can be expressed as [17]

$$L_o(fm) = 10 \times \log\left[10^{\frac{L_1(f_m)}{10}} + 10^{\frac{L_2(f_m)}{10}}\right] \tag{13}$$

where $L_0$, $L_1$, and $L_2$ are the phase noise spectral density of output signal, input signal, and LO signal, respectively. In this module, the phase noise of up-conversion signal is dependent largely on LO signal. After frequency multiplication of eight times, the phase noise of final Ka-band output signal would be degenerated by $20\log 8$, so the eventual phase noise is about $-96$ dBc/Hz@10 kHz.

### 3.3. Analysis of Spurs

Compared to PLL, the spurs of DDS are much more. Therefore, it is critical to reduce spurs of DDS. The simplified block diagram of DDS is shown in Fig. 5. DDS mainly includes a phase accumulator, a phase to amplitude converter (ROM), a digital-to-analog converter (DAC), and a low-pass filter (LPF). The major spurs in DDS are from the truncation error of the phase accumulator and amplitude quantization error of DAC [18].

The output frequency of DDS is

$$f = \frac{FTW}{2^N} f_{clk} \tag{14}$$

where $FTW$ is the frequency tuning word, and $N$ is the length of phase accumulator, while $f_{clk}$ is the sampling clock. The spurs introduced by phase accumulator truncation can be written as [19]

$$f_{spur} = \frac{f_{clk}}{2^{N-K}} \tag{15}$$

where $K$ is the number of bits for generation of the sine wave. The method to lower spurs is to increase the bit width of $FTW$ and phase accumulator. In comparison to phase truncation spurs, DAC images may cause higher spurs to the output of DDS. In the worst case, when the images of DAC harmonics fold back, they are near the fundamental frequency. The DAC images occur at

$$f_{ing} = A \cdot f_{clk} + B \cdot f_{out} \tag{16}$$

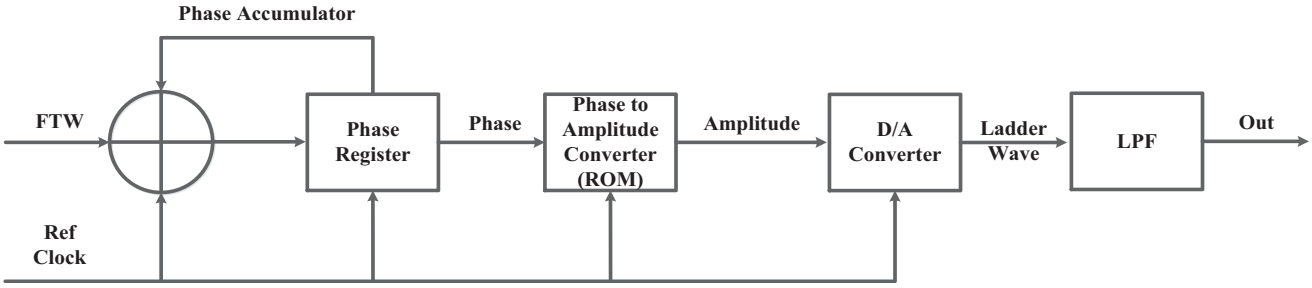



**Figure 5.** Simplified block diagram of DDS.

where $A$ and $B$ are the integer multiplication number of the sampling clock and output frequency of DDS, respectively. It is an achievable approach to reduce DAC related spurs by changing the combination of $f_{clk}$ and $FTW$ to obtain the same output frequency of DDS.

Once DDS chip is selected, one effective way to reduce spurs is to change the reference frequency. For a certain output signal of DDS, various reference frequencies can be used to acquire different frequency tuning words that make phase truncation error much lower.

### 3.4. Realization of Filter Array

In order to filter the LO leakage signals and the useless signals caused by mixing, the band-pass filter array is added behind the mixer. The filter array contains four dielectric filters with low insertion loss and high out-of-band rejection.

### 3.5. Design of Frequency Multiplier (×8)

The S-band up-conversion signal from mixer can be converted to Ka-band by frequency multiplier (×8). The simplified block diagram of frequency multiplier (×8) is presented in Fig. 6, which mainly includes three frequency doublers, three band-pass filters, and two attenuators. The filters are used to suppress the fundamental and third harmonic for frequency doublers. The attenuators are added to offer appropriate input power for next multiplier.

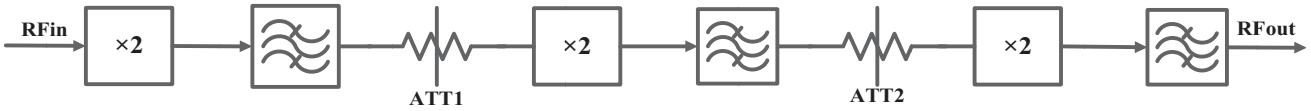


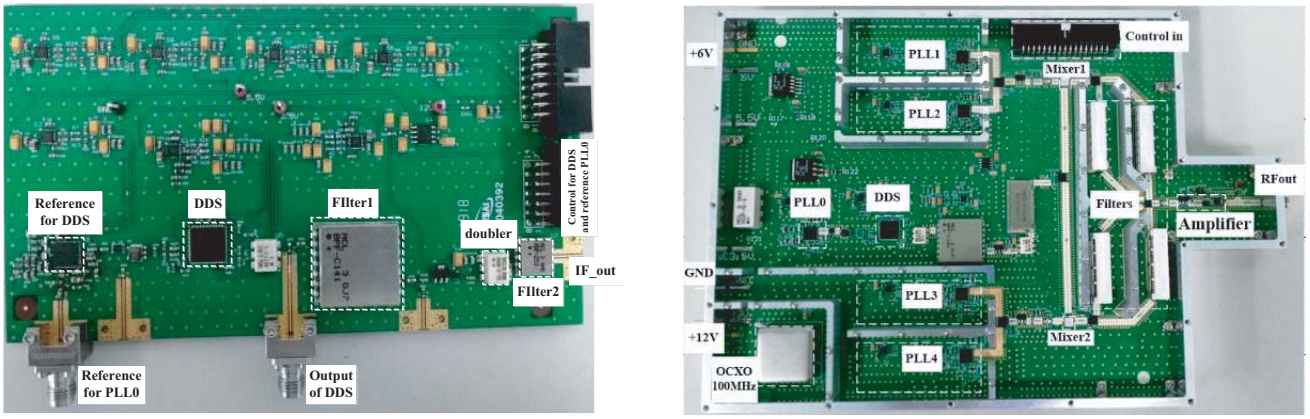

**Figure 6.** Simplified block diagram of frequency multiplier (×8).

## 4. EXPERIMENTAL RESULTS AND ANALYSIS

### 4.1. The Experimental Results and Analysis of S-Band Frequency Synthesizer

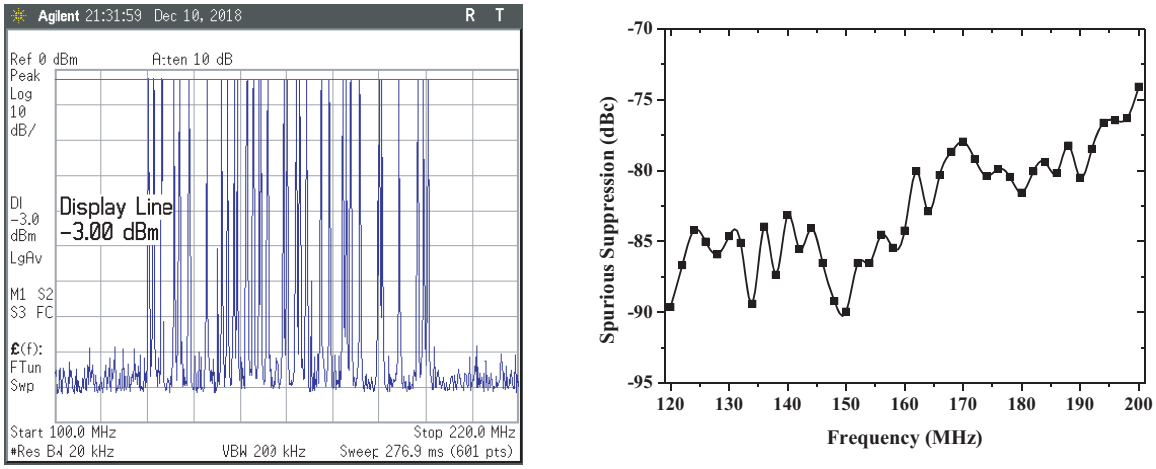
Figure 7(a) gives the generation circuit of IF signals, which is designed to choose the most suitable reference frequency and output frequency band with the lowest spurs for DDS. Fig. 7(b) shows the PCB test board and shielding cavity of the S-band frequency synthesizer. In order to prevent the disturbances, four LO signals are separated by shielding wall. The supply voltages of S-band frequency synthesizer are +6 V and +12 V, and the power consumption is about 10 W, which is lower than the case that four PLLs are all enabled (12 W). To minimize the digital processing time, the control instructions for all PLLs, DDS, SPDT switches and a single-pole four-throw (SP4T) switch are generated by Field Programmable Gate Array (FPGA).

The output frequency spectrum of DDS from 120 MHz to 200 MHz with 2 MHz step under 1.2 GHz reference clock is shown in Fig. 8(a), which is measured by Agilent E4447A spectrum analyzer. Fig. 8(b)




(a) (b)

**Figure 7.** (a) photograph of the IF signals generation circuit. (b) Photograph of the implemented S-band frequency synthesizer module.




(a) (b)

**Figure 8.** (a) The output spectrum of DDS from 120 $\sim$ 200 MHz. (b) The wideband spurious suppression of DDS.

shows that the wideband spurious suppression is better than $-75$ dBc from 120 MHz to 200 MHz, and the suppression is better than $-80$ dBc from 120 MHz to 170 MHz.

Figures 9(a), (b), and (c) show the typical frequency spectrum of S-band frequency synthesizer with spans of 500 kHz, 100 MHz, and 1 GHz, respectively, and Fig. 9(d) indicates the performance of measured spurious suppression for the S-band frequency synthesizer.

Figure 10(a) shows the phase noise of the synthesizer at output frequency of 3775 MHz. In Fig. 10(b), the measured phase noise is lower than $-113$ dBc/Hz from 3375 to 4000 MHz at frequency offset of 10 kHz and is close to the result of theoretical calculation by Equation (13).

As shown in Fig. 11(a), the output power of S-band frequency synthesizer is 22 dBm $\pm$ 1 dB. With offset of insertion loss from power splitter (14 dB) as well as coaxial cables and connectors (2 dB), the power delivered to the frequency multiplier ($\times 8$) is approximately 6 dBm, and it is appropriate input power for the first stage of frequency multiplier ($\times 8$). The measured switching time is from the reception of hopping instruction to the completion of frequency hopping for the synthesizer. It includes the switching time between two LO signals, the hopping time of IF signals, and the response time of filters. As shown in Fig. 11(b), the switching time from 3531.375 MHz to 3531.5 MHz is about 2 µs,

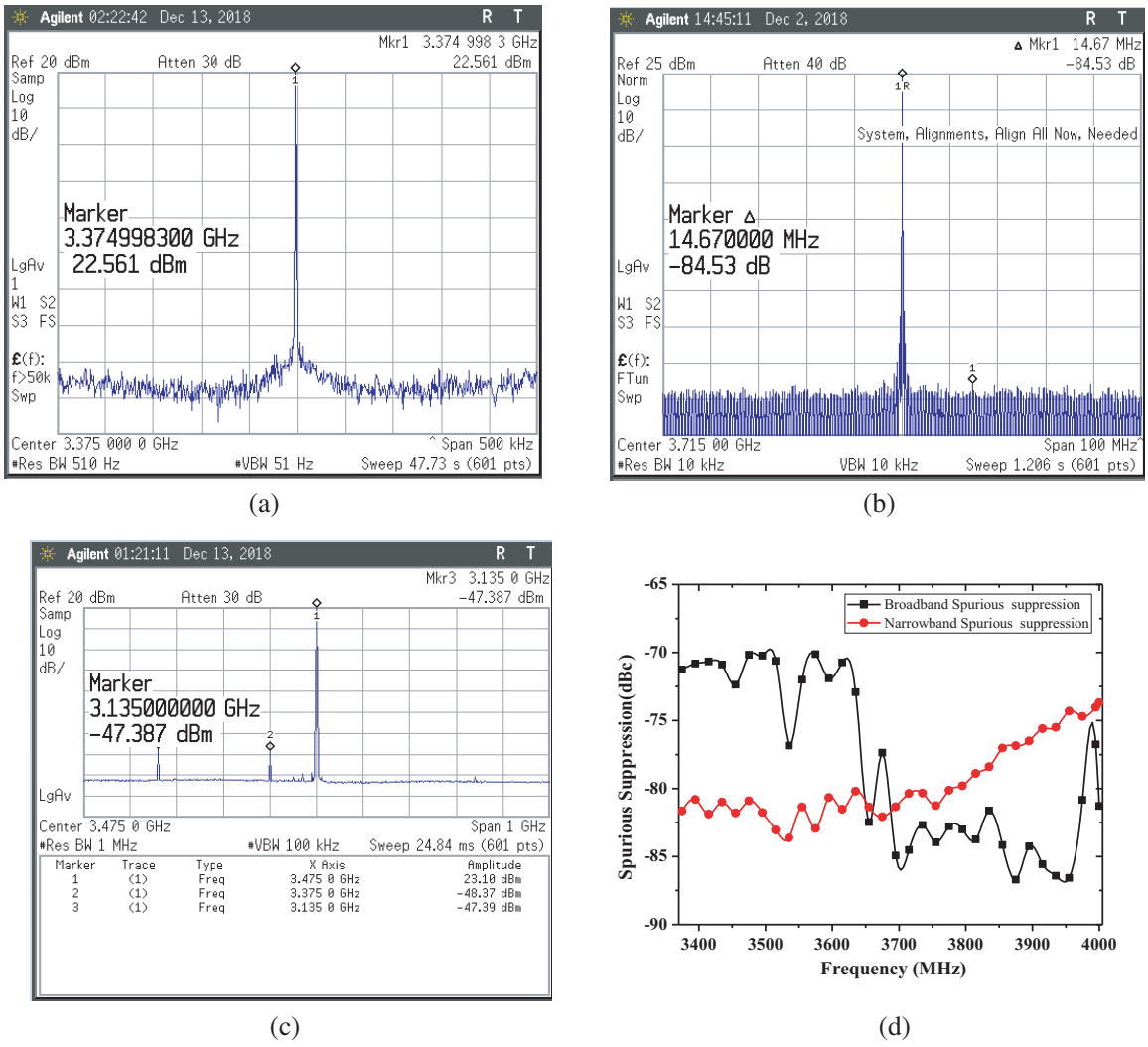
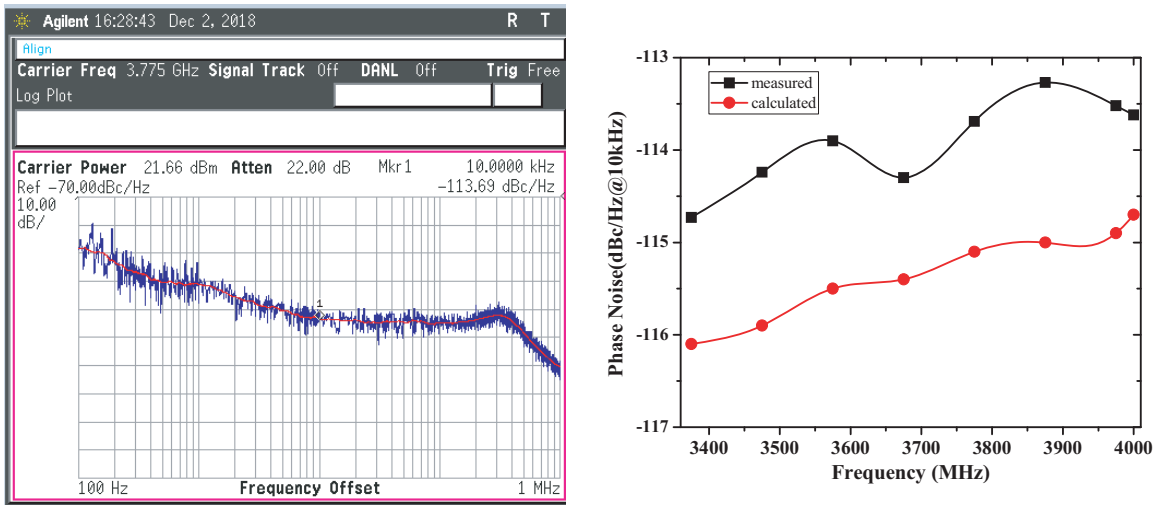



**Figure 9.** (a) The frequency spectrum of S-band frequency synthesizer (span = 500 kHz). (b) The frequency spectrum of S-band frequency synthesizer (span = 100 MHz). (c) The frequency spectrum of S-band frequency synthesizer (span = 1 GHz). (d) The measured spurious suppression of S-band frequency synthesizer.

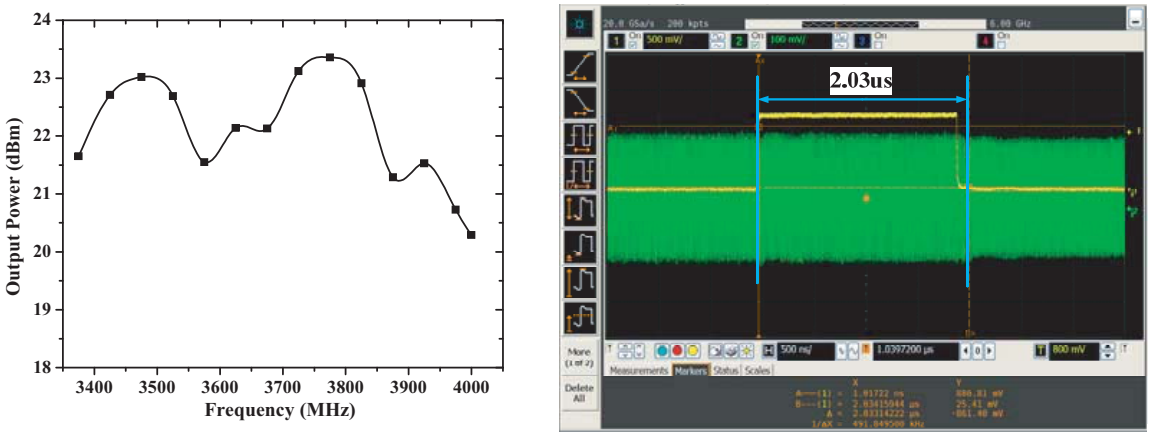
**Table 3.** Comparison with recently published results.

| Reference | [5] | [20] | [21] | [22] | [23] | This work |
|---|---|---|---|---|---|---|
| Synthesis Method | Conventional PLL | DDS Driven PLL | DDS Driven PLL | DDS Driven PLL | Mixing DDS with PLL | Mixing DDS with PLL |
| Frequency Range (GHz) | 12.5–13.5 | 11.75–12.25 | 0.003–5 | 6–18 | 12.6–13.45 | 27–32 |
| Phase Noise (dBc/Hz) | −89 @1 kHz | −104 @10 kHz | −80 @1 kHz | −93 @10 kHz | −85 @10 kHz | −95 @10 kHz |
| Hopping Time | N/A | 5 µs | 30 µs | 6 µs | N/A | 2 µs |
| Narrowband Spurious (dBc) | −50 | −50 | −55 | −50 | N/A | −50 |
| Broadband Spurious (dBc) | N/A | N/A | −65 | N/A | −69 | −60 |




(a) (b)

**Figure 10.** (a) The measured phase noise at 3.775 GHz. (b) The measured and calculated phase noise of S-band frequency synthesizer.



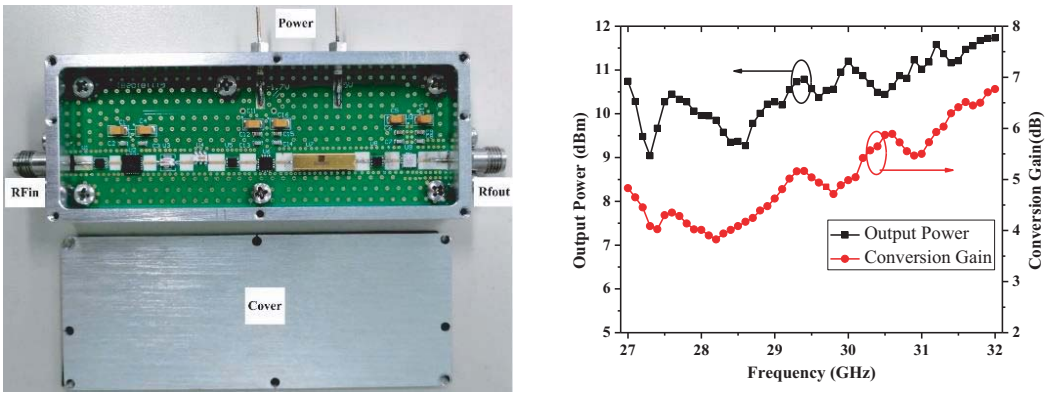

(a) (b)

**Figure 11.** (a) The output power of S-band frequency synthesizer. (b) Switching time for 3531.375 MHz to 3531.5 MHz frequency transition.

which is measured by Agilent DSO90604A digital storage oscilloscope. It is the worst case for frequency hopping because LO signal is changed. In most cases, since LO signal is fixed, the switching time is less than 2 μs. Furthermore, the frequency multiplier (×8) spends so little time that the total time of hopping Ka-band synthesizer is about 2 μs.

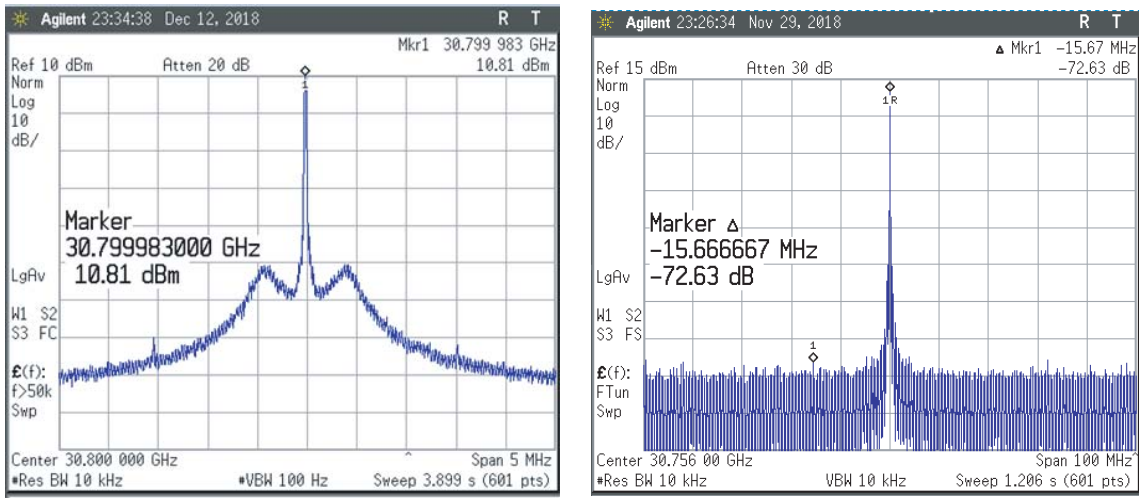
### 4.2. The Experimental Results of Frequency Multiplier (×8)

Figure 12(a) shows the implemented module of frequency multiplier (×8). As shown in Fig. 12(b), the frequency multiplier (×8) presents a flat conversion gain of 5.5 dB ± 1.5 dB from 27 GHz to 32 GHz, when input signals with amplitude of 6 dBm are generated by Agilent analog signal generator E8257D. The measured output power of final Ka-band frequency synthesizer for one channel is 10 dBm ± 1.5 dB, which is also shown in Fig. 12(b).

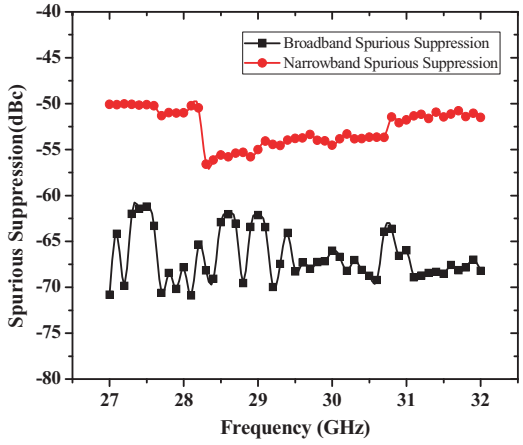



(a) (b)

**Figure 12.** (a) The module of frequency multiplier (×8). (b) The conversion gain of frequency multiplier (×8) and the measured output power of Ka-band frequency synthesizer.




(a) (b)




(c)

**Figure 13.** (a) The frequency spectrum of Ka-band frequency synthesizer (span = 5 MHz). (b) The frequency spectrum of Ka-band frequency synthesizer (span = 100 MHz). (c) The measured spurious suppression of Ka-band frequency synthesizer.

### 4.3. The Experimental Results and Analysis of Ka-Band Frequency Synthesizer

The Ka-band frequency synthesizer is realized by connecting the S-band frequency synthesizer, power splitter with the frequency multiplier (×8). As shown in Figs. 13(a), (b), and (c), the output spectrum and spurious suppression of Ka-band frequency synthesizer are presented respectively. It can be seen that the narrowband spur levels do not exceed −50 dBc, and wideband spurs are less than −60 dBc.

Figures 14(a) and (b) indicate that the phase noise of this Ka-band frequency synthesizer is lower than −90 dBc/Hz and −95 dBc/Hz at carrier offset of 1 kHz and 10 kHz respectively from 27 to 32 GHz.

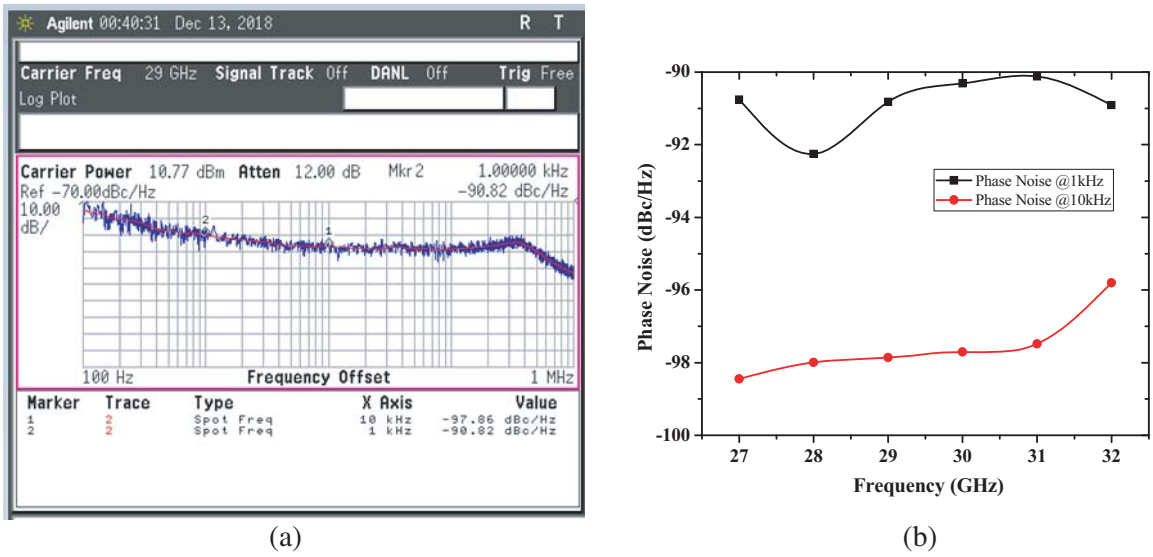



**Figure 14.** (a) The measured phase noise at 29 GHz. (b) The measured phase noise at carrier offset of 1 kHz and 10 kHz for Ka-band frequency synthesizer.

Table 3 summarizes the comparison of the proposed hybrid frequency synthesizer with recently reported results. Compared to the proposed hybrid frequency synthesizers, this synthesizer realizes lower phase noise and faster frequency hopping at higher output frequency and wider bandwidth. Meanwhile, the spurs are also low.

## 5. CONCLUSION

A wide Ka-band frequency agility synthesizer with high performance is presented in this paper, which combines the virtues of PLL, DDS, and direct analog synthesis. The experimental results demonstrate that the phase noise is better than −95 dBc/Hz from 27 to 32 GHz at a frequency offset of 10 kHz, and the narrowband spurs and broadband spurs are lower than −50 dBc and −60 dBc, respectively. Furthermore, benefitted from fast speed of DDS, the frequency hopping time is 2 μs, and the frequency resolution is 1 MHz. This Ka-band frequency synthesizer can be effectively applied to fully electronic MMW imaging system.

## ACKNOWLEDGMENT

This work is supported by the Nation Natural Science Foundation of China under contracts Nos. 61671439 and Nos. 61731021.

## REFERENCES


1. Ahmed, S. S., A. Genghammer, A. Schiessl, and L.-P Schmidt, "Fully electronic-band personnel imager of 2 $m^2$ aperture based on a multistatic architecture," *IEEE Trans. Microw. Theory Tech.*, Vol. 61, No. 1, 651–657, 2013.
2. Liu, C., M. Yang, and X. Sun, "Towards robust human millimeter wave imaging inspection system in real time with deep learning," *Progress In Electromagnetics Research*, Vol. 161, 87–100, 2018.
3. Sheen, D. M., D. L. Mcmakin, and T. E. Hall, "Three-dimensional millimeter-wave imaging for concealed weapon detection," *IEEE Trans. Microw. Theory Tech.*, Vol. 49, No. 9, 1581–1592, 2001.
4. Schiessl, A., A. Genghammer, and S. S. Ahmed, "Hardware realization of a 2 m × 1 m fully electronic real-time mm-wave imaging system," *European Conference on Synthetic Aperture Radar (EUSAR)*, Apr. 2012.
5. Wang, H., D. Guo, and L. Wang, "Design and implementation of Ku-band frequency synthesizer," *International Conference on Integrated Circuits and Microsystems (ICICM)*, Nov. 2016.
6. Zhao, Z., X. Li, and W. Chang, "LFM-CW signal generator based on hybrid DDS-PLL structure," *Electronic Letters*, Vol. 49, No. 6, 391–393, Mar. 2013.
7. Ahmed, S. S., A. Schiessl, and L.-P. Schmidt, "A novel fully electronic active real-time imager based on a planar multistatic sparse array," *IEEE Trans. Microw. Theory Tech.*, Vol. 59, No. 12, 3567–3576, Dec. 2011.
8. Kroupa, F., *Phase Lock Loops and Frequency Synthesis*, John Wiley & Sons, England, 2003.
9. Crawford, J. A., *Frequency Synthesizer Design Handbook*, Artech House, Boston, 1994.
10. Chen, M., K. Han, M. Yang, and X. Sun, "Effects of phase-locked loop bandwidth on error vector magnitude in transmitter," *Journal of Electromagnetic Waves and Applications*, Vol. 26, No. 10, 1315–1322, Jul. 2012.
11. Razavi, B., *Monolithic Phase-Locked Loops and Clock Recovery Circuits: Theory and Design*, Wiley-IEEE, Piscataway, New Jersey, 1996.
12. Banerjee, D., *PLL Performance, Simulation, and Design*, 5th edition, Texas Instruments Inc., Texas, May 2017.
13. Analog Devices Inc., "Fractional-N PLL with integrated VCO 45–1050, 1400–2100, 2800–4200 MHz," Norwood, U.S.A., Sep. 2011, [online] Available: https://www.analog.com/media/en/technical-documentation/data-sheets/hmc829.pdf.
14. Gardner, F. M., *Phaselock Techniques*, 3rd edition, John Wiley & Sons, New Jersey, 2005.
15. Analog Devices Inc., "1 GSPS direct digital synthesizer with 14-Bit DAC," Nor-wood, U.S.A., Jun. 2010, [online] Available: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9912.pdf.
16. Analog Devices Inc., "Fractional-N PLL with Integrated VCO SMT, 25–3000 MHz," Norwood, U.S.A., May 2012, [online] Available: https://www.analog.com/media/en/technical-documentation/data-sheets/hmc830.pdf.
17. Ma, H., X. Tang, F. Xiao, and X. Zhang, "Phase noise analysis and estimate of millimeter wave PLL frequency synthesizer," *Int. J. Infrared Millim. Waves*, Vol. 26, No. 2, 271–278, 2005.
18. Vankka, J., (n.d.), "Spur reduction techniques in sine output direct digital synthesis," *Proceedings of the IEEE International Frequency Control Symposium*, 951–959, Jun. 1996.
19. Caro, D. D. and A. G. M. Strollo, "High-performance direct digital frequency synthesizers using piecewise-polynomial approximation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 52, No. 2, 324–337, Feb. 2005.
20. Cui, W., X. Zhang, X. Lu, Y. Ren, M. Zhan, and B. Yan, "The design of high performance X-band frequency synthesizer based on DDS and PLL," *IEEE Cross Strait Quad-Regional Radio Science and Wireless Technology Conference*, 97–100, Jul. 2013.
21. Wang, L., Y. Yang, J. Cai, and G. Liu, "A wide frequency coverage synthesizer with high performance for 3 MHz–5 GHz transceiver," *IEEE Third International Conference on Information Science and Technology*, Mar. 2013.

22. Biswas, S. and V. Revathi, "A fast-switching low-spurious 6–18 GHz hybrid frequency synthesizer," *IEEE MTT-S International Microwave and RF Conference*, Dec. 2015.
23. Zhu, Y., H. Zhang, and W. Hong, "A frequency agile synthesizer using DDS and PLL techniques for FMCW radar," *Asia-Pacific Microwave Conference*, Dec. 2015.