Progress In Electromagnetics Research M, Vol. 81, 107–116, 2019

W-Band Single-Pole Four-Throw Switch for Multichannel High Power Transceiver Chipset Design

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Abstract—In this paper, a W-band single-pole four-throw (SP4T) switch for multichannel high power transceiver chipset design is proposed based on a standard commercial 100 nm GaAs power pseudomorphic high electron mobility transistor (pHEMT) technology. Process used in this work is optimized for use in power amplifier (PA) design, resulting in a larger drain electrode capacitance. In order to reduce the effect of large drain capacitance for switch design, a proper series capacitor is introduced. This capacitor can not only reduce the overall capacitance of the turn-off state transistor but also resonate with the parasitic inductance of the turn-on state transistor to improve the isolation. As known, a short stub is adopted to compensate the remaining parasitic capacitance. For verification, a prototype is fabricated and measured. The measured results are in good agreement with the simulated ones. The fabricated SP4T switch achieves a bandwidth of 75 GHz–96 GHz, with an insertion loss and isolation about 4.8 dB and 28 dB, respectively. The fabricated switch also realizes a Pin1 dB about 22 dBm.

1. INTRODUCTION

Recently, more and more attention has been paid to the applications of millimeter wave, such as broadband wireless communication systems [1–3], millimeter wave imaging [4–7], and automotive radar [8–11]. RF/MMW multiple-throw switches are of great importance to these systems in which multichannel transceiver chipset is utilized. In the past decades, a lot of fabrication technologies (GaAs PIN, InGaAs mHEMT, GaN HEMT, SiGe PIN, SiGe HBT, CMOS) and design methods have been adopted to realize RF/MMW switch design.

Monolithic switches fabricated using PIN diode have realized good performance even up to millimeter wave frequency [12–14]. Nevertheless, PIN fabrication process is incompatible with other semiconductor processes. In other words, it cannot be integrated with other transmitter/receiver (T/R) circuit blocks (PA, LNA, Mixer, etc.) to realize SoC design. Recently, silicon-based circuits have received more and more attention duo to the advantages of low cost and high integration [15–17]. However, silicon-based circuit has the weakness of low gain, high noise, and is unbearable for high power requirement compared with III-V compound semiconductor circuit. These shortcomings of silicon-based active or passive device result in the limitation of the application of silicon-based switches. There are several reported MMW switches fabricated using III-V compound semiconductor process [18–21]. In those articles, the layout and circuit model of transistor are redesigned and optimized specially for switch applications. Moreover, the processes used in those works are always expensive, still in development stage and not accessible for public, which is unfriendly to massive commercial applications. For this reason, a design method for W-band multiple-throw switch design is proposed using a standard commercial GaAs power pHEMT process in this work.

Received 27 April 2019, Accepted 22 May 2019, Scheduled 27 May 2019

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In this paper, a novel W-band SP4T switch is proposed based on a standard commercial 100 nm GaAs power pHEMT technology. In order to reduce the effect of parasitic capacitance of the off-state transistor, a series capacitor is introduced between the transistor and switch branch. It can not only decrease the overall parasitic capacitance of off-state transistor but also resonate with the series inductance of on-state transistor to improve isolation of the switch. The measured results show that the proposed SP4T switch achieves an insertion loss about 4.8 dB, and the isolation is all above 28 dB from 75 GHz to 96 GHz. A Pin1 dB about 22 dBm is also realized.

2. DESIGN OF THE RF/MILLIMETER-WAVES WITCH

2.1. Analysis of the Design Principle of the Switch

The series, series-shunt and quarter-wave shunt topology are well-established configurations for RF/MMW switch design as shown in Figure 1. For series device, the signal passes through when the transistor is turned on, while the signal is blocked if the transistor is turned off. However, it becomes unachievable to use series topology at high frequency because of capacitive feed in the off-state and adding loss in the on-state of the switch [22]. For series-shunt switch structure, the series transistor is turned on while the shunt transistor is turned off at the on-state branch of the switch, and it is just in the opposite state at the off-branch [23]. Unfortunately, this structure also suffers from the effect of parasitic parameters of series transistor at high frequency. Accordingly, the quarter-wave shunt configuration becomes the most common choice for millimeter wave switch design [24]. For this topology, an approximate short circuit is created at the drain of the transistor when the gate voltage is biased at a high voltage level. The short impedance is transformed to an open circuit state by the quarter-wave impedance transformer. The open circuit blocks the signal at the common port; therefore, no signal can flow towards this port. Gate voltage of the other device is biased at a low value, which presents a high impedance at the drain of the transistor. Eventually, the signal wave can pass through the on-state branch. Besides, a shunt short stub is always adopted to compensate the parasitic capacitive effect of the off-state transistor.

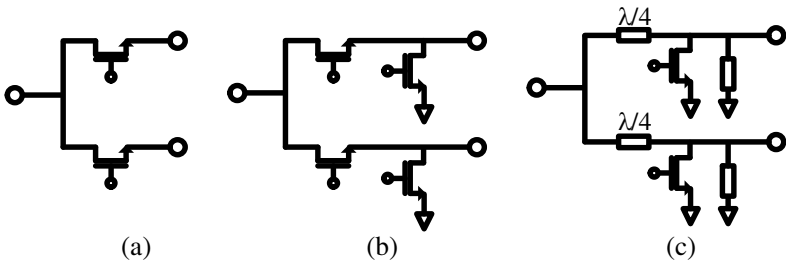

Figure 1. (a) Schematic diagrams of the switch with traditional series, (b) series-shunt and (c) quarter-wave shunt configurations.

For quarter-wave shunt switch, the insertion loss of the switch depends on how large of the drain impedance of the off-state transistor can be presented, while the isolation is determined by how small the drain electrode impedance can be realized. The insertion loss and isolation of the switch can be expressed with following Equations (1)–(5) [25]:

$$R_{T-off} = \frac{Z_0^2}{R_{on}//Z_0} \tag{1}$$

$$R_{T-on} = \frac{Z_0^2}{R_{off}//Z_0} \tag{2}$$

$$\Gamma = \frac{R_{T-on}//R_{T-off} - Z_0}{R_{T-on}//R_{T-off} + Z_0} \tag{3}$$

$$IL = \sqrt{(1-\Gamma^2)\left(\frac{R_{T-off}}{R_{T-off}+R_{T-on}}\right)\left(\frac{R_{off}}{R_{off}+Z_0}\right)} \tag{4}$$

$$ISO = \sqrt{(1-\Gamma^2)\left(\frac{R_{T-on}}{R_{T-off}+R_{T-on}}\right)\left(\frac{R_{on}}{R_{on}+Z_0}\right)} \tag{5}$$

where Z_0 is the characteristic impedance of the quarter-wave transmission line; R_{on} and R_{off} represent the impedance of on-state and off-state transistor; $R_{T\text{-}off}$ and $R_{T\text{-}on}$ denote the impedance of off-branch and on-branch at the common port. These expressions hold under the assumption that the shunt short stub is well designed to resonate with the capacitive effect of the shunt transistor.

Unfortunately, the formulas mentioned above are not always valid due to the large parasitic drain-source capacitance at W-band frequency, especially for the power semiconductor process in which devices are optimized for use in power circuit design.

The black solid line in Figure 2 gives the simulated response of the shunt off-state transistor with a gate width of $2*25$ µm from 0 to 110 GHz. As we know, the shunt off-state transistor should present an approximate open-circuit state at the turn-on branch of the switch. When the frequency is relatively low, the drain impedance is close to the open-circuit state. The parasitic capacitance can be compensated by the short stub easily. However, the drain electrode impedance gradually approaches the short circuit state with the increase of frequency. This is due to parasitic capacitor admittance increasing with frequency. When compensating the parasitic capacitance with a short stub, the impedance moves upward on equal conductance circle (dash circle in Figure 2). A drain impedance close to short circuit state (shown as the black square mark point) will result in the failure of compensation function of the short stub for shunt off-state transistor.

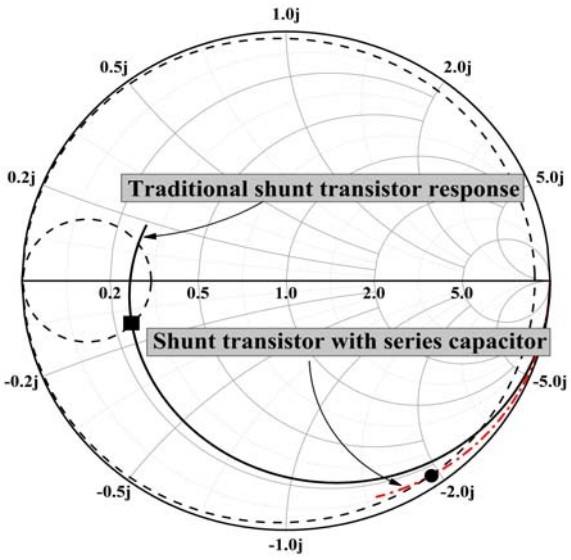

Figure 2. Simulated results of off-state response of the shunt off-state transistor from 0 to 110 GHz.

For this problem, a proper series capacitor is introduced between the drain electrode and the branch as shown in Figure 3. The overall capacitance of off-state transistor will decrease to a great extent. Simulated response of the proposed shunt structure with series capacitor is shown by the red dash dot line in Figure 2. It can be clearly observed that the capacitance effect is reduced under the action of the introduced series capacitor. The impedance at high frequency (shown as the black circular mark point) can be transformed to open circuit state with the compensation function of shunt short stub. In other words, the shunt structure can present an approximate open circuit state enabling a lossless passage for the signal wave. In addition, the introduced series capacitor can be optimized to resonate with the series inductance simultaneously. At this point, the impedance of on-state transistor will be relatively

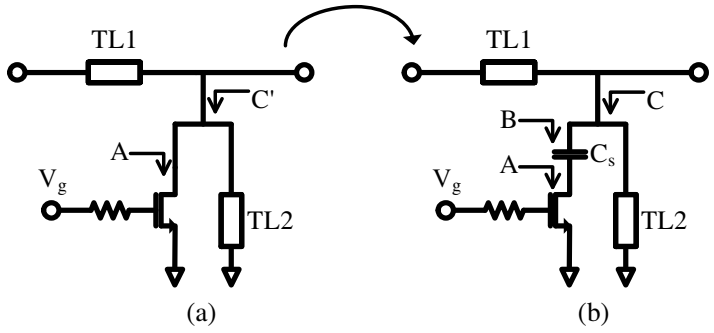

Figure 3. (a) The scheme of the traditional and (b) proposed shunt structure switch.

minimized. As mentioned before, a small drain electrode impedance of on-state transistor results in a good isolation at the off-branch.

2.2. Design Procedure of the Proposed Switch

As Figure 2 shows, the parasitic capacitance effect is largely reduced especially at high frequency which is the necessary condition for quarter-wave shunt switch design. The detailed design process of the proposed switch is discussed below.

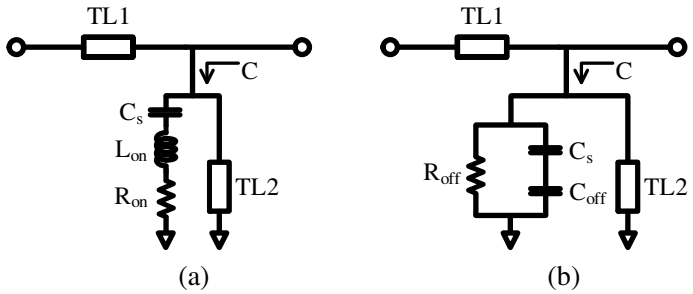

Figure 4. (a) Equivalent circuits of on-state and (b) off-state transistor models.

The equivalent circuits of the shunt on-state and off-state transistor are given in Figure 4. The drain electrode impedance of on and off-state looking into point C can be expressed by Equations (6) and (7), respectively.

$$Z_{on\text{-}shunt} = (R_{on} + j\omega L_{on} + \frac{1}{j\omega C_s})//(jZ_{stub}\tan\beta l_2) \tag{6}$$

$$Z_{off\text{-}shunt} = R_{off}//\frac{C_s + C_{off}}{j\omega C_s C_{off}}//(jZ_{stub}\tan\beta l_2) \tag{7}$$

where L_{on} and R_{on} denote series inductance and resistance at on-state, and C_{off} and R_{off} represent parasitic capacitance and resistance of off-state transistor. Z_{stub} and l_2 are the characteristic impedance and length of the short stub. C_s gives the value of the introduced series capacitor. All of the parasitic parameters of the on- and off-state transistor can be extracted from other known parameters.

In order to realize the resonance of on-state series inductance and introduce series capacitor and reduce off-state parasitic capacitance at the same time, the following Equation (8) is tenable

$$j\omega L_{on} + \frac{1}{j\omega C_s} = 0 \rightarrow C_s = \frac{1}{\omega^2 L_{on}} \tag{8}$$

The impedance of off-branch and on-branch at the common port will be reformed to the following equations:

$$Z_{T\text{-}off} = \frac{Z_0^2}{R_{on}//(jZ_{stub}\tan\beta l_2)//Z_0} \tag{9}$$

$$Z_{T\text{-}on} = \frac{Z_0^2}{R_{off}//\dfrac{1+\omega^2 L_{on}C_{off}}{j\omega C_{off}}//(jZ_{stub}\tan\beta l_2)//Z_0} \tag{10}$$

Γ, IL, and ISO equations are determined and rewritten as follows:

$$\Gamma = \frac{Z_{T\text{-}on}//Z_{T\text{-}off} - Z_0}{Z_{T\text{-}on}//Z_{T\text{-}off} + Z_0} \tag{11}$$

$$IL = \sqrt{(1-\Gamma^2)\left(\frac{Z_{T\text{-}off}}{Z_{T\text{-}off}+Z_{T\text{-}on}}\right)\left(\frac{Z_{off\text{-}shunt}}{Z_{off\text{-}shunt}+Z_0}\right)} \tag{12}$$

$$ISO = \sqrt{(1-\Gamma^2)\left(\frac{Z_{T\text{-}on}}{Z_{T\text{-}off}+Z_{T\text{-}on}}\right)\left(\frac{Z_{on\text{-}shunt}}{Z_{on\text{-}shunt}+Z_0}\right)} \tag{13}$$

Let's take the design procedure at 80 GHz as an example. The impedance looking into different points is displayed in Figure 5 shown with the black triangle marks. The dash line gives the change process between different points conditions, namely, the design process of the quarter-wave shunt switch. The process of traditional (A $\rightarrow$ C$'$) and proposed structure (A $\rightarrow$ B $\rightarrow$ C) are also compared in Figure 5, and the reference planes A, B, and C (C$'$) are shown in Figure 3. The capacitance effect is reduced largely after the series capacitor is added. With the compensation function of the short stub, the open-circuit response is formed for the turn-on branch of the switch; however, the traditional structure without series capacitor cannot realize the open-circuit response for the switch, which verifies the validation of the design theory. Of course, the transistor device size, the series capacitor and short stub should be optimized for several iterative loops to make a tradeoff between the insertion loss and isolation.

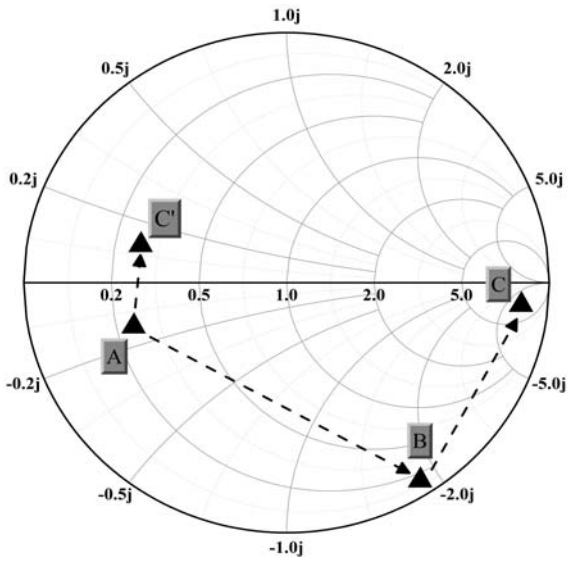

Figure 5. Simulated impedance looking into different points on the smith chart.

The schematic diagram of the proposed W-band SP4T switch is illustrated in Figure 6. It is constructed with two-stage SPDT switch. All the branches of the switch are realized with the proposed shunt structure, and the parameters of devices are obtained and optimized using the design method

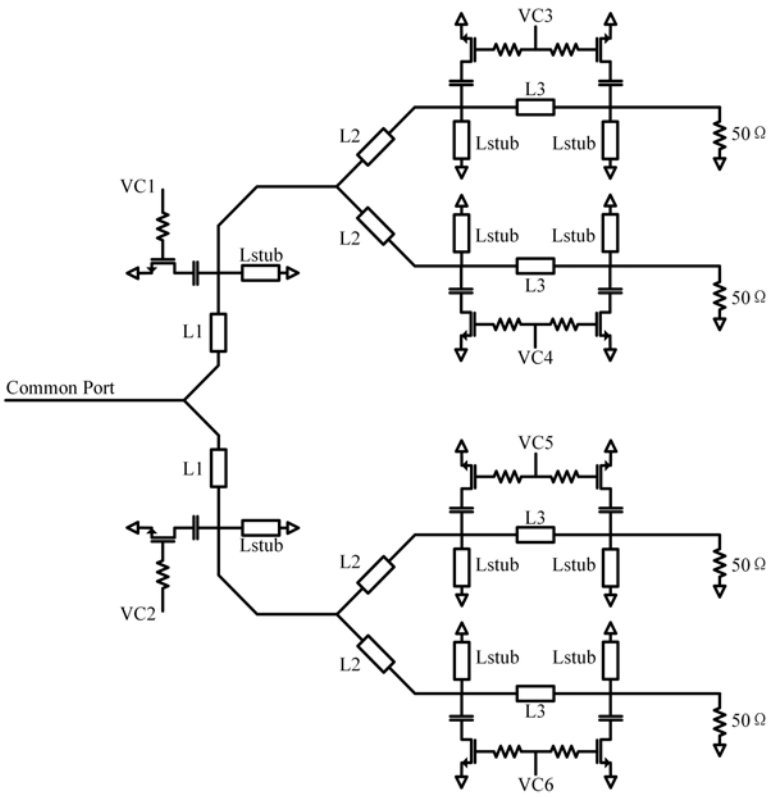

Figure 6. Schematic diagram of the proposed W-band SP4T switch.

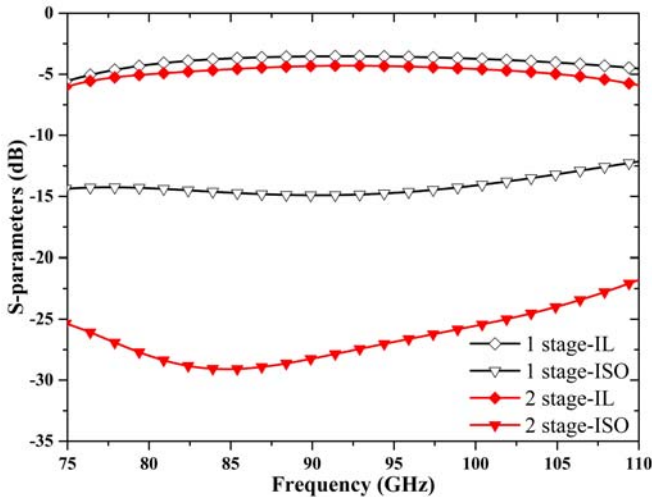

Figure 7. Simulated results of the proposed SP4T switch with different shunt stage at each output port.

mentioned above. The gate voltage of the transistor is biased through *kohm* resistor. Two shunt structures are cascaded at each output branch in order to realize a good isolation between two adjacent ports. Figure 7 gives the simulated results of the proposed SP4T switch with 1-stage and 2-stage shunt structures at each output port. The insertion loss of the switch with 2-stage shunt structure rises by only about 0.7 dB, compared with that of the switch with 1-stage shunt structure. At the same time, however, the isolation increases by an average of nearly 13 dB.

3. FABRICATION AND MEASUREMENT OF THE SWITCH

The proposed W-band SP4T switch is designed and fabricated using a standard commercial 100 nm GaAs power pHEMT technology. Figure 8 displays a chip photograph of the fabricated switch MMIC with a main size of 0.8 mm ∗ 2.0 mm.

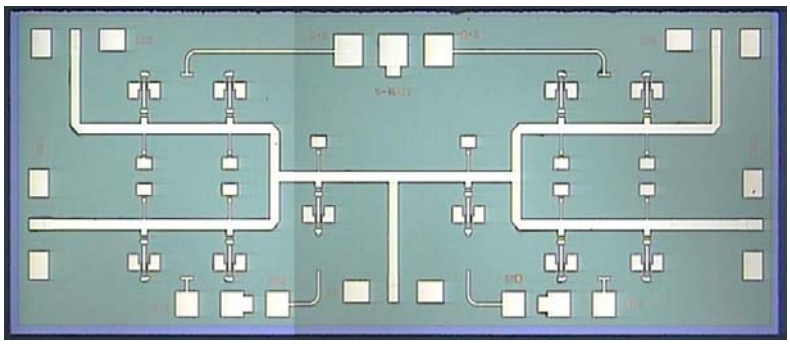

Figure 8. Chip photograph of the proposed W-band SP4T switch MMIC.

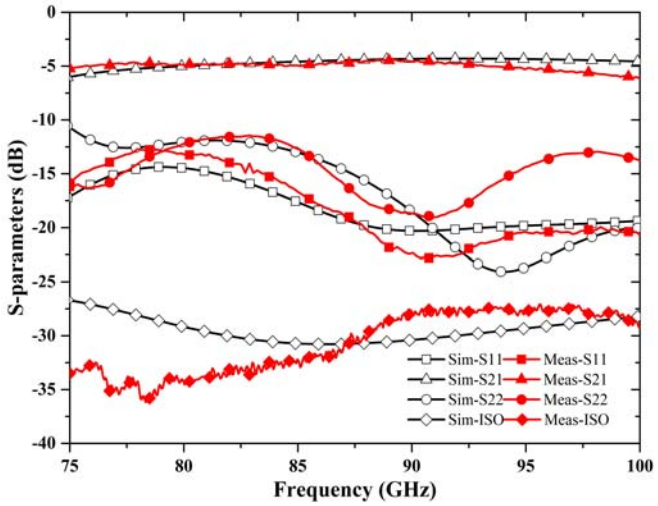

Figure 9. Measured and simulated results of S-parameters response of the fabricated switch.

S-parameters measurement is implemented using Cascade M150 probe station with Agilent N5245A Network Analyzer and Farran W-band frequency extender. The measured and simulated results of the proposed SP4T switch are shown in Figure 9. As can be seen, the measured results coincide well with the simulated ones. An insertion loss between 4.7 dB and 5.2 dB (average 4.8 dB) is realized from 75 GHz to 96 GHz, and the isolation is above 28 dB from 75 GHz to 100 GHz. The return losses, S_{11} and S_{22}, are both below −12 dB. There is only a little downward shift of the operation frequency, and the measured S_{22} goes up from 95 GHz to 100 GHz compared to the simulated S_{22} which leads to an increasing insertion loss by about 0.5 dB. The problems mentioned above are due to the inaccuracy of the device model at high frequency. The effect of inaccuracy of the model is not particularly evident at low frequencies. However, with the increase of frequency, a slight inaccuracy of the model will lead to inconsistency between the test and simulation results.

The large signal response of the fabricated switch is also measured with on-wafer test equipment. The input signal is provided by a frequency multiplier signal source with a maximum output power of 13 dBm, and the output power of the switch is measured by Agilent N1912A power meter with a power sensor W8486A. The measured and simulated results are displayed in Figure 10. As can be observed,

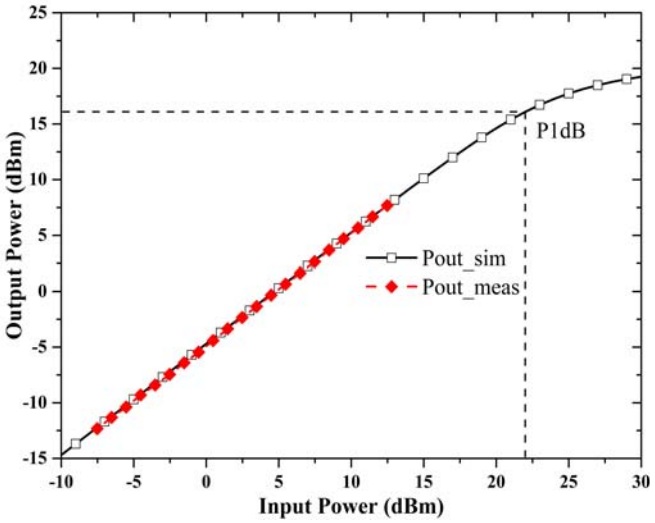

Figure 10. Measured and simulated results (@90 GHz) of large signal response of the fabricated switch.

the test results agree well with the simulated ones. The switch is tested with a maximum input power of 13 dBm due to the limited output power of the signal source, and the switch shows no compression. The simulated result gives that the proposed switch has a Pin1 dB about 22 dBm.

Table 1 summarizes the performance comparison between the proposed W-band SP4T switch and other previous works. As can be seen, SP4T switch is rarely reported compared with SPDT switch. The proposed SP4T switch realizes a good isolation and Pin1 dB performance.

Table 1. Comparison between the proposed SP4T switch and other millimeter-wave switches.

Reference	Technology	Topology	Frequency (GHz)	IL (dB)	ISO (dB)	Pin1 dB (dBm)	Pdc (mW)
[12]	GaAs PIN Diode	$\lambda/4$-shunt SPDT	75–110	1.1–1.6	> 21	n/a	n/a
[13]	SiGe PIN Diode	$\lambda/4$-shunt SPDT	77–135	1.4–2.0	19–22	> 24	10.2
[15]	130 nm CMOS	$\lambda/4$-shunt SP4T	50–70	2.0–2.4	> 32	13	0
[15]	130 nm CMOS	$\lambda/4$-shunt SPDT	50–70	3.4–3.8	> 22	13	0
[18]	50 nm InGaAs mHEMT	$\lambda/4$-shunt SPDT	64–124	2.1–3.0	38–52	19	0
[20]	50 nm InGaAs mHEMT	$\lambda/4$-shunt SPDT	70–120	1.8–2.5	29–35	> 19	0
[21]	40 nm GaN HEMT	$\lambda/4$-shunt SPDT	80–100	1.3–1.7	> 9	> 24	0
[23]	90 nm CMOS	series-shunt SPDT	75–110	6.3	> 20	11	0
[24]	130 nm SiGe HBT	$\lambda/4$-shunt SPDT	82–97	1.4–1.6	> 24	18.3	n/a
[25]	90 nm SiGe HBT	$\lambda/4$-shunt SPDT	65–110	1.4–2.8	22.8–24	16	5.5
This work	100 nm GaAs pHEMT	$\lambda/4$-shunt SP4T	75–96	4.8	> 28	22	0

4. CONCLUSION

In this paper, a W-band SP4T is designed, fabricated, and measured based on a standard commercial 100 nm GaAs power pHEMT technology. For the purpose of reducing the parasitic capacitance effect of the shunt off-state transistor, a series capacitor is introduced. Moreover, it can resonate with the series inductance of the on-state transistor to improve the isolation for the off-branch of the switch. The fabricated switch realizes an insertion loss of 4.8 dB from 75 GHz to 96 GHz, while the isolation is above 28 dB from 75 GHz to 100 GHz. No compression is shown with an input power of 13 dBm (limited by the maximum output power of signal source). The proposed switch presents a Pin1 dB of 22 dBm. The proposed W-band SP4T switch is suitable for MMW transceiver design with multiple channels, and it is a promising candidate for future MMW SoC circuit design.

ACKNOWLEDGMENT

This work is supported in part by National Natural Science Foundation of China under contracts No. 61671439 and contracts No. 61731021.

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