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A Design Oriented Linear Model for CRLH Distributed Oscillators

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Abstract—The aim of this paper is to present a model for a Composite Right-/Left-Handed (CRLH) distributed oscillator. A linear approach is used for the analysis of the circuit. The effects of the losses and of the parasitic elements, both present in the active devices and in the passive components, are included. Analytic formulas for the design of the transmission lines used in the oscillator are given. The model is validated by means of a comparison with previously published measured data.

1. INTRODUCTION

Distributed amplifier is an important wide-band element often used in microwave and millimeter wave systems [1–4]. The basic principle of this circuit has been also applied to other components, such as active dividers [5–7], frequency doublers [8–10], phase shifters [11–15], and oscillators [16–20]. For the latter ones the conventional configuration has been recently modified, replacing the low pass unit cell by a Composite Right-/Left-Handed (CRLH) topology [21, 22]. The conceptual configuration of this oscillator is shown in Fig. 1, where CRLHD and CRLHG are the drain and gate CRLH unit cells of the distributed amplifier, respectively. Each unit cell is composed by a series resonator and a parallel resonator, and for the transistor an ideal model can be assumed in this figure. Also, the drain and gate artificial lines of the distributed amplifier are connected by a feedback network (FTL) realized by means of a transmission line. As shown in [21], two output ports are available for this type of oscillator,

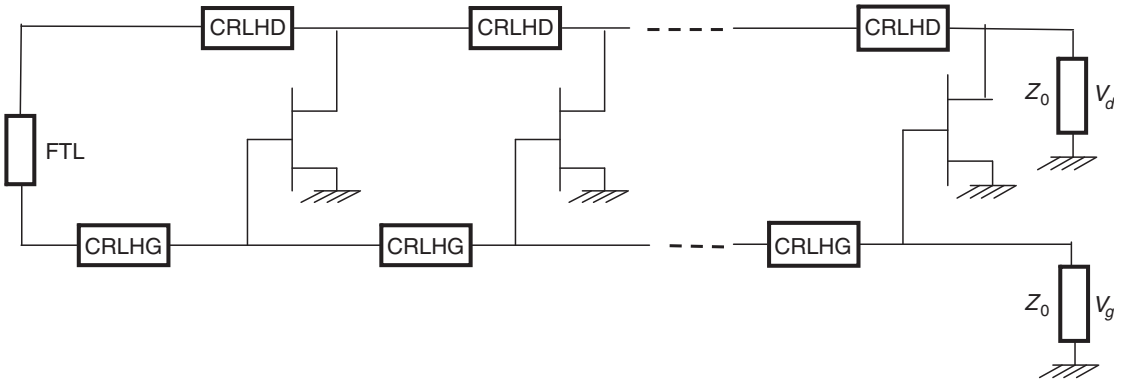

Figure 1. The distributed oscillator configuration composed by the feedback transmission line (FTL), the transistors, and the Composite Right-/Left-Handed cells termed CRLHD for the drain line and CRLHG for the gate line.

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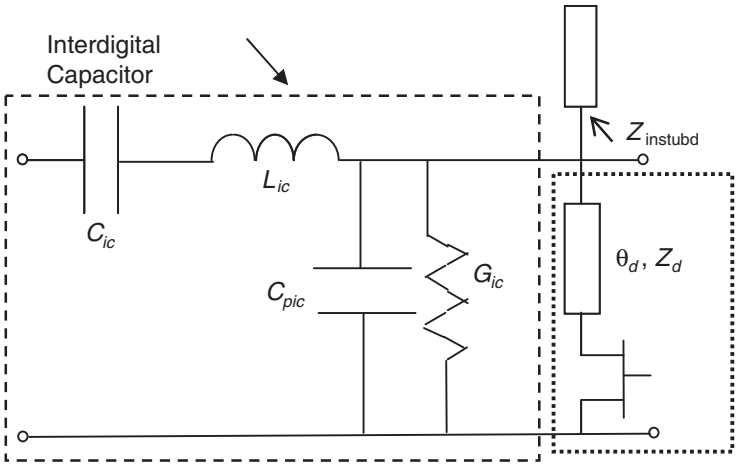


Figure 2. The unit cell of the drain line (CRLHD, taking into account the output impedance of the transistor).

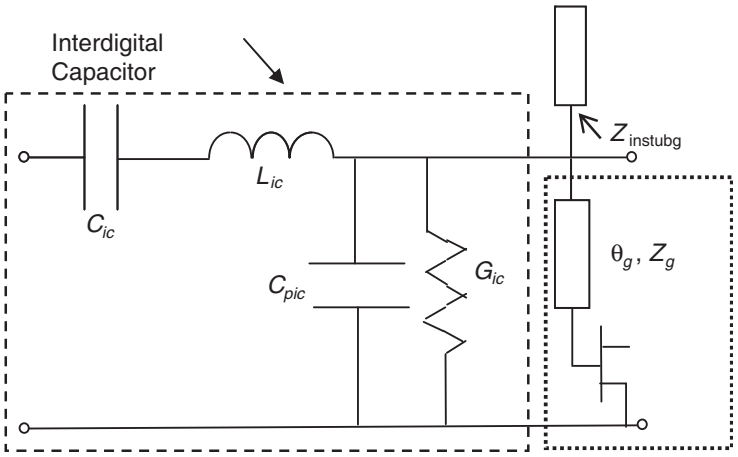


Figure 3. The unit cell of the gate line (CRLHG, taking into account the input impedance of the transistor).

where similar power level may be obtained, with these output ports located at the ends of the drain and gate lines. In practice, CRLHD and CRLHG unit cells may be obtained using interdigital capacitors to realize the series resonators, while the parallel resonators are obtained using transmission lines, where the effects of parasitic capacitances of interdigital capacitors must be included. Taking into account the input and output equivalent circuits of the transistors, the circuit configurations for the CRLHD and CRLHG unit cells used in Fig. 1 behave more complicatedly, as shown in Fig. 2 and Fig. 3, respectively, where $C_{ic}, L_{ic}, C_{pic}, G_{ic}$ are elements of the interdigital capacitor equivalent circuit (here, the same for both unit cells). This oscillator has been designed and fabricated using MGF 4941AL InGaAs HEMTs, as presented in [21]. A photo of this circuit is presented in the same reference, but it is also shown here in Fig. 4 for the clarity of this paper, where the circuit elements of CRLHD and CRLHG unit cells may be observed.

In this paper, a linear approach is proposed for the characterization of this circuit. We can note that in literature this method of analysis has been at first applied to the standard distributed oscillator [16–19], and after adopted in [21] also for the CRLH configuration. However, the analytic results presented in [21] have been obtained neglecting the following elements: the drain and gate resistors, which account for the losses in the transistor; the drain and gate inductors; the parasitic components of the CRLH passive cell. The purpose of this work is to develop a model for the oscillator which includes all

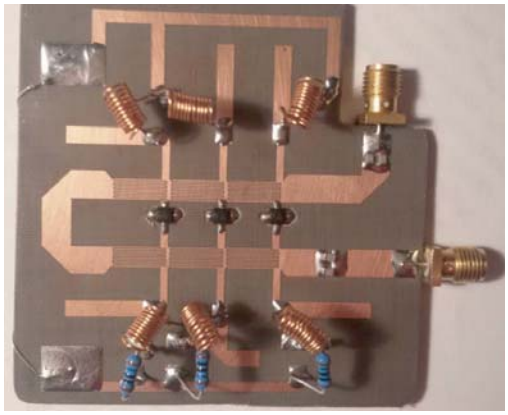


Figure 4. Photograph of the fabricated CRLH distributed oscillator which uses three active devices ($N = 3$) [22].

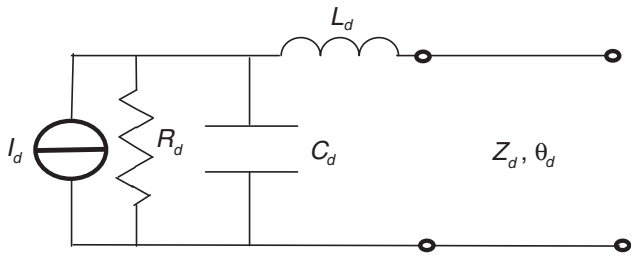


Figure 5. The model of the part of the drain line unit cell included in the dotted rectangle in Fig. 2. It is composed by the equivalent circuit of the drain of the transistor and by the connecting line with length θ_d.

these effects, thus providing, in the general case, the analytic expression for the oscillation condition. Moreover, closed-form equations for the synthesis of the transmission lines utilized in the unit cell are derived.

The outline of the paper and the new contributions are listed below. In Sections 2 and 3 the models of the gate line and of the drain line are described, respectively. Section 4 is focused on the analysis of the feedback network, which is the key-element for transforming the distributed amplifier in an oscillator. Subsequently, the oscillation condition is imposed in the general case, including losses and parasitic effects. These analytic results are used in Section 5 for producing an innovative design procedure, which is the most important contribution of this work. In Section 6, some considerations on the power of the output signals are given. The validation of the presented approach is discussed in Section 7, where a comparison between predicted data and previously published experimental results is illustrated. Concluding remarks are provided in Section 8.

2. THE ANALYSIS OF THE DRAIN LINE

The equivalent circuit of the CRLHD unit cell is represented in Fig. 2. The transmission line of electrical length θ_d is used to facilitate the physical connection of the transistor drain, inside the drain unit cell. The part of the cell included in the dotted rectangle is detailed in Fig. 5, where the equivalent circuit of the transistor drain together with the connecting transmission line is shown. This one port network can be characterized by means of the Norton's theorem, so obtaining the equivalent circuit depicted in Fig. 6. For the admittance Y_{nd} and the current I_{nd}, we have:

$$Y_{nd} = \frac{1}{Z_d} \frac{Z_d + jZ_{\mathrm{LRC}}\mathrm{tg}\theta_d}{Z_{\mathrm{LRC}} + jZ_d\mathrm{tg}\theta_d} \tag{1}$$

and

$$I_{nd} = \frac{I_d}{P_2 \cos\theta_d} \tag{2}$$

where:

$$Z_{\mathrm{LRC}} = j\omega L_d + \frac{R_d}{1 + j\omega C_d R_d} \tag{3}$$

and

$$P_2 = 1 + (j\omega L_d + jZ_d\mathrm{tg}\theta_d)\left(\frac{1}{R_d} + j\omega C_d\right) = |P_2|\, e^{j\psi_2} \tag{4}$$

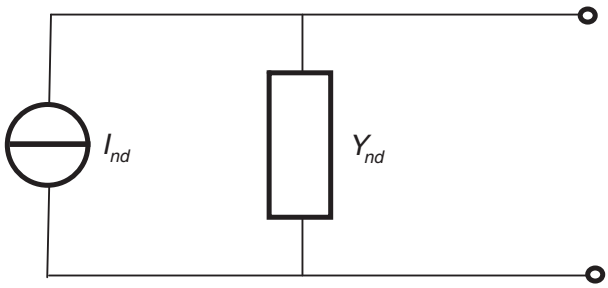


Figure 6. The Norton model for the circuit in Fig. 5.

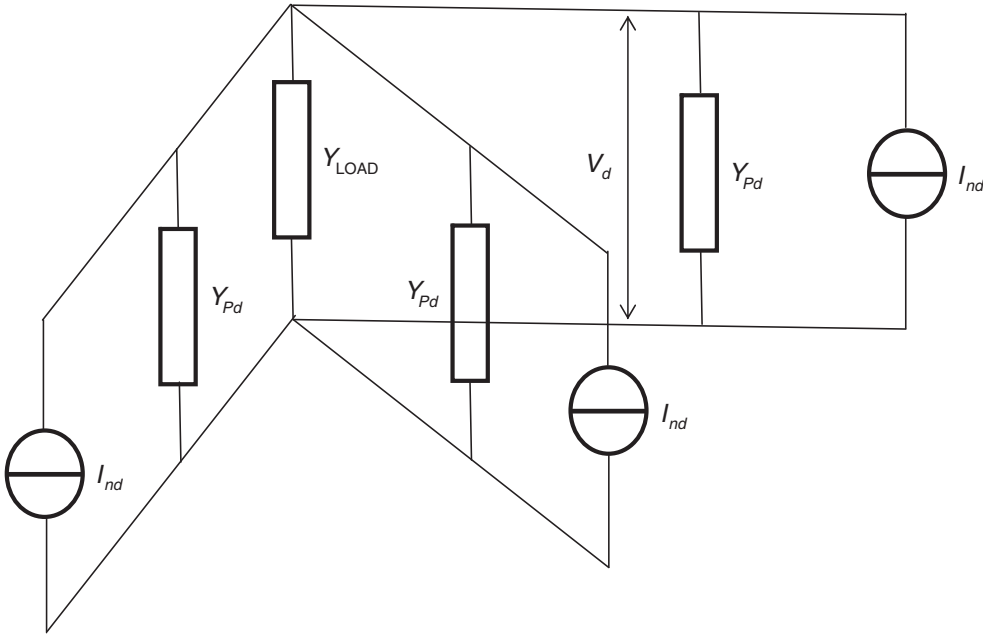


Figure 7. The equivalent network for the drain line.

Let's assume that the circuit composed by the inductor L_{ic} and the capacitor C_{ic} resonates at the oscillation frequency f_0. Hence it becomes a short circuit, and according to Figs. 2, 5, and 6, the unit cell can be modeled by the current generator I_{nd} and the admittance Y_{pd}, which is defined as follows:

$$Y_{pd} = Y_{nd} + j\omega_0 C_{pic} + \frac{1}{Z_{\text{instubd}}} + G_{ic} \tag{5}$$

where Z_{instubd} is the input impedance of the stub in the drain unit cell. Therefore, at the frequency of resonance f_0, for the whole drain line we can obtain the network shown in Fig. 7. The admittance Y_{LOAD} is obtained by adding the load admittance of the drain line, that is $1/Z_0$, to the input admittance of the feedback network loaded by the gate line.

3. THE ANALYSIS OF THE GATE LINE

The equivalent circuit of the CRLHG unit cell is shown in Fig. 3. The transmission line of electrical length θ_g has a similar role to the line of electrical length θ_d used in the drain unit cell. It must be mentioned that the lines of electrical lengths θ_g and θ_d also ensure a separation between the gate and drain lines. In this way, the electromagnetic coupling between the two parts of the circuit is avoided. It is observed that the gate unit cell in this case has the same topology as that for the drain line (see

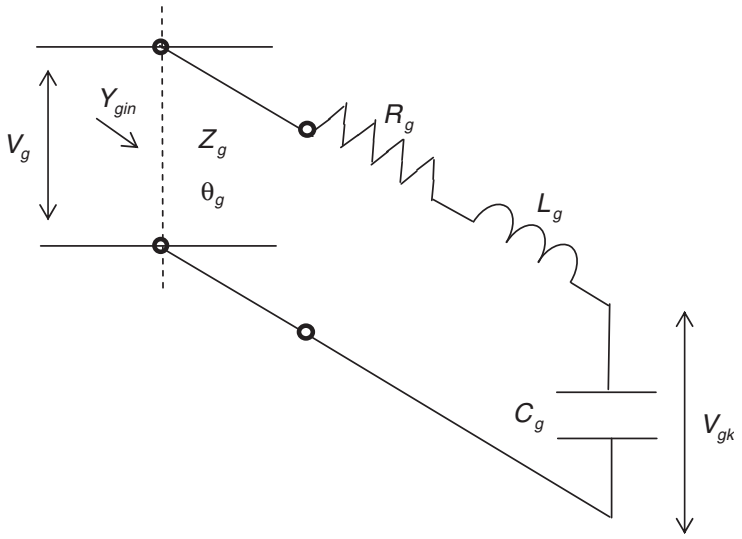


Figure 8. The model of the part of the gate line unit cell included in the dotted rectangle in Fig. 3. It is composed by the equivalent circuit of the gate of the transistor and by the connecting line with length θ_g.

Fig. 2). The differences are in the value of the input impedance of the stub and in the electric parameters of the connecting line. The model of the elements included in the dotted rectangle is shown in Fig. 8, where the equivalent circuit of the transistor gate and the connecting line are present. For the input admittance Y_{gin} we find:

$$Y_{gin} = \left[Z_g \frac{Z_{gk} + jZ_g \mathrm{tg}\theta_g}{Z_g + jZ_{gk}\mathrm{tg}\theta_g} \right]^{-1} \tag{6}$$

where Z_{gk} is given by:

$$Z_{gk} = j\omega L_g + \frac{1}{j\omega C_g} + R_g \tag{7}$$

The following relationship between V_{gk} and V_g can be written:

$$V_{gK} = P_4 V_g \tag{8}$$

where:

$$P_4 = \frac{1}{j\omega C_g \left(Z_{gk} \cos\theta_g + jZ_g \sin\theta_g \right)} = |P_4| \, e^{j\psi_4} \tag{9}$$

As for the drain line, the unit cell of the gate line is characterized by an admittance Y_{pg}, which is defined at f_0 as:

$$Y_{pg} = Y_{gin} + j\omega_0 C_{pic} + \frac{1}{Z_{\mathrm{instubg}}} + G_{ic} \tag{10}$$

where Z_{instubg} is the input impedance of the stub in the gate line unit cell.

4. THE FEEDBACK NETWORK AND THE OSCILLATION CONDITION

A transmission line with characteristic impedance Z_0 and electric length ϕ_0, evaluated at f_0, is used for realizing the feedback network (see Fig. 1). If N is the number of unit cells, the load admittance of this feedback line, let say Y_{Lg}, is given by the load impedance of the gate line Z_0 and by the admittances of the N cells, and the resulting circuit may be used to compute the input admittance into the feedback line, Y_{di}, given in Fig. 9. Thus, we have the following expression for Y_{Lg} and Y_{di}:

$$Y_{Lg} = \frac{1}{Z_0} + NY_{pg} \tag{11}$$

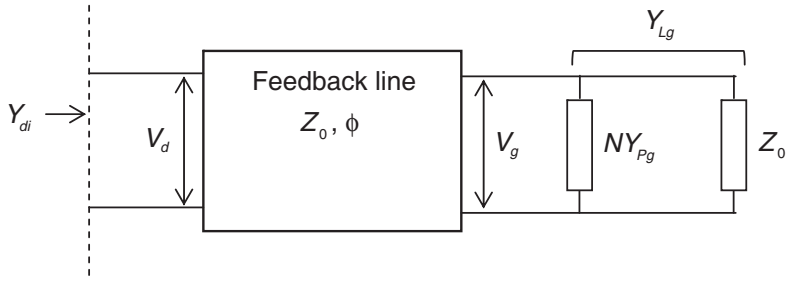


Figure 9. The feedback transmission line loaded by Z_0 and by the N gate line unit cells.

and

$$Y_{di} = \left[Z_0 \frac{1 + jY_{Lg} Z_0 \mathrm{tg}\phi}{Z_0 Y_{Lg} + j\mathrm{tg}\phi} \right]^{-1} \tag{12}$$

The relationship between V_g and V_d can be expressed as:

$$V_g = V_d \left(\cos\phi - jZ_o Y_{di} \sin\phi \right) \tag{13}$$

V_d can be calculated as the ratio of the current given by the N generators I_{nd} and the admittance obtained by adding Y_{LOAD} to NY_{pd}. Therefore:

$$V_d = \frac{-NI_{nd}}{NY_{pd} + Y_{\mathrm{LOAD}}} = \frac{-N}{NY_{pd} + Y_{\mathrm{LOAD}}} \frac{I_d}{P_2 \cos\theta_d} \tag{14}$$

where:

$$Y_{\mathrm{LOAD}} = \frac{1}{Z_o} + Y_{di} \tag{15}$$

We assume for I_d:

$$I_d = g_m V_{gK} = g_m P_4 V_g \tag{16}$$

By substituting Equation (16) in Equation (14), we obtain:

$$V_d = \frac{-N}{NY_{pd} + Y_{\mathrm{LOAD}}} \frac{g_m P_4 V_g}{P_2 \cos\theta_d} \tag{17}$$

From Eqs. (17) and (13) one then has:

$$1 = \frac{-Ng_m P_4}{P_2 \cos\theta_d} \frac{\left(\cos\phi - jZ_o Y_{di} \sin\phi \right)}{NY_{pd} + Y_{\mathrm{LOAD}}} \tag{18}$$

This equation is the oscillation condition for the CRLH distributed oscillator.

5. THE DESIGN PROCEDURE OF THE CRLH OSCILLATOR

We can note that neglecting the losses in the two stubs, their input impedances Z_{instubd} and Z_{instubg} are imaginary numbers. By using Equations (5) and (10), let us impose the following conditions at the oscillation frequency f_0:

$$j\mathrm{Im}\left[Y_{pd}\right] = j\mathrm{Im}\left[Y_{nd}\right] + j\omega_0 C_{pic} + \frac{1}{Z_{\mathrm{instubd}}} = 0 \tag{19}$$

$$j\mathrm{Im}\left[Y_{pg}\right] = j\mathrm{Im}\left[Y_{gin}\right] + j\omega_0 C_{pic} + \frac{1}{Z_{\mathrm{instubg}}} = 0 \tag{20}$$

Equations (19) and (20) can provide the values of Z_{instubd} and Z_{instubg}, thus allowing the design of the two stubs. As a consequence of Eqs. (19) and (20), the admittances Y_{pd}, Y_{pg} are real and become:

$$Y_{pd} = \mathrm{Re}\left[Y_{nd}\right] + G_{ic} \tag{21}$$

$$Y_{pg} = \mathrm{Re}\left[Y_{gin}\right] + G_{ic} \tag{22}$$

Let's introduce parameters B, D, ψ:

$$B = Z_0 N Y_{pg} \tag{23}$$

$$D = \sqrt{\left[NY_{pd} + (2+B)\,Y_o\right]^2 + NY_{pd}B\left[(2+B)\,(NY_{pd}+2Y_o)\right]\sin\phi^2} \tag{24}$$

$$\psi = \text{arctg}\left[\text{tg}\phi\frac{(1+B)\,(NY_{pd}+Y_o)+Y_o}{NY_{pd}+(2+B)\,Y_o}\right] \tag{25}$$

so that the oscillation condition (18) can be written as:

$$1 = \frac{-Ng_m\,|P_4|\,e^{j\psi_4}}{De^{j\psi}\,|P_2|\,e^{j\psi_2}\cos\theta_d} \tag{26}$$

which gives:

$$\psi = -\psi_2 + \psi_4 + \pi \tag{27}$$

and

$$g_m = \frac{D\,|P_2|\cos\theta_d}{N\,|P_4|} \tag{28}$$

According to Eq. (25), the unknown ϕ is related to the phase ψ as follows:

$$\phi = \text{arctg}\left[\text{tg}\psi\frac{NY_{pd}+(2+B)\,Y_o}{(1+B)\,(NY_{pd}+Y_o)+Y_o}\right] \tag{29}$$

The phase ϕ must be inserted in Eq. (24) for obtaining D, which in turn can be utilized in Eq. (28) for computing g_m.

In conclusion, the design steps of the distributed oscillator can be briefly summarized as follows:

Step1: The interdigital capacitor is designed by means of an electromagnetic simulator, imposing f_0 as resonance frequency. Hence, the values of the capacitance C_{pic} and of the conductance G_{ic} are also calculated.

Step2: The two transmission lines used for connecting the transistor to the passive elements of the unit cells are synthesized, choosing the electric lengths θ_d and θ_g in such a way to avoid unwanted coupling effects between the gate and drain lines.

Step3: The bias point in the characteristic curves of the transistor is selected. As a consequence of this choice, the values of L_d, L_g, C_d, C_g, R_d, and R_g are obtained.

Step4: The two stubs are designed by using the values of Z_{instubd} and Z_{instubg} provided by Eqs. (19) and (20).

Step5: The electric length ϕ is utilized for computing the geometric length of the feedback transmission line.

6. CONSIDERATIONS ON THE POWER OF THE OUTPUT SIGNALS

The distributed oscillator shown in Fig. 1 has two output ports, hence it provides two sinusoidal signals. The linear model presented in this paper does not allow to calculate the powers of these signals, respectively P_g and P_d. However, it yields an analytic formula for the ratio of these two powers, which is related to the difference between their values in dBm, $P_{g\text{dBm}}$ and $P_{d\text{dBm}}$. The expressions of $P_{g\text{dBm}}$ and $P_{d\text{dBm}}$ can be written as:

$$P_{g\text{dBm}} = 10\log P_g = 10\log\frac{|V_g|^2}{2Z_0 10^{-3}} \tag{30}$$

$$P_{d\text{dBm}} = 10\log P_d = 10\log\frac{|V_d|^2}{2Z_0 10^{-3}} \tag{31}$$

Thus we have for the difference of the output powers ΔP_{dBm}:

$$\Delta P_{\text{dBm}} = P_{d\text{dBm}} - P_{g\text{dBm}} = 10\log\frac{|V_d|^2}{|V_g|^2} \tag{32}$$

According to Eq. (13), we find:

$$\left|\frac{V_d}{V_g}\right|^2 = 1 + \sin\phi^2\,(2+B)\,B \tag{33}$$

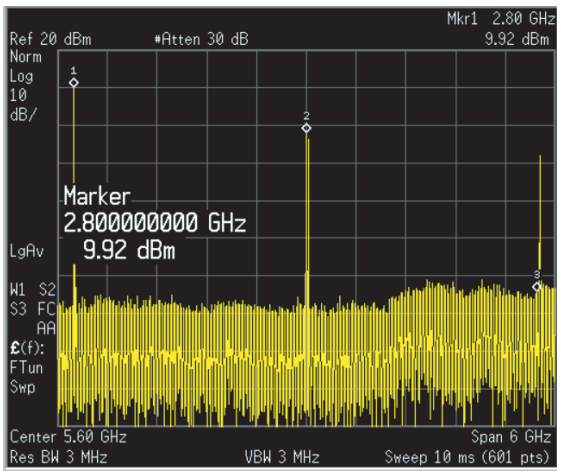
From Eqs. (32) and (33), we obtain for ΔP_{dBm}:

$$\Delta P_{\mathrm{dBm}} = 10\log\frac{|V_d|^2}{|V_g|^2} = 10\log\left[1 + \sin\phi^2\,(2+B)\,B\right] \tag{34}$$

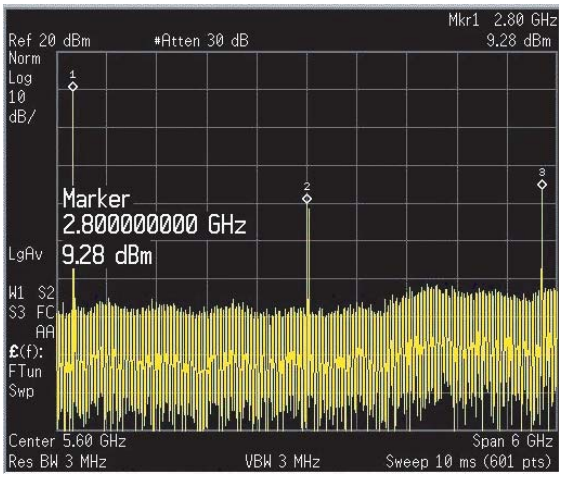
7. COMPARISON WITH EXPERIMENTAL RESULTS

The numerical results obtained by using the proposed linear approach have been compared to the experimental results presented in [22]. The values of its equivalent circuit elements are listed in Table 1. In particular, L_d, L_g, C_d, C_g, and R_g have been obtained in [23], whereas R_d is as usual computed as the inverse of the slope of the current-voltage characteristics (I_d-V_d) at the operating point. In Table 1, the values of C_{pic} and G_{ic} are also reported, both achieved by the electromagnetic simulation of the interdigital capacitor. For this purpose, the Momentum simulator implemented in the Advanced Design System (ADS) — Keysight software package has been utilized. Moreover, in Table 1 the values of characteristic impedances Z_d, Z_g and the values of electrical lengths θ_d and θ_g are given. For this oscillator, the measured frequency spectra at the drain and gate line outputs are presented in Fig. 10 [22]. Using these experimental results, $\Delta P_{\mathrm{dBm}} = 0.64\,\mathrm{dBm}$ is obtained. In Table 2, the values for ΔP_{dBm} and ϕ (evaluated at the oscillation frequency $f_0 = 2.8\,\mathrm{GHz}$) are computed by using the formulas developed in this paper, in comparison with the results provided by the simplified analysis [21] and with the experimental values measured for the realized circuit [22]. From Table 2, the following considerations can be inferred:

- The length of the feedback line for the manufactured oscillator is smaller than the value predicted in [21]. The proposed approach yields an electric length quite close to the value of the realized circuit.
- By using the simplified analysis in [21], the same power is expected for the two output signals. However, the measured values are not equal. This difference is mostly accounted in the described model. It is worth adding that in the model the losses in the feedback line and the stubs are not included. This approximation can explain the existing small discrepancy in Table 2.



(a)



(b)

Figure 10. Measured frequency spectra at the two outputs of the oscillator: (a) drain line output and (b) gate line output.

Table 1.

Parameters	Values
L_d (nH)	1
L_g (nH)	0.45
C_d (pF)	0.16
C_g (pF)	0.43
R_d (Ω)	250
R_g (Ω)	18
C_{pic} (pF)	0.64
G_{ic} (Ω^{-1})	$0.733 \cdot 10^{-3}$
Z_d (Ω)	107
Z_g (Ω)	107
θ_d ($^\circ$)	18.6
θ_g ($^\circ$)	6.2

Table 2.

Parameters	ϕ (deg.)	ΔP_{dBm}
Simplified analysis [21]	180°	0
Realized Circuit [22]	138°	0.64
This work	158°	0.41

8. CONCLUSION

A linear model for the CRLH distributed oscillator has been proposed. An analytic expression for the oscillation condition has been obtained. The model includes most of the losses present in the structure. Moreover, it provides a general design procedure for this kind of circuit. A comparison with experimental results for a previously realized oscillator confirms the validity of the presented approach.

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