

An Improved Calculation Method for Static Capacitance in Inductor Windings

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Abstract—This paper proposes an improved method for calculating static capacitance between two conductors with circular cross-sections in inductor windings. It considers the effects of electric field coupling and energy distribution on static capacitance. In this paper, the capacitance between two conductors in inductor windings is calculated by the improved calculation method and finite-element method (FEM), respectively. The relative error of the improved calculation method is between 0.11% and 4.51% compared to the FEM. In order to verify the effectiveness of this method for inductor winding, the orthogonal stacking winding and staggered stacking winding are chosen as calculation examples to accurately predict the static capacitance of multi-layer circular-section induction coils. Finite element models for the two types of windings are built to determine the capacitances for our 3×3 array arrangement winding. The results show that the improved calculation method proposed in this paper highly conforms to FEM. Finally, we adopt an air-cored cylindrical inductor winding for experimental verification, and the improved calculation method is proved to be correct.

1. INTRODUCTION

The frequency and power density of power devices are improving with the rapid development of power electronics technology [1]. Inductor, as one of the key components in power electronics system, has important applications in electric vehicles [2], DC power transmission [3], pulse power application [4], electromagnetic detection measurement [5, 6], etc. The capacitance in high-frequency windings significantly impacts the performance of power electronics system [7]. The electrical energy of the parasitic capacitance between windings can cause transient voltage peaks, which may affect the performance of the electric equipment seriously [8–10], thus reducing their efficiency [11]. Moreover, parasitic capacitance and leakage inductance are likely to induce circuit resonance, resulting in malfunction of electrical equipment. Consequently, it is important to calculate and analyze the capacitance of high-frequency inductor windings.

The values of parasitic capacitance of magnetic devices (inductor or transformer) may be obtained by performing experimental measurements on a specific device [12]. Reference [13] proposes a new imaging algorithm of permittivity for Electrical Capacitance Tomography (ECT), and it provides a new way to determine capacitance. Since experimental measurements are time and material consuming to optimize a project, they can barely acquire the specific parameters inside a component. In addition, analytical methods [14, 15] and numerical calculations [16] are also available for calculation of parasitic capacitance. However, considering that numerical calculation has been proven computationally intensive and time-consuming, analytical methods are considered as a favorable method for acquiring parasitic

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capacitance. Reference [17] summarizes some analytical calculation methods of static capacitance, which can be divided into the following three categories according to the different integral paths: the radial path [18], the shortest path [19], and the parabolic path [20].

The insulation layer thicknesses of inductor windings indicate different insulation layer static capacitances. In addition, the calculated values in [18] and [19] differ significantly from the actual values, resulting from the curved actual electric field line. The calculation of static capacitance emphasizes the definition of the path between two conductors. Reference [20] provides a calculation method of static capacitance, but it barely considers the coupling of electric field and energy distribution of winding. Based on the shortest integral path, [17] explores the impact of relative position between winding turns on their electric field under two stacking methods. The different winding arrangement changes the winding potential which results in disparities in the air capacitance of different stacking modes [21]. Given the actual energy distribution shape between conductors, the hyperbolic trajectory of the energy density in the air is defined as an integral path to calculate the total elementary capacitance in this paper.

This paper is organized as follows. Section 2 analyzes the integral path of static capacitance and proposes the analytical models for the capacitance between conductors. Section 3 calculates the capacitances between conductors in different specifications and verifies the accuracy of the calculation method. Besides, the section analyzes the effect of the geometry parameters of the winding on the static capacitance and draws a conclusion that the static capacitances of orthogonal and staggered stacked windings are different due to different integral angles. Section 4 verifies the accuracy of the hyperbolic integral path for the inductor winding.

2. ANALYSIS OF STATIC CAPACITANCE INTEGRAL PATH BETWEEN CONDUCTORS

Assuming that the surface of conductor is equipotential, the capacitance of two conductors may be calculated by Equation (1). The integral path defines the distance of the capacitor plates, as shown in Figure 1(a), and the capacitance may be determined by an elementary unit of area, as shown in Figure 1(b). References [18, 20] show that the total capacitance of the windings is composed of two insulator capacitors C_{ins} and one air capacitor C_{air} in series, as shown in Equation (2). By Equation (3), the elementary capacitance is obtained. The distance for the integral path is crucial for air capacitor C_{air} .

$$C = \varepsilon_r \varepsilon_0 \frac{A}{x(\theta)} \quad (1)$$

$$C_{tt} = \frac{1}{2 \frac{1}{C_{air}} + \frac{1}{C_{ins}}} \quad (2)$$

$$dC = \frac{\varepsilon_r \varepsilon_0 r}{x(\theta)} d\theta dl \quad (3)$$

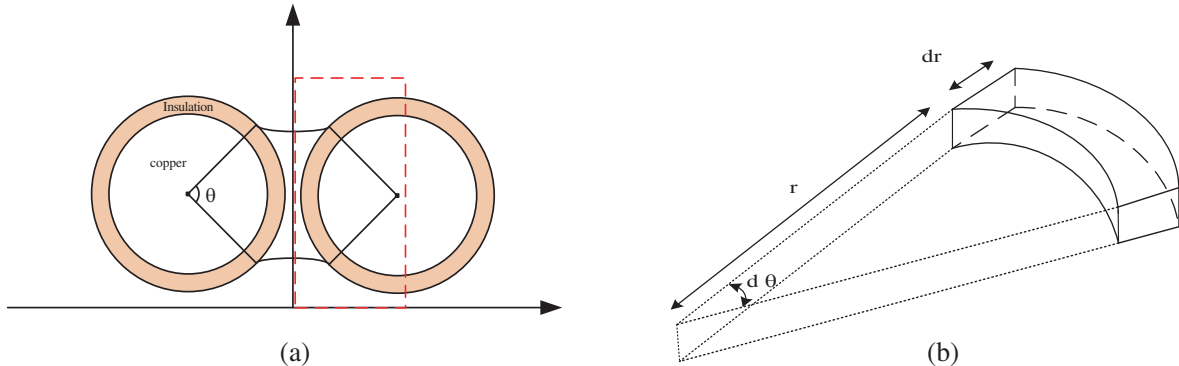


Figure 1. Elementary cylindrical surface located inside the insulating coating.

2.1. Analysis of Integral Path

The first step is to determine the relative distance $x(\theta)$, thereby calculating the air capacitor C_{air} between conductors. Several calculation models are proposed in [18–20], respectively. The electric field lines in the air defined in [18] are shown in Figure 2(a), where the lines are radial. The electric field lines follow the shortest distance between the two conductors in [19], which is shown in Figure 2(b). Besides, Figure 2(c) demonstrates a circular path in [20].

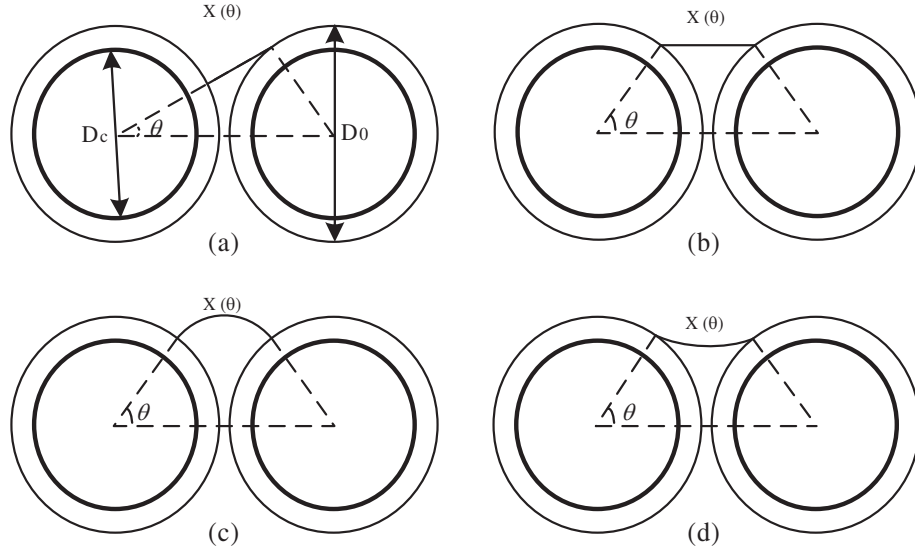


Figure 2. Proposed path of electric field lines between two circular cross section conductors. (a) Dalessandro et al. [18]. (b) Massarini and Kazimierczuk [19]. (c) Liu et al. [20].

Since the different emphases, three models from [18–20] are diverse fundamentally from each other. The model in Figure 2(a) is considered more suitable for the large winding resistance and the imbalance of charge distribution between two adjacent turns. A conservatively estimated path is shown in Figure 2(b), and the charge is concentrated around the near points of the two conductors when θ is small, and the integral path is approximately a straight line. The elementary capacitance of air is obtained by Equation (4), and the error in this model also increases following θ . In order to solve the problems above, the circular integral path shown in Figure 2(c) is obtained by optimizing Figure 2(b), and the elementary capacitance of air is then obtained by Equation (5). And Chagas and Marchesan [17] proposed a parabolic integral path to obtain Equation (6).

$$dC_{air-b} = \epsilon_0 \cdot \frac{1}{2 \cdot (1 - \cos(\theta))} \cdot d\theta \tag{4}$$

$$dC_{air-c} = \epsilon_0 \cdot \frac{1}{2 \cdot \theta \cdot \tan \frac{\theta}{2}} \cdot d\theta \tag{5}$$

$$y = \frac{x^2 \cdot \left(\frac{D_c}{2} - \frac{D_0}{2} \right) \cdot \sin \theta}{\left(\frac{D_0}{2} - \frac{D_c}{2} \cdot \cos \theta \right)^2} + \frac{D_0}{2} \cdot \sin \theta \tag{6}$$

For the improvement of the calculation accuracy of static capacitance, we study the energy distribution between two conductors with circular cross-sections through finite element simulation, as shown in Figure 3. When angle θ is small, the charge distribution density in Figure 3(a) has higher electric field energy in region I. The hyperbolic structure in Figure 2(d) may be observed via the change of energy depth. With the increase of θ , the conductor charges and energy density decrease accordingly,

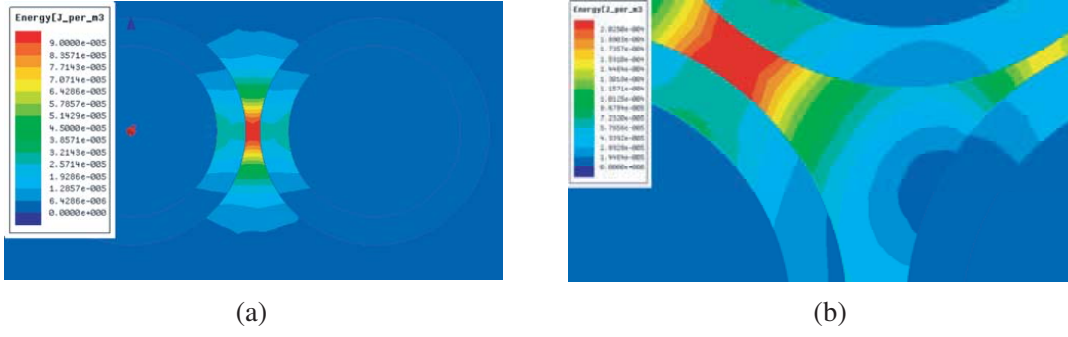


Figure 3. Energy distribution between two turns of circular section; (a) FEM simulation of two conductors and (b) FEM simulation of windings.

as shown in region II. The outside of the cloud image in Figure 3(a) is similar to the circular trajectory model in Figure 2(c). However, if applying the energy distribution curve in the outer layer as the integral path of capacitance calculation, the results would be higher than the actual value since the energy distribution in the outer layer is now at its weakest level. At the same time, the electric field coupling, as shown in Figure 3(b), will occur in the actual winding scenario, and the model in Figure 2(c) is not accurate. As we can notice from Figure 3(b), the electric field energy tends to concentrate towards the center, considering the coupling of the electric field. In summary, the hyperbolic integration path model that the paper proposes refers to Figure 2(d).

For simplifying the analysis, we analyze the symmetrical structure of Figure 1(a) inside the red dotted wireframe, enlarging it to get Figure 4, which presents the coordinates of the capacitive integration path. Further, x_1 and y_1 may be expressed by Equations (7) and (8), respectively. The vertex may be defined by $(0, y_0)$, where the expression of y_0 is shown in Equation (10), and the variable “ p ” may be defined by Equation (9), considering that the point (x_2, y_1) is known based on Equation (11). The function “ y ” that describes the integral path is defined by the combination of Equations (7)–(11), thus Equation (12) is obtained.

$$x_1 = \frac{D_0}{2} (1 - \cos \alpha) \quad (7)$$

$$y_1 = \frac{D_0}{2} \cdot \sin \alpha \quad (8)$$

$$x^2 = 2p (y - y_0) \quad (9)$$

$$y_0 = \sin \alpha \cdot \left(\frac{D_c}{3} + \frac{D_0}{6} \right) \quad (10)$$

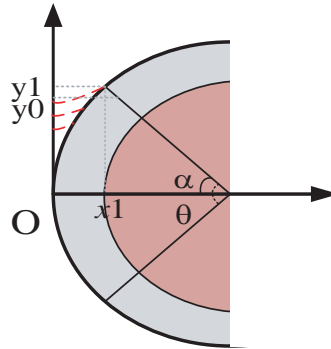


Figure 4. Coordinates used to define the path of the field lines.

$$p = \frac{3 \cdot D_0^2 \cdot (1 - \cos \alpha)^2}{8 \cdot (D_0 - D_c) \cdot \sin \alpha} \tag{11}$$

$$y = \frac{4 \cdot x^2 \cdot \sin \alpha (D_0 - D_c)}{3 \cdot D_0^2 (1 - \cos \alpha)^2} + \frac{D_c}{2} \cdot \sin \alpha \tag{12}$$

The length of the integral path $x(\theta)$ may be calculated by Equation (13). Thus, the proposed calculation of the elementary capacitance of air may be conducted by Equation (14).

$$x(\theta) = \int_{-x_1}^{x_1} \sqrt{1 + \left(\frac{dy}{dx}\right)^2} dx \tag{13}$$

$$dC_{\text{air}} = \frac{\varepsilon_0 \cdot \frac{D_0}{2}}{x(\theta)} d\theta = \frac{\varepsilon_0 \cdot \frac{D_0}{2}}{\int_{-x_1}^{x_1} \sqrt{1 + \left(\frac{4x \cdot \sin \alpha \cdot (D_0 - D_c)}{D_0^2 (1 - \cos \alpha)^2}\right)^2} dx} d\theta \tag{14}$$

2.2. Analysis of Insulation Capacitance Integral Path

Dalessandro et al. considered that the elementary capacitance of the insulating layer is calculated based on the cylindrical capacitor [18–20], where the copper conductor indicates one plate, and the insulating layer indicates the other plate of the capacitor. Figure 5 demonstrates the distribution of electric field lines obtained by finite element simulation, in which the electric field lines in the insulating layer are evenly distributed and perpendicular to both sides.

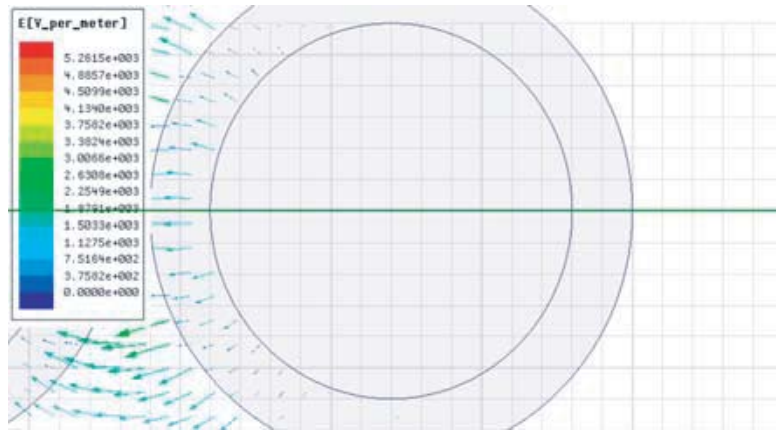


Figure 5. Analysis of insulation capacitance C_{ins} integral path.

Hence the unit capacitance may be expressed by Equation (15), and the capacitance of the insulation layer is related to θ , as shown in Equation (16). The charges distribute on the adjacent side of the two conductors due to the electric field force between conductors. Therefore, the size of the integral angle θ should be adjusted according to the actual stack, and l is the length of the conductor in Equation (16).

$$dC_{ins} = \frac{\varepsilon_r \varepsilon_0 r d\theta dh}{dr} \tag{15}$$

$$dC_{ins} = \varepsilon_r \varepsilon_0 d\theta \int_0^l dh \int_{r_c}^{r_0} \frac{r}{dr} = \frac{\varepsilon_r \varepsilon_0 l}{\ln \frac{r_0}{r_c}} d\theta \tag{16}$$

2.3. Turn-to-Turn Capacitance

The Turn-to-turn capacitance C_{tt} may be calculated by Equations (4), (14), and (16), resulting in Equation (17). The total static capacitance Equation (18) may then be obtained by integrating Equation (17)

$$dC_{eq} = \frac{dC_{air} \cdot dC_{ins}}{2dC_{air} + dC_{ins}} \quad (17)$$

$$C_{tt} = \int_{\theta_1}^{\theta_2} dC_{eq} d\theta \quad (18)$$

Substituting Equations (4) and (16) into Equation (18), the static capacitance expression calculated based on the shortest path model [17] is obtained, as shown in Equation (19).

$$C_{tt-b} = \frac{\varepsilon_0}{2} \cdot \int_{\theta_1}^{\theta_2} \frac{1}{1 + \frac{1}{\varepsilon_r} \cdot \ln\left(\frac{D_0}{D_c}\right) - \cos\theta} \cdot d\theta \quad (19)$$

Substituting Equations (5) and (16) into Equation (18), the static capacitance C_{tt-c} , is obtained, which is calculated by the circular integral path [19], as shown in Equation (20).

$$C_{tt-c} = \int_{\theta_1}^{\theta_2} \frac{\varepsilon_0^2 \varepsilon_r}{\ln\frac{D_0}{D_c} + \theta \cdot \tan\frac{\theta}{2} \cdot \varepsilon_r} d\theta \quad (20)$$

By substituting Equations (14) and (16) into Equations (17) and (18), Equation (21) is obtained for calculating C_{tt} using the proposed method of this paper.

$$C_{tt} = 2 \int_{\theta_1}^{\theta_2} \frac{1}{\frac{1}{\varepsilon_0 \cdot \frac{D_0}{2} \cdot \int_{-x_1}^{x_1} \sqrt{1 + \left(\frac{4x \sin\theta (D_0 - D_c)}{D_0^2 (1 - \cos\theta)}\right)^2} dx} + \frac{2 \ln \frac{r_0}{r_c}}{\varepsilon_r \varepsilon_0 l}} d\theta \quad (21)$$

3. SIMULATION VERIFICATION

To validate the theoretical calculation method proposed in the previous section, the simulation model is built and shown in Figure 6. Otherwise, it can be seen from Equations (19), (20), and (21) that the static capacitance is correlated with the ratio of insulation thickness to copper diameter. Therefore, when conducting simulations and calculations on the capacitance between conductors with different diameters, the value k ranges from 0.01 to 0.1, where k represents the ratio of the thickness of insulating paint to the radius of the copper core by Equation (22). The diameter of copper wire D_c in this section is set as 2 mm. Generally, 20 simulations and 60 numerical calculations are applied in our work.

$$k = \frac{D_0 - D_c}{D_c} \quad (22)$$

The limits of the integral stake of Equation (21) may be set as $-90^\circ \sim 90^\circ$. This section aims to calculate the capacitance between conductors using the path shown in Figures 2(b) and (c) and the path we suggested, and the results are shown in Table 1.

Figure 7 presents the comparison of the error presented by the existing methods in [19, 20] with the FEM simulation result. The method proposed presents a low error in the research scope.

In order to testify the feasibility of the improved method in practical engineering applications, the static capacitance of the wire AWG10–AWG41 has been simulated and calculated for 32 times in this paper, and the calculation errors are shown in Figure 8. Although the partial error marked in the red box is at a higher level, it is yet better than the result in Figure 2(b). At the same time, an approximately linear relationship among the error, diameter ratio k , and AWG may be observed. The

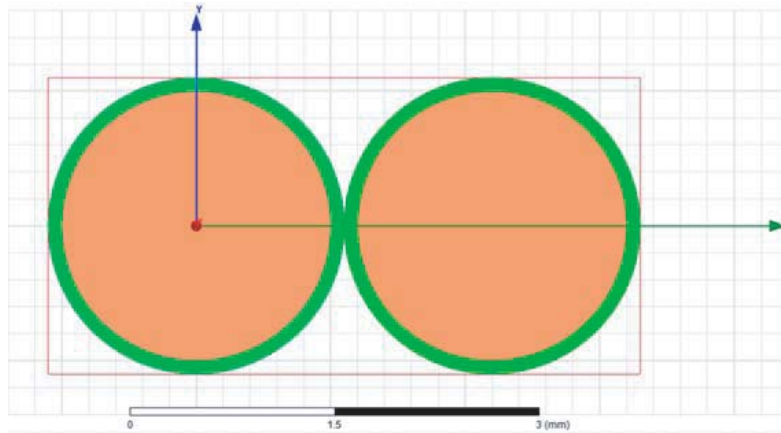


Figure 6. Two-conductor simulation model.

Table 1. Capacitive value between two conductor systems.

k	C_{FEM}/pF	C_b/pF	C_c/pF	$C_{proposed}/\text{pF}$
0.01	338.79	359.62	355.52	353.54
0.015	277.65	292.28	288.26	285.27
0.02	240.29	252.18	248.23	244.49
0.025	214.46	224.84	220.94	216.63
0.03	195.25	204.68	200.85	196.06
0.035	180.25	189.02	185.24	180.06
0.04	168.13	176.42	172.69	167.17
0.045	158.08	165.98	162.3	156.5
0.05	149.56	157.17	153.53	147.47
0.055	142.23	149.59	145.99	139.72
0.06	135.84	142.98	139.43	132.96
0.065	130.21	137.16	133.65	127
0.07	125.19	131.98	128.51	121.7
0.075	120.68	127.34	123.89	116.95
0.08	116.61	123.13	119.73	112.65
0.085	112.91	119.31	115.94	108.75
0.09	109.53	115.82	112.47	105.19
0.095	106.42	112.6	109.29	101.91
0.1	103.56	109.64	106.35	98.89

image results show that although the calculation error increases significantly when the wire diameter is less than 0.1 mm, the whole error rate of the proposed method is low and applies to most standard types of conductors, thus it has higher accuracy in calculating static capacitances.

The static capacitance calculation method may be extended to the total capacitance dimension of multi-layer inductor winding combining all C_{tt-t} and C_{tt-l} . The method for the total capacitance of different winding types is obtained, considering additionally the geometrical parameters of winding [21]. According to the energy conservation principle [21, 22], the entire multi-layer winding total capacitance

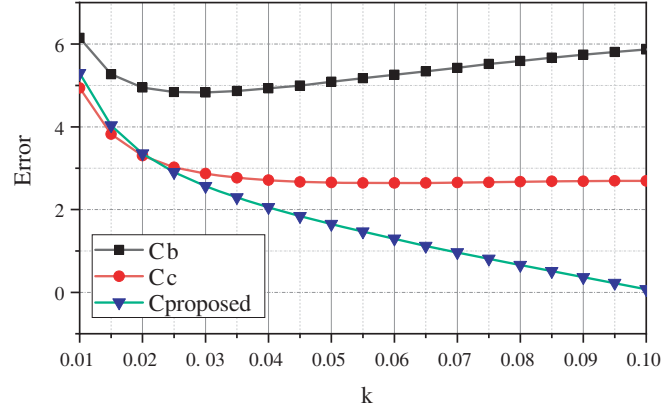


Figure 7. Comparison of different calculation methods.

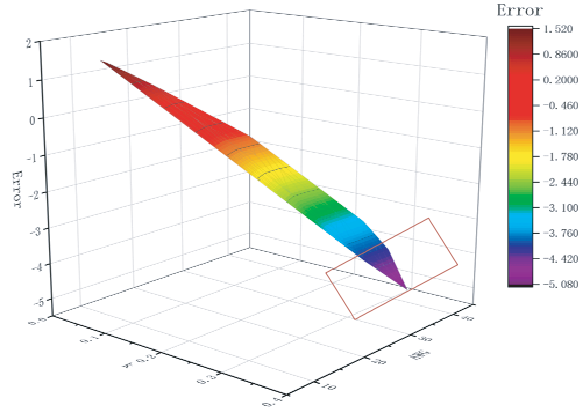


Figure 8. Error comparison of standard wire AWG10–AWG41.

would be:

$$C = \frac{1}{N^2} \left[(N_m - 1) N_l C_{tt-t} + \sum_{i=1}^{N_m} (2i - 1)^2 (N_l - 1) C_{tt-l} \right] \quad (23)$$

where N_m indicates the number of turns per layer, while N_l indicates the number of layers.

The paper focuses mainly on two types of stacking methods as orthogonal stacking and staggered stacking. The positions of the wires in the two stacking schemes tend to cause different types of capacitances between adjacent conductors, as shown in Table 2. The assembly method for the circular cross-sections is shown in Figure 9. The orthogonal/staggered stack arrangement of the three-layer winding is shown in Figures 9(a) and (c), respectively. Figures 9(a) and (c) are the enlarged diagram of the winding structure in the red box of Figures 9(b) and (d), respectively. Given the difference between the electric field distribution of the edge conductor and the inner conductor, their integral angles are correspondingly various, as shown in Table 2. The integral angles are determined by the inter-turn geometry inside the winding.

Due to the large calculation amount we list merely the main capacitance values of AWG10 and AWG19 when the wires are stacked. To verify the applicability of the capacitance calculation method suggested in practical engineering applications, we choose calculation and simulation of C_{24} in orthogonal stacking and C_{12} in staggered stacking, as shown in Table 3.

The position of the winding array of staggered stacks is different from that of the orthogonal stack in Figure 9(c), and there are four different types of capacitances under the staggered stack. A 3×3 staggered stacked conductor winding is proposed in this paper, and the capacitance in the staggered

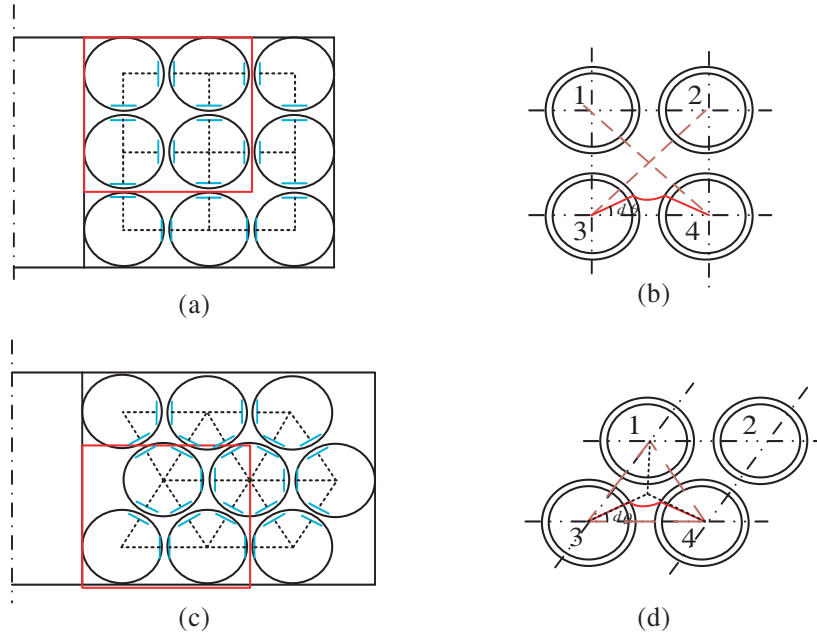


Figure 9. Two types of stacking. (a) Orthogonal Stacking. (b) Capacitances considered of (a). (c) Staggered Stacking. (d) Capacitances considered of (c).

Table 2. Capacitance type and integration angle.

Stacking	Capacitance	θ_1	θ_2
Orthogonal	C_{12}	-45°	90°
	C_{13}	-90°	45°
	C_{24}	-45°	45°
	C_{34}	-90°	45°
Staggered	C_{12}	-30°	30°
	C_{13}	-60°	30°
	C_{14}	-90°	-30°
	C_{34}	-90°	30°

Table 3. The capacitance of two stacking scheme.

	Orthogonal Stacking				Staggered Stacking			
	C_{FEM}/pF	C_b/pF	C_c/pF	$C_{proposed}/\text{pF}$	C_{FEM}/pF	C_b/pF	C_c/pF	$C_{proposed}/\text{pF}$
AWG10	96	104	102	98	76.6	99	97	93
AWG19	141	144.5	142.5	139.5	131	139	137	134

stack scheme may be calculated by the main capacitance C_{12} , C_{13} , and C_{34} . The comparison results of the main capacitance value C_{12} are shown in Table 3, although there are some differences between the calculation and simulation results, and the error of the proposed method is lower than the methods in [19, 20].

Based on different stacking schemes, we verify the accuracy of the calculation method in two stacking schemes where their calculation accuracy is optimized to some extent, and the results of the

staggered stack are better than those of orthogonal stack. The total capacitance of the multilayer induction winding is calculated by substituting C_{tt-t} and C_{tt-l} into Equation (23), and the specific calculation process will not be derived in detail in this paper.

4. EXPERIMENTAL VALIDATION

The performance of the method proposed is evaluated by comparing the measured and calculated values of the capacitance of actual induction windings. From the previous research and the calculation results in Section 3, the capacitance calculation method has been proven to be accurate for the stack of winding [20, 21]. For the achievement of a better experimental effect, orthogonal stacking is selected for calculation verification in this paper. The unit capacitances of the winding are connected in parallel, and the principle of calculating C_{tt-t} and C_{tt-l} is the same as Equation (21). We prepare a single layer induction winding to simplify the calculation. In this case, we choose AWG26 as the wire type. The winding skeleton adopts PQ26/20 standard element, and the test equipment is shown in Figure 10. Figure 10(a) presents the top view of the equipment under test (EUT), and the inductance winding skeleton diameter parameters d_1 and d_2 are 14.3 mm and 21.6 mm, respectively. The profile of the inductor winding along the YOZ plane refers to Figure 10(b). The wire diameter is $d_3 = 0.46$ mm, and the number of turns is $n = 15$.

WAYNE KERR 6500B precision impedance analyzer is used to measure the self-capacitance of the winding. A network of lumped capacitors obtained for a coreless single-layer coil is shown in Figure 11. In this case, the total stray capacitance of the coil is given by the equivalent capacitance of the turn-to-turn capacitances in series by Equation (25).

The turn length is $Lt = \pi \times Dt = 44.925$ mm. The dielectric constant of the coating material used for the nonimpregnated winding is $\varepsilon_r = 3.5$. Using Equation (21), we can get the inter-turn capacitance

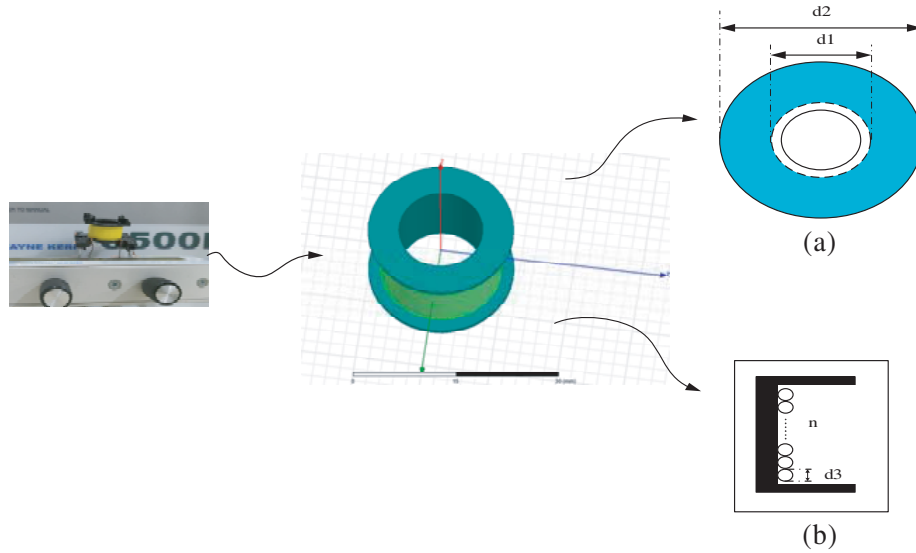


Figure 10. Component test diagram. (a) The top view of EUT. (b) The profile of EUT.

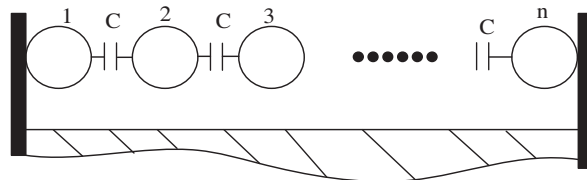


Figure 11. Lumped capacitor network for a single-layer coil.

$C_{tt-l} = 82.46$ pF of a unit length wire, whereas the static capacitance may be obtained by Equation (24). The inductor winding customized by us has 15 turns, thus the static capacitance of the winding may be calculated by Equation (25), where n is the turn number of the winding, $C_s = 0.265$ pF.

$$C_{tt} = L_t \cdot C_{tt-l} \quad (24)$$

$$C_s = \frac{C_{tt}}{n-1} \quad (25)$$

The inductive prototype is measured with an impedance analyzer, in which the inductive value is $L = 6.7\mu\text{H}$, and the resonant frequency is 115 MHz. Thus, the size of the static capacitance may be calculated according to Equation (26), which gives a result of 0.28 pF. The error rate of the model calculation is 5.35%.

$$f = \frac{1}{2\pi\sqrt{L \cdot C}} \quad (26)$$

Based on the analysis above, the calculation results of the hyperbolic integration model in this paper are in line with the experimental results and provide a favorable reference for designers. In addition, the wire is affected by the skin collection and proximity effects in high frequencies, and the measurement results have been affected, as well.

5. CONCLUSION

This paper proposes an analytical method for obtaining the capacitance value between adjacent turns of circular cross-section conductors. The energy distribution and electric field coupling between adjacent conductors are analyzed by FEM, and an improved method for capacitance between adjacent turns integral path selection is proposed along with the premise of ignoring the effect of nonadjacent conductors, thereby improving the accuracy comparing to the existing methods. Also, the capacitance between adjacent conductors depends on the position of the conductor in the winding. Therefore, practical applications shall pay additional attention to the stacking types in the winding.

The method proposed considerably reduces the error between analytical calculated and FEM simulated values of parasitic capacitances compared to various existing methods. Based on the simulation and calculation in AWG10 and 19 wire stacks, the error of the specific calculation method is less than 2%, and its results agree well with the simulation. The experimental results show that the frequency response of the model corresponds to that of the prototype. Considering the resonant frequency, the calculation and test result error is not higher than 5%. In addition, along with the premise of the lumped parameter model, the calculation method is a good reflection of the dynamic characteristics of the parasitic capacitance and the inductor of the magnetic device.

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REFERENCES

1. Lateef, K. H. B., H. Hamad, and A. K. Ahmad, “New design and construction of high-voltage high-current pseudospark switch,” *IEEE Transactions on Plasma Science*, Vol. 43, No. 2, 625–628, 2015.
2. Bosshard, R. and J. W. Kolar, “Inductive power transfer for electric vehicle charging: Technical challenges and tradeoffs,” *IEEE Power Electronics Magazine*, Vol. 3, No. 3, 22–30, 2016.
3. Solas, E., G. Abad, J. A. Barrena, S. Aurtenetxea, A. Cárcar, and L. Zajac, “Modular multilevel converter with different submodule concepts — Part II: Experimental validation and comparison for HVDC application,” *IEEE Transactions on Industrial Electronics*, Vol. 60, No. 10, 4536–4545, 2013.

4. Aguglia, D., "Interconnected high-voltage pulsed-power converters system design for H-ion sources," *IEEE Transactions on Plasma Science*, Vol. 42, No. 10, 3070–3076, 2014.
5. Shadmand, M. B. and R. S. Balog, "Determination of parasitic parameters in a high frequency magnetic to improve the manufacturability, performance, and efficiency of a PV inverter," *38th IEEE Photovoltaic Specialists Conference*, 001368–001372, Austin, TX, USA, 2012.
6. Moorthy, V., "Important factors influencing the magnetic barkhausen noise profile," *IEEE Transactions on Magnetics*, Vol. 52, No. 4, 1–13, 2016.
7. Abetti, P. A., "Survey and classification of published data on the surge performance of transformers and rotating machines," *Transactions of the American Institute of Electrical Engineers. Part III: Power Apparatus and Systems*, Vol. 77, No. 3, 1403–1413, 1958.
8. López, Z. L., P. Gómez, F. P. Espino-Cortés, and R. Peña-Rivero, "Modeling of transformer windings for fast transient studies: Experimental validation and performance comparison," *IEEE Transactions on Power Delivery*, Vol. 32, No. 4, 1852–1860, 2017.
9. Liu, J. and V. Dinavahi, "Detailed magnetic equivalent circuit based realtime nonlinear power transformer model on FPGA for electromagnetic transient studies," *IEEE Transactions on Industrial Electronics*, Vol. 63, No. 2, 1191–1202, 2016.
10. Farhangi, B. and H. A. Toliyat, "Modeling and analyzing multiport isolation transformer capacitive components for onboard vehicular power conditioners," *IEEE Transactions on Industrial Electronics*, Vol. 62, No. 5, 3134–3142, 2015.
11. Wang, L., Q. Zhu, W. Yu, and A. Q. Huang, "A medium-voltage medium-frequency isolated dc-dc converter based on 15-kV SiC MOSFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. 5, No. 1, 100–109, 2017.
12. Liu, C., L. Qi, X. Cui, and X. Wei, "Experimental extraction of parasitic capacitances for high-frequency transformers," *IEEE Transactions on Power Electronics*, Vol. 32, No. 6, 4157–4167, 2017.
13. Pańczyk, M. and J. Sikora, "A new imaging algorithm for electric capacitance tomography," *Prace Instytutu Elektrotechniki*, Vol. LXIII, No. 274, 27–41, 2016.
14. Liu, X., Y. Wang, J. Zhu, Y. Guo, G. Lei, and C. Liu, "Calculation of capacitance in high-frequency transformer windings," *IEEE Transactions on Magnetics*, Vol. 52, No. 7, 1–4, 2016.
15. Massarini, A. and M. K. Kazimierczuk, "Self-capacitance of inductors," *IEEE Transactions on Power Electronics*, Vol. 12, No. 4, 671–676, 1997.
16. Liu, C., L. Qi, X. Cui, and X. Wei, "Experimental extraction of parasitic capacitances for high-frequency transformers," *IEEE Transactions on Power Electronics*, Vol. 32, No. 6, 4157–4167, 2017.
17. Chagas, N. B. and T. B. Marchesan, "Analytical calculation of static capacitance for high-frequency inductors and transformers," *IEEE Transactions on Power Electronics*, Vol. 34, No. 2, 1672–1682, 2019.
18. Dalessandro, L., F. D. S. Cavalcante, and J. W. Kolar, "Self-Capacitance of High-Voltage Transformers," *IEEE Transactions on Power Electronics*, Vol. 22, No. 5, 2081–2092, 2007.
19. Massarini, A. and M. K. Kazimierczuk, "Self-capacitance of inductors," *IEEE Transactions on Power Electronics*, Vol. 12, No. 4, 671–676, 1997.
20. Liu, X., Y. Wang, J. Zhu, Y. Guo, G. Lei, and C. Liu, "Calculation of capacitance in high-frequency transformer windings," *IEEE Transactions on Magnetics*, Vol. 52, No. 7, 1–4, 2016.
21. Wu, B., X. Zhang, X. Liu, and C. He, "An analytical model for predicting the self-capacitance of multi-layer circular-section induction coils," *IEEE Transactions on Magnetics*, Vol. 54, No. 5, 1–7, 2018.
22. RamRakhyani, A. K., S. Mirabbasi, and M. Chiao, "Design and optimization of resonance-based efficient wireless power delivery systems for biomedical implants," *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 5, No. 1, 48–63, 2011.