

A Tunable Diode-Based Reflective Analog Predistortion Linearizer for Microwave Power Amplifiers

Parsa Tahbazalli and Hossein Shamsi*

Abstract—Analog predistortion is an efficient method for improving the linearity of power amplifiers. This paper presents a simple and tunable analog predistortion linearizer with low insertion loss, capable of reducing the non-linearity effects of microwave power amplifiers. The linearizer employs Schottky diodes as a distortion generator and does not require any additional matching circuit. By controlling the DC bias of the diodes, various combinations of characteristics can be obtained; therefore, this structure can be used to match different device behaviors. Experimental validation using a $\varepsilon_r = 3.38$, 20-mil thick Rogers substrate at the center frequency of 2 GHz shows that the fabricated linearizer can provide up to 7.5 dB gain expansion. The fractional bandwidth and insertion loss of the linearizer are 10% and 1.7 dB, respectively. The simulated and measured results are in good agreement with each other. To illustrate an approach for compensating the limited phase characteristics of the presented structure, the design and simulation of a dual-branch linearizer utilizing the reflective Schottky diode predistortion linearizer as a nonlinear unit are also presented.

1. INTRODUCTION

With the rapid growth of communication systems, the need for high data rate transmission has become the essence. To achieve this goal in today's crowded spectrum, bandwidth-efficient modulation schemes such as QAM are employed [1]. These complex digital modulation schemes have non-constant envelopes with a high peak to average power ratio (PAPR). Therefore, they are susceptible to the nonlinearity of power amplifiers (PAs) and have to endure amplitude (AM/AM) and phase (AM/PM) distortions [2]. These distortions reduce the quality of the transmitted signal and generate adjacent channel interference (ACI) [2], hence reducing the ability to decode signals properly and also exceeding the acceptable limits of distortion and channel interference specified by various communication standards.

A trivial solution to reduce the effects of the distortions is that the amplifier operates at a lower output power level (backing off from the compression point). For instance, to meet the error vector magnitude (EVM) specifications for IEEE 802.11a at 54-Mb/s mode, operating at 8-dB back-off from the transmitter 1-dB compression point is required [3]. This approach results in a much lower power efficiency since PAs generally achieve higher power efficiency when operating closer to their maximum output power. PA architectures that provide high efficiency in back-off have been developed; Doherty PA is an example where the maximum efficiency occurs at 6 dB output-power back-off from the peak output power [4]. However, these techniques have their challenges and have not been widely used for microwave applications [1, 5].

Linearization is an alternate method used for reducing the nonlinearity effects of PAs, allowing us to have a higher level of power efficiency for a given level of distortion [5]. In this method, the nonlinearity of a power-efficient PA is compensated by additional circuits and signal processing, resulting in a linear and efficient system as a whole. Various PA linearization techniques can be classified mainly as

Received 16 February 2021, Accepted 2 April 2021, Scheduled 13 April 2021

* Corresponding author: Hossein Shamsi (shamsi@eetd.kntu.ac.ir).

The authors are with the Faculty of Electrical Engineering, K. N. Toosi University of Technology, Tehran, Iran.

feedforward [6, 7], feedback [8–11], and predistortion (PD) in both analog [12–21] and digital [22–25] domains. Using neural networks as a method to determine the necessary distortion to be added has also been reported in literatures [25–28]. Among these methods, analog PD linearizers show promise due to their simplicity, bandwidth, and ability to operate as an adjustable stand-alone unit. Fig. 1 illustrates the concept of the PD linearization technique. In this method, the linearizer creates a nonlinear transfer characteristic which is the reverse of the amplifier's transfer characteristics in both magnitude and phase [5]. By placing this block before the PA, the magnitude and phase linearities of the amplifier are both improved.

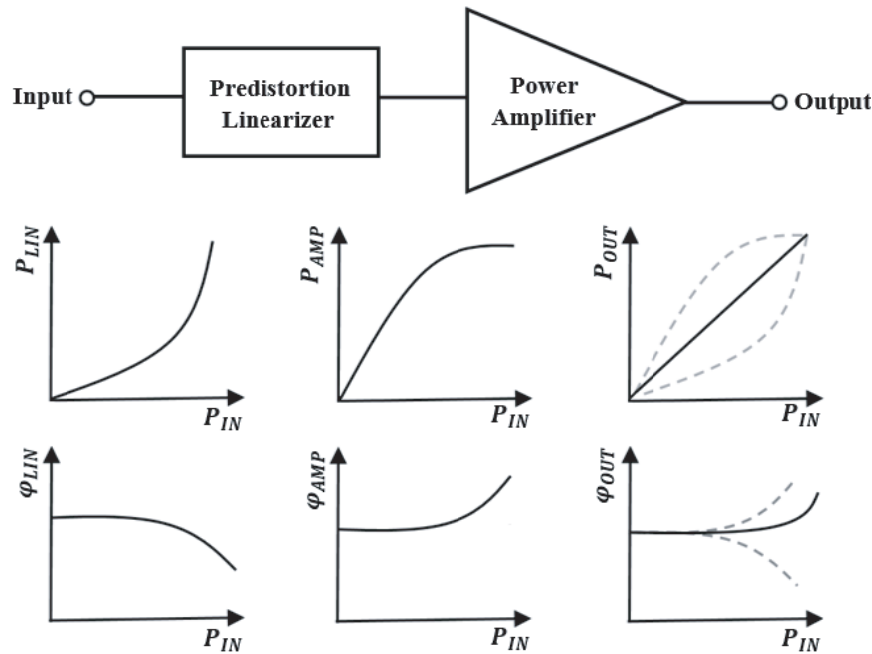


Figure 1. PD linearization concept.

Various analog PD linearizers have been developed. [12] investigates the nonlinearity of Schottky diode and presents a simple linearizer using Schottky diode. However, this linearizer is not suitable for PAs with high nonlinearity and also needs additional matching circuits. Reflective analog PD linearizers have been reported in literatures [13–17]. These structures have a trade-off among complexity, tuning capability, and insertion loss. Dual-branch topologies have gained a lot of attention [18–21]. The structure given in [18] utilizes Schottky and PIN diodes to realize an adjustable PD linearizer. In [19], an X-band dual-branch linearizer based on FET and Schottky diode has been presented. However, this linearizer is not very versatile. [20] presents a method to achieve independent tuning of gain and phase conversions using a similar architecture to [18]. In [21], another dual-branch architecture is presented where one branch consists of a nonlinearity generator followed by a vector multiplier while the other path is made of a delay line. This linearizer has some drawbacks; for instance, the vector multiplier can produce distortion if being driven into saturation. Despite having good tuning capability, dual-branch architectures have complex structures, relatively high insertion loss, and occupy a large area.

In this paper, a simple and tunable diode-based reflective analog PD linearizer with low insertion loss for microwave PAs is presented. The presented PD linearizer's characteristics can be easily adjusted by controlling the bias current of the diodes. Therefore, this structure can be used to correct different device behaviors. In Section 2, the behavior of Schottky diode's dynamic resistance over the change of input RF power is initially studied. In Section 3, the operation of the reflective Schottky diode PD linearizer used for compensating nonlinearity of PAs is investigated. In Section 4, simulation and measurement results are presented and compared, showing acceptable agreement between them. As an approach for compensating the limited phase characteristics of the presented structure, the design and simulation of a dual-branch PD linearizer utilizing the reflective Schottky diode PD linearizer as a

nonlinear unit is presented in Section 5. Finally, the paper is concluded in Section 6.

2. DYNAMIC RESISTANCE BEHAVIOR OF SCHOTTKY DIODE

Schottky diode is a semiconductor device formed by the junction of a semiconductor with a metal. Compared to a conventional p-n junction diode, Schottky diode has a relatively smaller junction capacitance, making it suitable for various RF applications [29] such as linearizers, phase shifters, and limiters [12–21, 30, 31]. The forward junction current of a Schottky diode is expressed as:

$$I_d(V_d) = I_s \left(e^{\frac{q}{\eta k T} V_d} - 1 \right) \quad (1)$$

where q is the electron charge, k the Boltzmann constant, η the ideality factor, T the temperature, I_s the reverse saturation current, and I_d and V_d denote the diode current and voltage, respectively. The RF equivalent circuit of a forward-biased Schottky diode is shown in Fig. 2(a) where R_d is the dynamic resistance, and C_d is the junction capacitance. The dynamic resistance R_d of the Schottky diode is derived from Equation (1) and given as follows [32].

$$R_d = \frac{1}{\frac{\partial I_d}{\partial V_d}} = \eta \frac{kT}{q} \frac{e^{-\frac{q}{\eta k T} V_d}}{I_s} \quad (2)$$

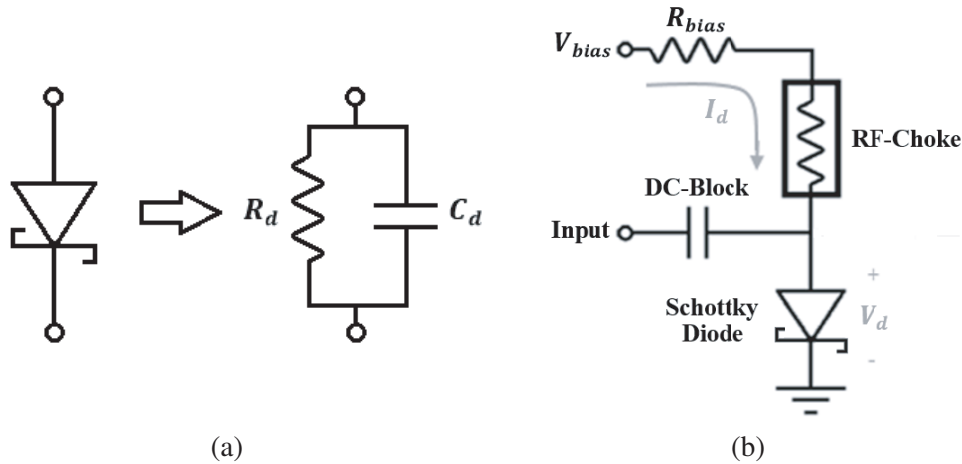


Figure 2. (a) RF equivalent circuit of forward biased Schottky diode. (b) Setup used for studying dynamic resistance behavior.

The setup shown in Fig. 2(b) is used to analyze the behavior of dynamic resistance R_d versus the RF input power variations. The average current through the bias resistor R_{bias} increases with an increase in the input power due to the clipping caused by the diode. Therefore, the DC bias operating point of the diode changes from small signal to large signal with increasing input power as shown in Fig. 3 [12]. Equation (3) indicates that with an increase in the diode current I_d , the voltage across the diode V_d decreases because of the voltage drop caused by the bias resistor R_{bias} .

$$V_d = V_{bias} - R_{bias} I_d \quad (3)$$

It can be concluded from Equations (2) and (3) that the diode dynamic resistance R_d increases as the input power level rises. This can also be interpreted from Fig. 3 since the slope of the tangent to the I-V curve is smaller at point L than point S . Fig. 4 shows the simulated R_d variation versus the change in input power in ADS using Spice parameters of MA4E2054 from MACOM at the operating frequency of 2 GHz to help understand the phenomenon discussed above. It should be noted that the parasitic components of the package were included in the simulation process. This nonlinear behavior would be used in the following section as the main principle in a reflective Schottky diode PD linearizer.

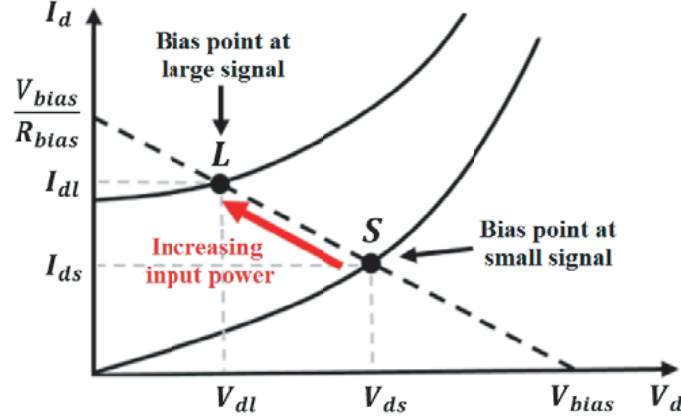


Figure 3. DC operating point movement of Schottky diode [12].

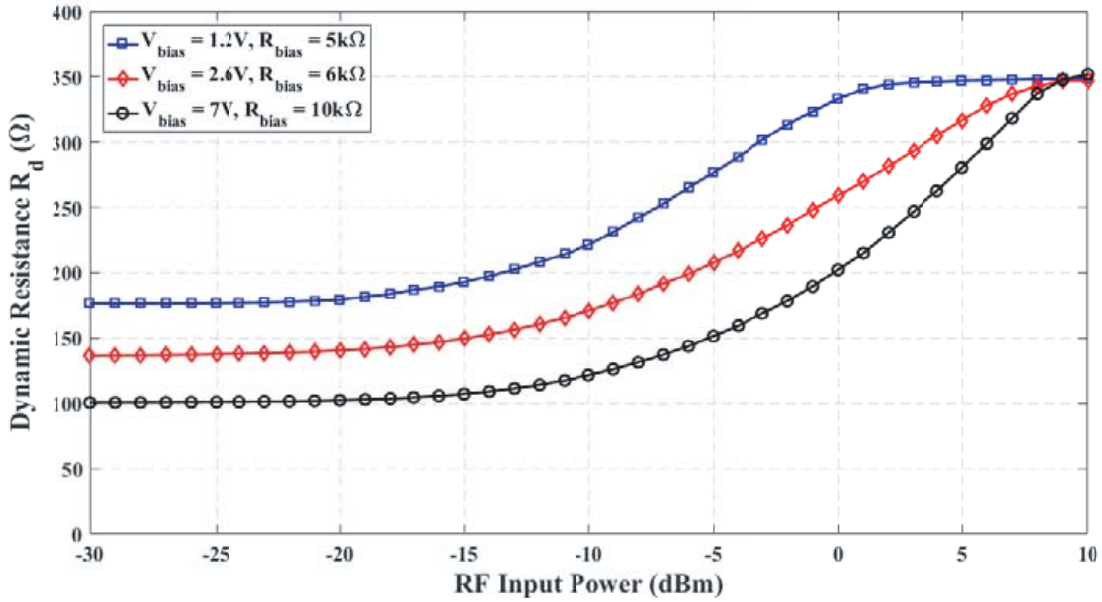


Figure 4. Simulated dynamic resistance versus input power for different bias conditions.

3. REFLECTIVE SCHOTTKY DIODE PREDISTORTION LINEARIZER

The schematic of a reflective Schottky diode PD linearizer is shown in Fig. 5. This structure consists of a hybrid coupler and two Schottky diodes. It is apparent from Fig. 5 that the presented linearizer would not need any additional matching circuit since input and output ports are matched to the characteristic impedance Z_0 of the coupler ($50\ \Omega$ in this case).

When the input signal is fed into port 1 of the hybrid coupler, divided signals go through the Schottky diodes attached at ports 2 and 3 and are then reflected and combined at the output port (port 4). In order to investigate the behavior of this PD linearizer, we use the scattering matrix of the hybrid coupler where a_i and b_i represent the incident and reflected waves at port i of the hybrid coupler, respectively.

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & 1 & j & 0 \\ 1 & 0 & 0 & j \\ j & 0 & 0 & 1 \\ 0 & j & 1 & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \quad (4)$$

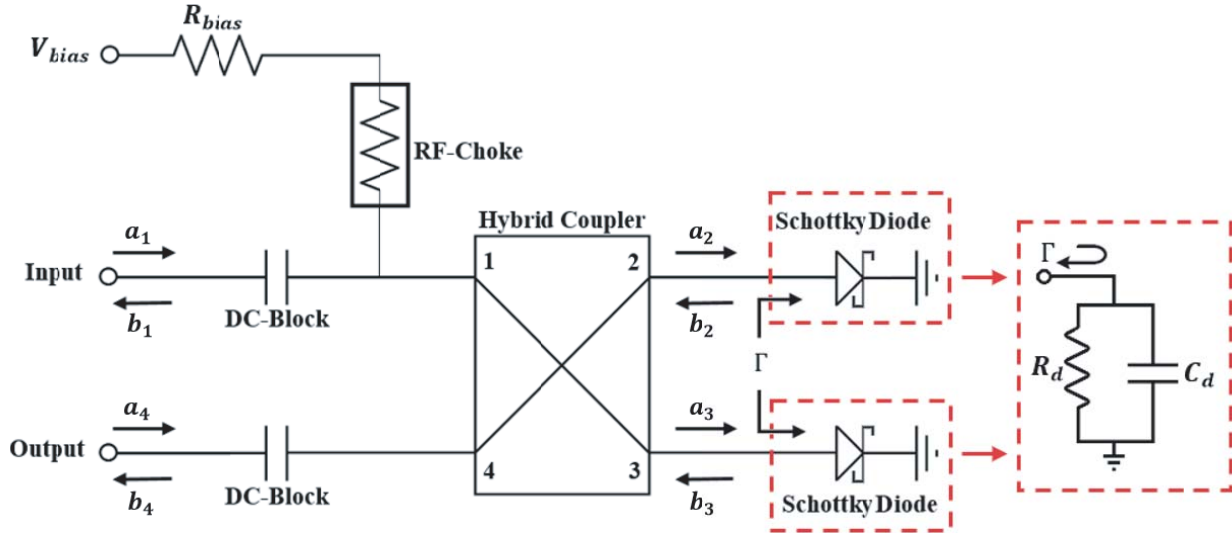


Figure 5. Schematic of the reflective Schottky diode PD linearizer.

From Fig. 5 it is obvious that $a_4 = 0$ since port 4 is the transmitting port and is matched to characteristic impedance of the coupler. Therefore, the reflection coefficient at this port is 0, and there is no reflected signal. It is also evident that $a_2 = \Gamma b_2$ and $a_3 = \Gamma b_3$ where Γ is the nonlinear reflection coefficient at the nonlinear branches. By substituting these values in Equation (4), the following relation between the input signal a_1 and output signal b_4 would be derived:

$$b_4 = -j\Gamma a_1 \quad (5)$$

Therefore, the gain G and phase shift $\Delta\varphi$ of the linearizer are given by Equation (6).

$$G = 20\log(|\Gamma|) \quad (6a)$$

$$\Delta\varphi = -90^\circ + \angle\Gamma \quad (6b)$$

As stated in the preceding section, the equivalent RF circuit of forward biased Schottky diode consists of the dynamic resistance R_d and junction capacitance C_d (Fig. 2(a)). Thus, the reflection coefficient Γ is given by Equation (7).

$$\Gamma = \frac{\left(\frac{1}{Z_0} - \frac{1}{R_d}\right) - jC_d\omega}{\left(\frac{1}{Z_0} + \frac{1}{R_d}\right) + jC_d\omega} \quad (7)$$

Magnitude and phase of Γ can be derived from Equation (7) as shown below.

$$|\Gamma| = \sqrt{\frac{\left(\frac{1}{Z_0} - \frac{1}{R_d}\right)^2 + (C_d\omega)^2}{\left(\frac{1}{Z_0} + \frac{1}{R_d}\right)^2 + (C_d\omega)^2}} \quad (8a)$$

$$\angle\Gamma = -\tan^{-1}\left(\frac{C_d\omega}{\frac{1}{Z_0} - \frac{1}{R_d}}\right) - \tan^{-1}\left(\frac{C_d\omega}{\frac{1}{Z_0} + \frac{1}{R_d}}\right) \quad (8b)$$

As discussed earlier, the value of dynamic resistance R_d increases when the input power level rises. Thus it can be concluded from Equations (6) and (8) that this structure can provide the desired magnitude characteristics of a PD linearizer. Fig. 6 shows the calculated gain and phase characteristics

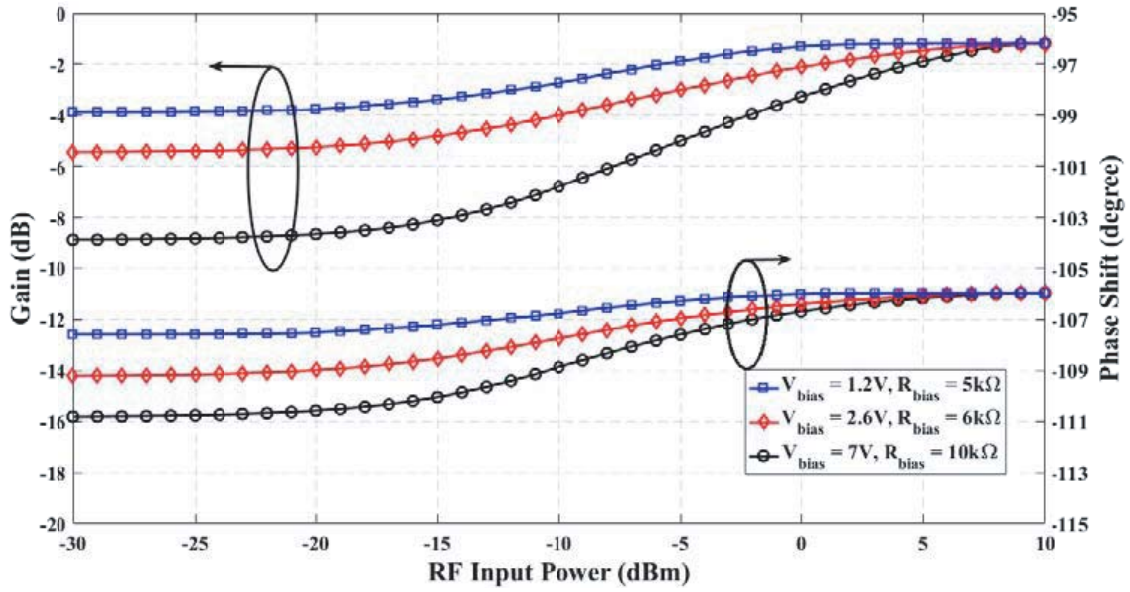


Figure 6. Calculated gain and phase characteristics of the reflective Schottky diode PD linearizer.

at the center frequency of 2 GHz using the dynamic resistance behavior obtained in the preceding section. Junction capacitance is assumed to be constant over the applied input power range. As shown in Fig. 6, this structure is capable of providing the desired magnitude response. However, phase expansion is small since Schottky diode has a relatively small junction capacitance. Another limit to be considered is that this structure can only provide expansive phase shift characteristics, and the direction of the phase deviation cannot be controlled. This limits the use of this linearizer since solid-state PAs (SSPAs) typically require compressive phase shift characteristics for linearization. These issues can be solved by using this distortion generator in a more complicated structure at the expense of a larger area, a more complicated circuit, and greater insertion loss. This issue will be revisited later in this paper.

4. EXPERIMENTAL RESULTS

To validate the presented concept, a reflective Schottky diode PD linearizer is simulated, fabricated, and finally measured at the center frequency of 2 GHz. A photograph of the fabricated linearizer is shown in Fig. 7(a). The linearizer is fabricated on an RO4003C substrate with the dielectric constant of 3.38, thickness of 20 mil, loss tangent of 0.0027, and 35 μm copper thickness on both sides. The used Schottky diode is MA4E2054 from MACOM. A double-box branchline coupler is used as the hybrid coupler to increase the operating bandwidth compared to a regular branchline coupler [29]. The detailed schematic of the fabricated linearizer is shown in Fig. 7(b). All simulations are carried out by using ADS momentum, and the measurements are performed by Agilent MXG N5181A signal generator and Agilent N9000A CXA spectrum analyzer.

Figure 8 shows the normalized gain conversion under different DC bias conditions obtained from simulation and measurement. As illustrated in Fig. 8, various combinations of magnitude characteristics can be created by adjusting the DC bias of the diodes. Therefore, this structure can be used to linearize a wide range of PAs with different behaviors. The fabricated linearizer is capable of providing up to 7.5 dB gain expansion over a 40 dB input power dynamic range at the center frequency of 2 GHz. The results of the simulation and measurement are found fairly consistent with each other. Fig. 9 shows the measured gain response of the fabricated linearizer over 1.9–2.1 GHz under small and large input power levels for the DC bias condition which results in maximum gain expansion. Fig. 9 shows a gain expansion from 7.4 to 7.85 dB across the frequency band with an insertion loss of less than 1.93 dB.

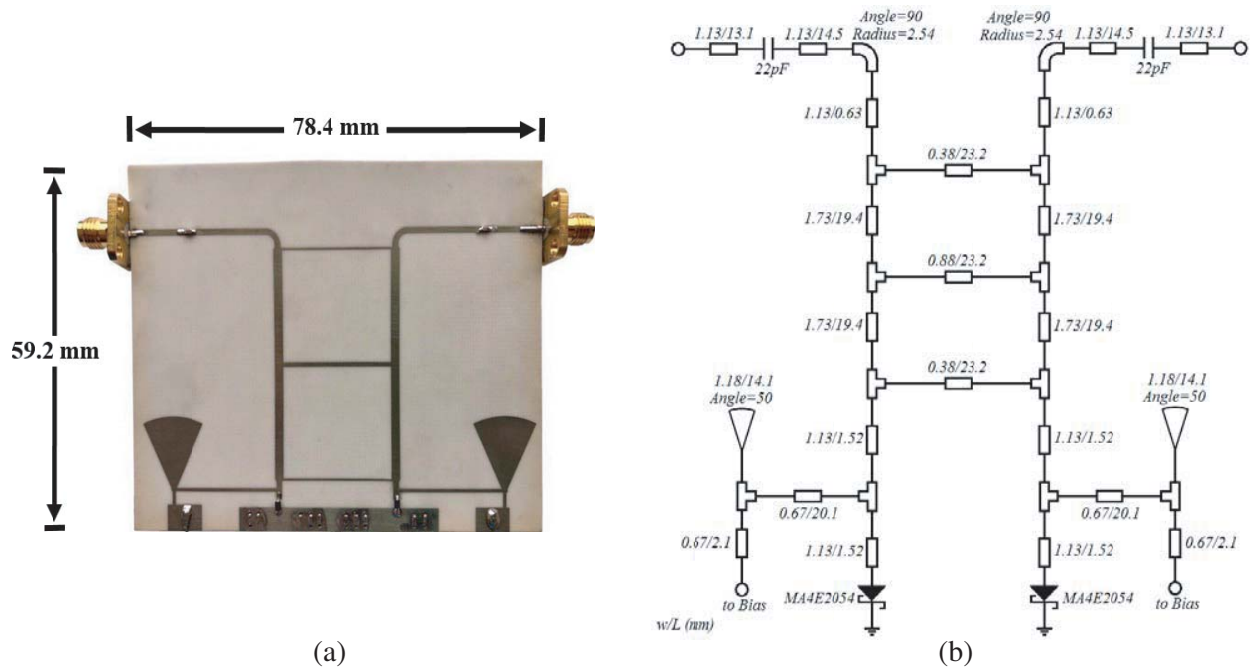


Figure 7. (a) Photograph of the fabricated reflective PD linearizer. (b) Detailed schematic of the fabricated reflective PD linearizer (dimensions are in millimeters).

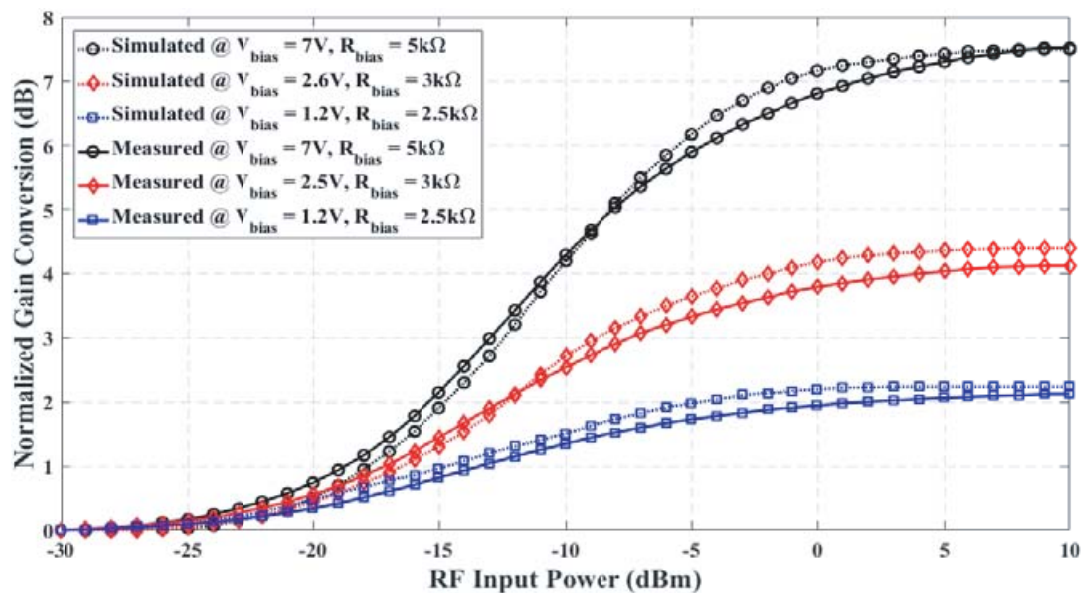


Figure 8. Simulated and measured normalized gain conversion of the reflective Schottky diode PD linearizer.

5. DUAL-BRANCH REFLECTIVE PREDISTORTION LINEARIZER

As previously mentioned, Schottky diode has a relatively small junction capacitance. Therefore, the reflective Schottky diode PD linearizer is not suitable for PAs with high phase nonlinearity. Furthermore, the direction of the phase deviation cannot be changed which limits the use of this structure. These issues can be solved by using the Schottky distortion generator in a more complicated structure at the expense

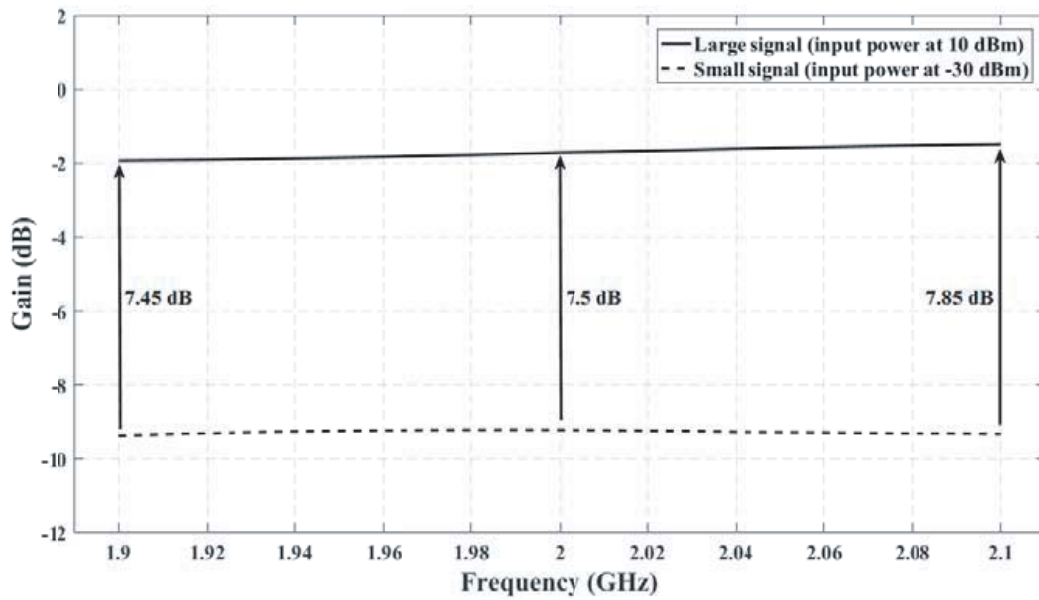


Figure 9. Measured gain response of the reflective PD linearizer over the frequency range of 1.9–2.1 GHz.

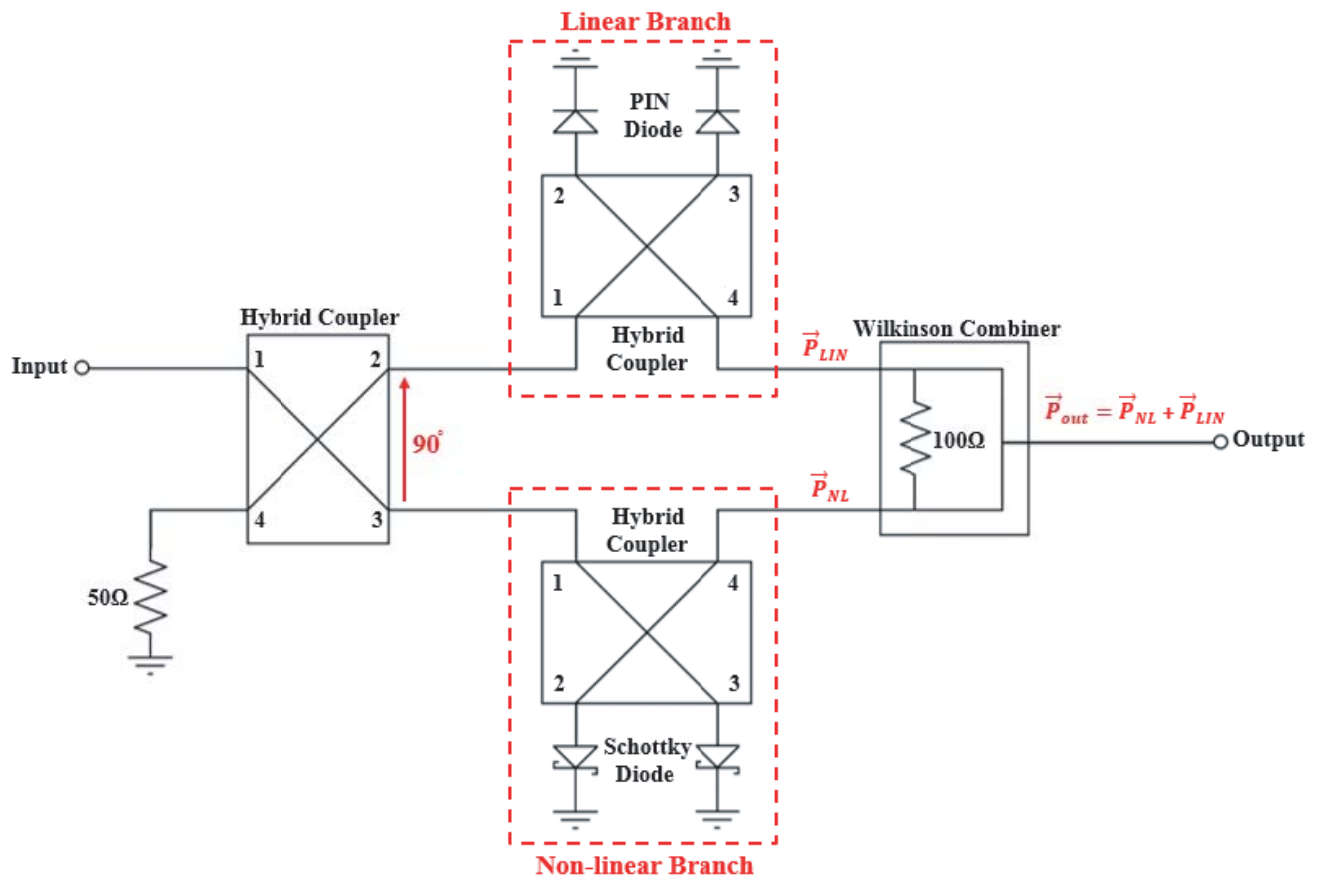


Figure 10. Simplified schematic of the dual-branch PD linearizer [18].

of a larger area, a more complicated circuit, and greater insertion loss. The dual-branch architecture shown in Fig. 10 is capable of reducing high AM/PM distortion as well as AM/AM distortion [18]. In this topology, the input signal is divided into two signals with equal magnitudes and a 90° phase difference; one signal is fed to a linear branch and the other to a nonlinear branch. The nonlinear branch consists of a distortion generator, i.e., reflective Schottky diode PD linearizer. The linear branch is a reflective variable attenuator based on PIN diode. A PIN diode acts as a linear RF current-controlled resistor where the resistance is an inverse function of the forward DC current of the diode. Therefore, the insertion loss of the attenuator can be adjusted by changing the bias current. The outputs of these branches are then combined using an in-phase power combiner.

The vector diagram given in Fig. 11 demonstrates the concept of this PD linearizer [18]. For the small input power level, the vectors corresponding to the gain of linear and nonlinear branches are OL and ON_1 , respectively. As the RF input power level rises, the vector ON_1 increases to ON_2 , while the vector OL remains unchanged. Therefore, the resultant output vector changes from OR_1 to OR_2 [18], which results in a gain expansion of ΔG and a phase compression of $\Delta\varphi$ at the output. It should be noted that the direction of the phase deviation can be changed by switching the position of the diodes.

A dual-branch PD linearizer is designed and simulated using ADS momentum. To show the feasibility of applying the reflective Schottky diode PD linearizer at higher frequencies, the circuit is designed at the center frequency of 13.5 GHz. HSCH5312 Schottky diode and HPND4005 PIN diode are adopted

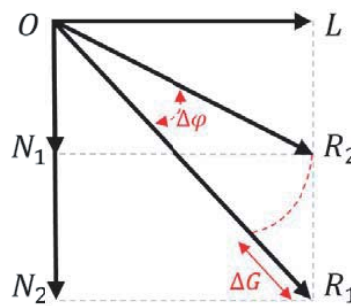


Figure 11. Vector diagram of the dual-branch topology [18].

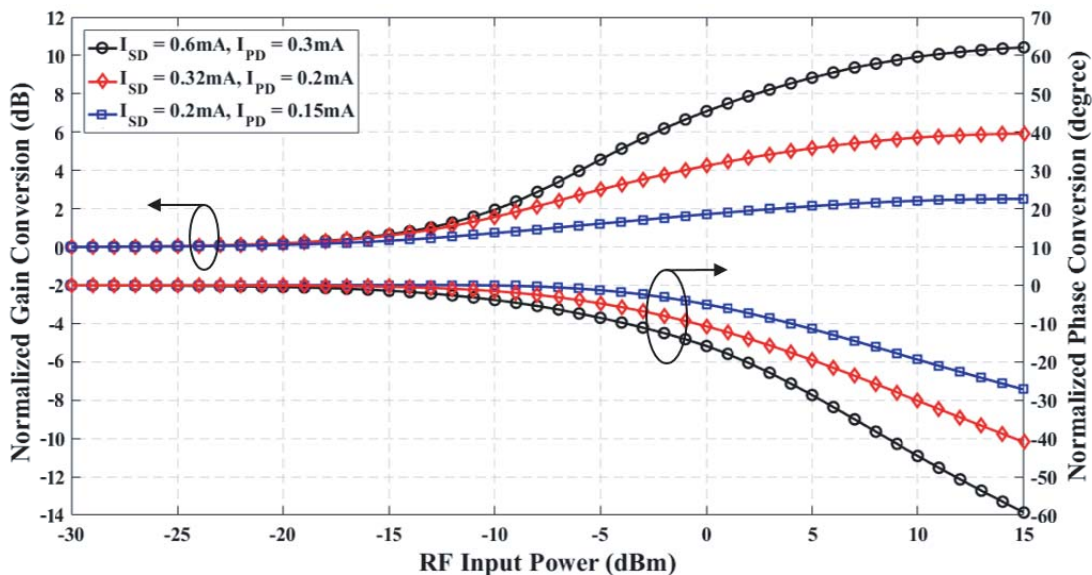


Figure 12. Simulated normalized gain conversion and phase conversion of the dual-branch reflective PD linearizer (I_{SD} and I_{PD} denote the DC bias current of the Schottky diode and PIN diode, respectively).

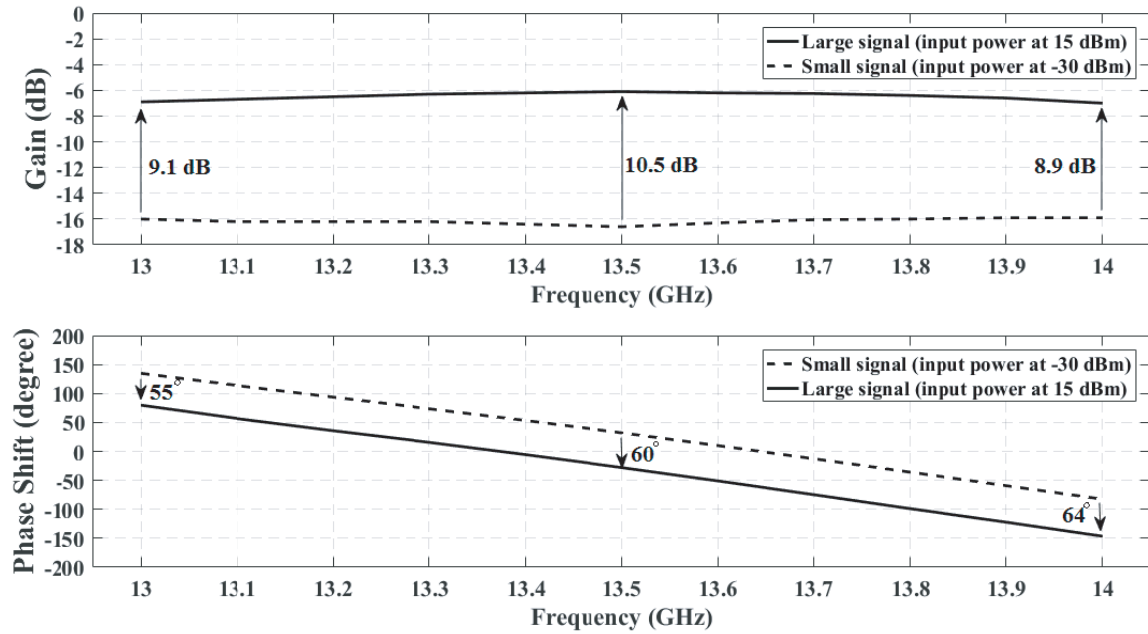


Figure 13. Simulated frequency response of the dual-branch reflective PD linearizer over the frequency range of 13–14 GHz.

Table 1. Performance comparison with similar reported analog PD linearizers.

Ref.	Structure	Center Frequency (GHz)	Fractional Bandwidth (%)	Maximum Gain Expansion (dB) ⁽¹⁾	Maximum Phase Deviation (degree) ⁽¹⁾	Insertion Loss (dB) ⁽¹⁾
[12]	Analog PD linearizer using a parallel Schottky diode	2.7	—	3.5	25	—
[13]	Reflective Analog PD linearizer based on variable impedance matching network	30	6.7	6.5	55	—
[14]	Reflective Analog PD linearizer	12.5	4	7.2	45	—
[17]	Wideband Reflective Analog PD linearizer	49	12.2	4.03	42.5	—
[18]	Dual-branch linearizer using PIN and Schottky diodes	—	—	10	65	—
[19]	Dual-branch PD linearizer using FET and Schottky diode	8.48	2.35	6	45	20.25
[20]	Dual-branch topology with independent tunable gain and phase conversions	30	6.7	7.7	59.2	12.5
This work	Reflective Schottky diode PD linearizer	2	10	7.5	—	1.7
This work	Dual-branch PD linearizer ⁽²⁾	13.5	7.4	10.5	60	6.1

(1)Data reported at the center frequency

(2) Simulation results

in this design. Double-box branchline coupler and 3-dB Wilkinson power combiner are designed on the same microstrip substrate as the preceding section. Fig. 12 shows the simulated normalized gain conversion and phase conversion under different DC bias conditions. As illustrated in Fig. 12, various combinations of magnitude and phase characteristics can be created by adjusting the DC bias of the diodes. The simulated results show a maximum of 10.5 dB gain expansion and 60° phase deviation. Fig. 13 shows the simulated frequency response of the designed linearizer over 13–14 GHz under small and large input power levels under the DC bias condition which results in maximum gain expansion. Fig. 13 shows a gain expansion from 8.9 to 10.5 dB and a phase deviation from 55° to 64° across the frequency band with an insertion loss of less than 7 dB.

The results obtained for the presented PD linearizers in this work are compared with similar analog PD linearizers in Table 1. As seen, the PD linearizers presented have good tuning capability, wide bandwidth, and low insertion loss in comparison with previous works.

6. CONCLUSION

In this paper, the design, simulation, and measurement of a simple and tunable diode-based reflective analog PD linearizer with low insertion loss is presented. This structure is capable of providing various combinations of characteristics only by adjusting the DC bias of the diodes. Therefore, it can be used to linearize a wide range of PAs. Experimental validation at the center frequency of 2 GHz shows that the fabricated linearizer can provide up to 7.5 dB gain expansion. The fractional bandwidth and insertion loss of the fabricated linearizer are 10% and 1.7 dB, respectively. The simulated and measured results are in good agreement with each other. As an approach for compensating the limited phase characteristics of the presented structure, the design and simulation of a dual-branch PD linearizer utilizing the reflective Schottky diode PD linearizer as a nonlinear unit is also presented.

REFERENCES

1. Katz, A., J. Wood, and D. Chokola, "The evolution of PA linearization: From classic feedforward and feedback through analog and digital predistortion," *IEEE Microwave Magazine*, Vol. 17, No. 2, 32–40, Feb. 2016.
2. Andreoli, S., H. G. McClure, P. Banelli, and S. Cacopardi, "Digital linearizer for RF amplifiers," *IEEE Transactions on Broadcasting*, Vol. 43, No. 1, 12–19, Mar. 1997.
3. Vassiliou, I., K. Vavelidis, T. Georgantas, S. Plevridis, N. Haralabidis, G. Kamoulakos, C. Kapnistis, S. Kavadias, Y. Kokolakis, P. Merakos, J. C. Rudell, A. Yamanaka, S. Bouras, and I. Bouras, "A single-chip digitally calibrated 5.15 ~ 5.825-GHz 0.18- μ m CMOS transceiver for 802.11a wireless LAN," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 12, 2221–2231, Dec. 2003.
4. Grebennikov, A. and S. Bulja, "High-efficiency doherty power amplifiers: Historical aspect and modern trends," *Proceedings of the IEEE*, Vol. 100, No. 12, 3190–3219, Dec. 2012.
5. Katz, A., "Linearization: Reducing distortion in power amplifiers," *IEEE Microwave Magazine*, Vol. 2, No. 4, 37–49, 2001.
6. Gokceoglu, A., A. ghadam, and M. Valkama, "Steady-state performance analysis and step-size selection for LMS-adaptive wideband feedforward power amplifier linearizer," *IEEE Transactions on Signal Processing*, Vol. 60, No. 1, 82–99, Jan. 2012.
7. Ghadam, A., S. Burglechner, A. H. Gokceoglu, M. Valkama, and A. Springer, "Implementation and performance of DSP-oriented feedforward power amplifier linearizer," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 59, No. 2, 409–425, Feb. 2012.
8. Pipilos, S., Y. Papananos, N. Naskas, M. Zervakis, J. Jongsma, T. Gschier, N. Wilson, J. Gibbins, B. Carter, and G. Dann, "A transmitter IC for TETRA systems based on a Cartesian feedback loop linearization technique," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 3, 707–718, Mar. 2005.
9. Kim, J. H. and C. S. Park, "A feedback technique to compensate for AM-PM distortion in linear CMOS class-F power amplifier," *IEEE Microwave and Wireless Components Letters*, Vol. 24, No. 10, 725–727, Oct. 2014.

10. Kang, S., E.-T. Sung, and S. Hong, "Dynamic feedback linearizer of RF CMOS power amplifier," *IEEE Microwave and Wireless Components Letters*, Vol. 28, No. 10, 915–917, Oct. 2018.
11. Abbasnezhad, F., M. Tayarani, A. Abrishamifar, and V. Nayyeri, "A simple and adjustable technique for effective linearization of power amplifiers using harmonic injection," *IEEE Access*, Vol. 9, 37287–37296, Mar. 2021.
12. Yamauchi, K., K. Mori, M. Nakayama, Y. Mitsui, and T. Takagi, "A microwave miniaturized linearizer using a parallel diode with a bias feed resistance," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 45, No. 12, 2431–2435, Dec. 1997.
13. Deng, H., D. Zhang, D. Lv, D. Zhou, and Y. Zhang, "A tunable reflective analog predistorter based on variable impedance matching network," *AEU — International Journal of Electronics and Communications*, Vol. 98, 139–143, Jan. 2019.
14. Chen, X., D. Zhou, J. Xu, and L. Yang, "Predistortion linearization of a Ku-band TWTA for communication applications," *Proceedings of the 2nd International Conference on Computer Science and Electronics Engineering (ICCSEE 2013)*, Mar. 2013.
15. Zhou, R., X. Xie, B. Yan, and S. Li, "A novel diode-based predistortion linearizer for Ka-band power amplifier," *2012 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, May 2012.
16. Hashmi, M. S., Z. S. Rogojan, and F. M. Ghannouchi, "A flexible dual-inflection point RF predistortion linearizer for microwave power amplifiers," *Progress In Electromagnetics Research C*, Vol. 13, 1–18, 2010.
17. Bian, C., D. Zhang, H. Deng, Q. Liu, D. Lv, Y. Zhang, and D. Zhou, "Complete analysis and design for a Q/V band (46–52 GHz) wideband analog predistorter," *International Journal of RF and Microwave Computer-Aided Engineering*, Vol. 31, No. 2, Dec. 2020.
18. Bera, S. C., P. S. Bhardhwaj, R. V. Singh, and V. K. Garg, "A diode linearizer for microwave power amplifiers," *Microwave Journal*, Vol. 46, No. 11, 102–113, Nov. 2003.
19. Hu, X., G. Wang, Z.-C. Wang, and J.-R. Luo, "Predistortion linearization of an X-band TWTA for communications applications," *IEEE Transactions on Electron Devices*, Vol. 58, No. 6, 1768–1774, Jun. 2011.
20. Deng, H., D. Zhang, D. Lv, D. Zhou, and Y. Zhang, "Analog predistortion linearizer with independently tunable gain and phase conversions for Ka-band TWTA," *IEEE Transactions on Electron Devices*, Vol. 66, No. 3, 1533–1539, Mar. 2019.
21. Tripathi, G. C. and M. Rawat, "RF_{in}-RF_{out} linearizer system design for satellite communication," *IEEE Transactions on Electron Devices*, Vol. 65, No. 6, 2378–2384, Jun. 2018.
22. Guan, N., N. Wu, and H. Wang, "Digital predistortion of wideband power amplifier with single undersampling ADC," *IEEE Microwave and Wireless Components Letters*, Vol. 27, No. 11, 1016–1018, Nov. 2017.
23. Liu, X., Q. Zhang, W. Chen, H. Feng, L. Chen, F. M. Ghannouchi, and Z. Feng, "Beam-oriented digital predistortion for 5G massive MIMO hybrid beamforming transmitters," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 66, No. 7, 3419–3432, Jul. 2018.
24. Zhao, J., C. Yu, J. Yu, Y. Liu, and S. Li, "A robust augmented combination of digital predistortion and crest factor reduction for RF Power Amplifiers," *Progress In Electromagnetics Research C*, Vol. 57, 181–191, 2015.
25. Hu, X., Z. Liu, W. Wang, M. Helaoui, and F. M. Ghannouchi, "Low-feedback sampling rate digital predistortion using deep neural network for wideband wireless transmitters," *IEEE Transactions on Communications*, Vol. 68, No. 4, 2621–2633, Apr. 2020.
26. Ciminski, A. S., "Neural network based adaptable control method for linearization of high power amplifiers," *AEU — International Journal of Electronics and Communications*, Vol. 59, No. 4, 239–243, Jun. 2005.
27. Rawat, M., K. Rawat, and F. M. Ghannouchi, "Adaptive digital predistortion of wireless power amplifiers/transmitters using dynamic real-valued focused time-delay line neural networks," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 58, No. 1, 95–104, Jan. 2010.

28. GraciaSaez, R. and N. Medrano Marques, "RF power amplifier linearization in professional mobile radio communications using artificial neural networks," *IEEE Transactions on Industrial Electronics*, Vol. 66, No. 4, 3060–3070, Apr. 2019.
29. Pozar, D. M., *Microwave Engineering*, Wiley, New York, 2005.
30. Lopez, D., J.-F. Villemazet, D. Geffroy, J.-L. Cazaux, G. Mouchon, J. Maynard, M. Perrel, and M. Amarouali, "Ka band power limiter for satellite channel amplifier," *2009 SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference (IMOC)*, Nov. 2009.
31. Bera, S. C., K. Basak, V. K. Jain, R. V. Singh, and V. K. Garg, "Schottky diode-based microwave limiter with adjustable threshold power level," *Microwave and Optical Technology Letters*, Vol. 52, No. 7, 1671–1673, Jul. 2010.
32. Maas, S. A., *Nonlinear Microwave Circuit*, Artech House, Norwood, MA, 1988.