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Research on Conducted EMI Characteristics of SiC MOSFET Considering Temperature Effect

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Abstract—The junction temperature change of SiC MOSFET will change its switching process, and then affect the electromagnetic interference (EMI) characteristics of the system where the device is located and the safe operation of the surrounding equipment. Therefore, it is of great significance to research the temperature dependence of its EMI characteristics. In this paper, a buck converter composed of SiC MOSFET is taken as the research object to study the temperature variation characteristics of the conducted EMI spectrum during the switching process. Combined with the specific circuit connection form of the buck converter, the coupling paths of the conducted EMI are determined, and then the influence mechanisms of temperature change on the differential mode (DM) interference and common mode (CM) interference are analyzed. The theoretical analysis and experimental results show that the DM interference of the buck converter composed of SiC MOSFET increases with the increase of temperature, and the CM interference is almost unaffected by temperature. When the working temperature increases from 25°C to 145°C, the peak value of DM voltage increases by 6.7 dBμV, and the peak value of CM voltage changes less than 1.4 dBμV.

1. INTRODUCTION

SiC MOSFET is widely used in high-frequency and high-power fields such as electric vehicle, smart grid, and aerospace due to its high switching speed, high working temperature, and low switching loss [1–3]. However, high switching frequency and high power increase the electromagnetic interference (EMI) in the system [4] which affects the safe operation of the surrounding equipment [5, 6]. Due to the long-time operation of SiC MOSFET under severe conditions, it is vital to properly handle the electromagnetic compatibility (EMC) problem to ensure the reliable operation of the system [7]. The high *di/dt* and *dv/dt* during the SiC MOSFET switching process are the main sources of EMI [8–10], and the temperature will affect the switching process [11–14], so the temperature will affect its EMI characteristics. As EMC standards become more and more strict, a better understanding of the EMI characteristics in the system is of great significance to guide the design of related products [15, 16].

Because SiC MOSFET has the characteristics of high switching frequency and high power, the EMI problem of the power converter composed of SiC MOSFET has always been the focus of researchers. The influence mechanisms of driving parameters, parasitic inductance, module ground parasitic capacitance, switching frequency, package structure, and modulation mode on the EMI characteristics have been studied in [17–21]. However, the theoretical analysis and variation law of the temperature effect on the EMI characteristics of SiC MOSFET have not been fully studied [22]. Due to the small temperature dependence of the internal gate resistance [23], interelectrode parasitic capacitance [24], module-ground parasitic capacitance [25], and smaller parasitic inductance with the development of packaging

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technology [26], the temperature dependence of these parameters can be ignored when the temperature effect on conducted EMI in the system is analyzed. The temperature effect on the EMI characteristics of SiC MOSFET is essentially the temperature effect on the characteristics of semiconductor materials. The increase of temperature will change the intrinsic carrier concentration, carrier mobility, and other internal parameters, which are characterized by the change of threshold voltage and transconductance, then cause the change of SiC MOSFET switching process, and ultimately affect its EMI characteristics. The researches in [11–13] show that with the increase of temperature, the turn-on processes di/dt and dv/dt of SiC MOSFET increase, while the turn-off processes di/dt and dv/dt decrease. In the process of measuring the temperature variation characteristics of the SiC MOSFET conducted EMI spectrum, we found that the temperature dependence of the turn-on process di/dt is higher than that of the turn-off process di/dt, and the theoretical basis of this phenomenon is found through theoretical derivation and analysis.

To sum up, this paper takes a buck converter composed of SiC MOSFET as the research object, and focuses on the temperature variation characteristics of the SiC MOSFET conducted EMI spectrum, which provides a reference for the EMC design of power converter. The structure of the paper is as follows. In the second section, the temperature variation mechanisms of the SiC MOSFET conducted EMI spectrum are analyzed, and on this basis, the temperature variation characteristics of conducted EMI in the system are demonstrated by combining the interference coupling paths in the buck converter. In the third section, the correctness of the theory is verified by the test results of conducted EMI. The fourth section presents the conclusion.

2. THEORETICAL ANALYSIS

Considering that the EMI characteristics of the buck converter are typical and can be extended to the conducted EMI analysis of other converters [17], this paper takes a buck converter composed of SiC MOSFET as the research object to analyze the temperature variation characteristics of the conducted EMI signals in the buck converter. The equivalent circuit diagram of the buck converter composed of SiC MOSFET is shown in Fig. 1.

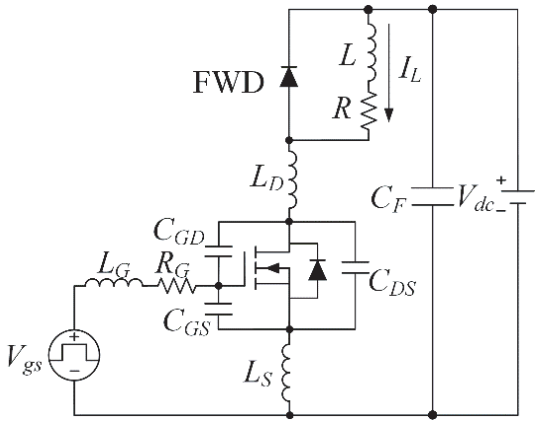

Figure 1. Equivalent circuit diagram of buck converter composed of SiC MOSFET.

In Fig. 1, V_{dc} is the bus voltage, I_L the load current, and the freewheeling diode (FWD) provides the conduction path for the load current when the SiC MOSFET is turned off. The total gate resistance R_G is composed of gate resistance and external driving resistance. L_G, L_S, and L_D are the gate inductance, common source inductance, and drain inductance, respectively. C_{GS}, C_{DS}, and C_{GD} are the gate-source parasitic capacitance, drain-source parasitic capacitance, and gate-drain parasitic capacitance, respectively. The input capacitance is defined as $C_{iss} = C_{GS} + C_{GD}$. The output voltage of the buck converter is realized by controlling the duty cycle of the gate drive signal. During the period when a positive drive voltage is applied, the SiC MOSFET is gradually turned on; the freewheeling diode is blocked; and the bus voltage V_{dc} supplies power to the load. During the period when a negative drive

voltage is applied, the SiC MOSFET is gradually turned off, and the energy stored in the load current I_L is released through the freewheeling diode.

The voltage and current waveforms of SiC MOSFET switching process are shown in Fig. 2.

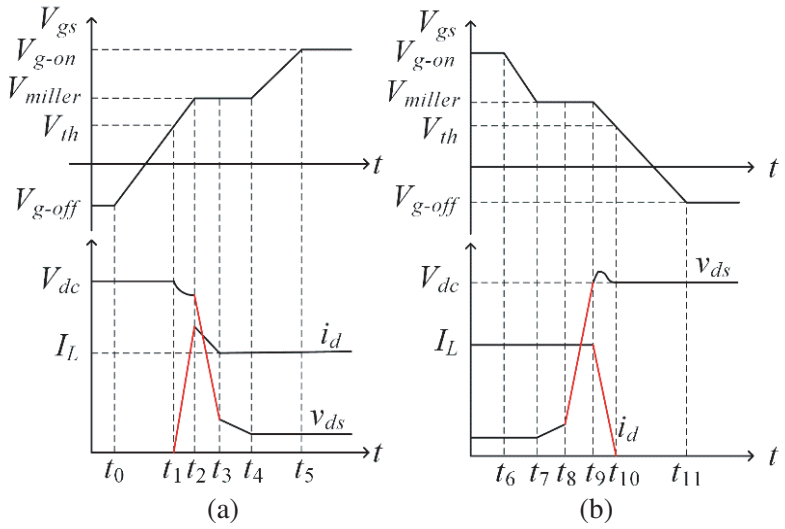

Figure 2. Voltage and current waveforms of SiC MOSFET switching process. (a) Turn-on and (b) Turn-off.

In the buck converter composed of SiC MOSFET, the coupling of high *di/dt* and parasitic inductance produces a large amount of DM interference in the circuit; the interaction of high *dv/dt* and parasitic capacitance produces a large amount of CM interference between the phase line and the ground line [17]. Since the parasitic capacitance C_{GD}, which varies with the inter-electrode voltage, is smaller in the t_2–t_3 stage than in the t_3–t_4 stage, the *dv/dt* negatively related to C_{GD} is larger in the t_2–t_3 stage. Similarly, the *dv/dt* during the turn-off process is larger in the t_8–t_9 stage than in the t_7–t_8 stage. Therefore, during the SiC MOSFET switching process, the larger *di/dt* in the two stages of t_1–t_2 and t_9–t_{10} are the main sources of the DM interference, and the larger *dv/dt* in the two stages of t_2–t_3 and t_8–t_9 are the main sources of CM interference. In this paper, we will analyze the DM interference and CM interference in two parts.

2.1. DMInterference Analysis

2.1.1. Temperature Variation Mechanism of DMInterference Spectrum

During the t_1–t_2 stage, when the gate source voltage V_{gs} exceeds the threshold voltage V_{th}, the channel of SiC MOSFET gradually forms, and the drain current i_d increases rapidly. The change rate of i_d in this stage is shown in Eq. (1) [27]

$$\frac{di_{d\text{-}on}}{dt} = \frac{V_{g\text{-}on} - V_{th} - I_L/g_{fs}}{R_G C_{iss}/g_{fs} + L_S} \tag{1}$$

where g_{fs} is the transconductance, and $V_{g\text{-}on}$ is the turn-on driving voltage.

During the t_9t_{10} stage, V_{gs} drops from the Miller voltage V_{miller} to V_{th}; the freewheeling diode is forward biased; I_L gradually transfers from the SiC MOSFET to the freewheeling diode; and i_d begins to decrease rapidly. The change rate of i_d in this stage is shown in Eq. (2) [27].

$$\frac{di_{d\text{-}off}}{dt} = \frac{V_{g\text{-}off} - V_{th} - I_L/g_{fs}}{R_G C_{iss}/g_{fs} + L_S} \tag{2}$$

where $V_{g\text{-}off}$ is the negative turn-off driving voltage.

According to Eqs. (1) and (2), the temperature variation characteristics of the DM interference sources are mainly affected by V_{th} and g_{fs} under the premise that the gate driving voltage amplitude remains unchanged.

The expression of V_{th} is [28]:

$$V_{th}=V_{FB}+2\psi_B+\frac{\sqrt{4\varepsilon_{SiC}qN_A\psi_B}}{C_{ox}}=V_{FB}+2\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)+\frac{\sqrt{4\varepsilon_{SiC}qN_A\psi_B}}{C_{ox}} \tag{3}$$

where V_{FB} is the flat-band voltage, ψ_B the Fermi potential, C_{ox} the gate oxide capacitance, q the electron charge, ε_{SiC} the dielectric constant of SiC, N_A the doping concentration, k the Boltzmann constant, and n_i the intrinsic carrier concentration.

With the increase of temperature, n_i increases, and then ψ_B decreases. Although V_{FB} increases with the increase of temperature, V_{th} has a negative temperature dependence in general [23].

The expression of g_{fs} is [28]:

$$g_{fs}=\frac{W_{ch}\mu C_{ox}}{2L_{ch}}(V_{gs}-V_{th}) \tag{4}$$

where W_{ch} and L_{ch} are the channel width and length of SiC MOSFET, respectively. μ is the carrier mobility, and considering its widebandgap characteristics, the temperature effect on μ can be neglected [29]. According to Eq. (4), the temperature dependence of g_{fs} is opposite to that of V_{th}, so g_{fs} has a positive temperature dependence.

Based on the above analysis, di_d/dt has positive temperature dependence both during the turn-on and turn-off process. Since $di_{d\text{-}on}/dt$ is positive, with the increase of temperature, the rising rate of i_d increases, which increases the DM interference generated in the turn-on process; since $di_{d\text{-}off}/dt$ is negative, with the increase of temperature, the falling rate of i_d decreases, which decreases the DM interference generated in the turn-off process. To further clarify the difference of di_d/dt changes during the turn-on and turn-off process, it is necessary to analyze the relationship between $di_{d\text{-}on}/dt$ and $di_{d\text{-}off}/dt$ with temperature.

Differentiate Eqs. (1) and (2) with respect to temperature, respectively, to obtain Eqs. (5) and (6).

$$\frac{d^2i_{d\text{-}on}}{dtdT}=-\frac{g_{fs}}{R_GC_{iss}+g_{fs}L_S}\frac{dV_{th}}{dT}+\frac{(V_{g\text{-}on}-V_{th})R_GC_{iss}+I_LL_S}{(R_GC_{iss}+g_{fs}L_S)^2}\frac{dg_{fs}}{dT} \tag{5}$$

$$\frac{d^2i_{d\text{-}off}}{dtdT}=-\frac{g_{fs}}{R_GC_{iss}+g_{fs}L_S}\frac{dV_{th}}{dT}+\frac{(V_{g\text{-}off}-V_{th})R_GC_{iss}+I_LL_S}{(R_GC_{iss}+g_{fs}L_S)^2}\frac{dg_{fs}}{dT} \tag{6}$$

According to Eqs. (5) and (6), the difference of di_d/dt temperature dependence during the turn-on and turn-off processes of SiC MOSFET is shown in Eq. (7).

$$\left|\frac{d^2i_{d\text{-}on}}{dtdT}\right|-\left|\frac{d^2i_{d\text{-}off}}{dtdT}\right|=\frac{(V_{g\text{-}on}-V_{g\text{-}off})R_GC_{iss}}{(R_GC_{iss}+g_{fs}L_S)^2}\frac{dg_{fs}}{dT}>0 \tag{7}$$

According to Eq. (7), the temperature dependence of di_d/dt during the turn-on process of SiC MOSFET is stronger than that during the turn-off process. To further quantify the variation degree of di_d/dt with temperature during the turn-on and turn-off process of SiC MOSFET, the drain current waveforms of the switching process at different temperatures are obtained through double pulse test experiment, as shown in Fig. 3.

The experimental results show that with the increase of temperature, the rising rate of i_d during the turn-on process of SiC MOSFET increases. When the temperature increases from 25°C to 145°C, di_d/dt increases from 50.30 A/μs to 56.25 A/μs. However, with the increase of temperature, the falling rate of i_d does not change significantly during the turn-off process. Therefore, the temperature change mainly affects di_d/dt during the turn-on process, and then affects the DM interference spectrum of the buck converter composed of SiC MOSFET.

2.1.2. Acquisition of Temperature Variation Characteristics of DMInterference Spectrum

The equivalent circuit diagram of the conducted EMI test for the buck converter is shown in Fig. 4.

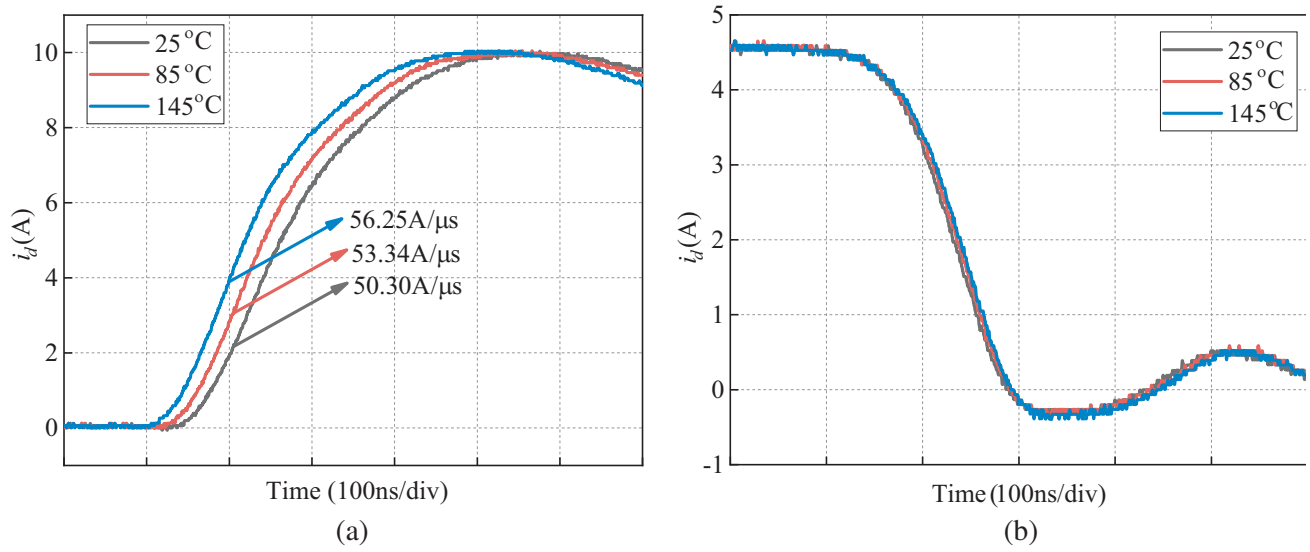

Figure 3. Drain current waveforms at different temperatures. (a) Turn-on, and (b) Turn-off.

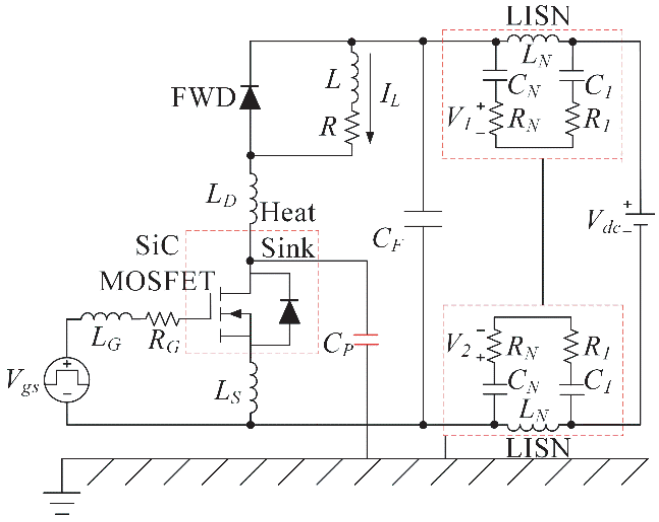

Figure 4. Equivalent circuit diagram of conducted EMI test for buck Converter.

In Fig. 4, the DC power supply supplies power to the system through the line impedance stabilization network (LISN). The function of LISN is to isolate the interference from the DC power supply and make the test results correct and repeatable. C_P is the parasitic capacitance between the drain of SiC MOSFET and the heat sink. Since the heat sink is usually grounded, C_P provides a conduction path for CM interference. The thin film capacitor C_F is used to keep the voltage stable.

The coupling path of the DM interference in the system is shown in Fig. 5 [30].

In Fig. 5, R_{line1}, L_{line1}, R_{line2}, and L_{line2} are the resistance and inductance of the connecting line between C_F and LISN, respectively. R_F and L_F are the parasitic parameters of C_F. $I(s)$ is the frequency domain expression of the DM interference source $i_d(t)$, and V_{DM} is the DM interference voltage. The drain current $i_{d\text{-}on}(t)$ during the turn-on process, the drain current $i_{d\text{-}off}(t)$ during the turn-off process, the corresponding frequency domain expression, and the corresponding DM interference voltage are shown in Eqs. (8)–(13), respectively.

$$i_{d\text{-}on}(t) = \frac{di_{d\text{-}on}}{dt}t \quad (t_1 < t < t_2) \tag{8}$$

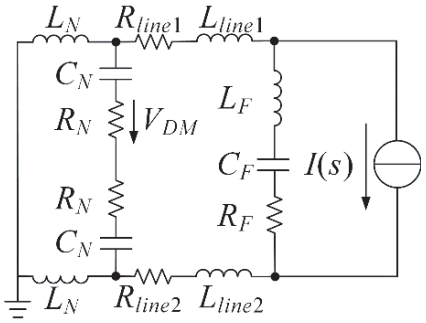

Figure 5. Coupling path of DM interference.

$$i_{d\text{-}off}(t) = I_L - \frac{di_{d\text{-}off}}{dt}t \quad (t_9 < t < t_{10}) \tag{9}$$

$$I_{d\text{-}on}(s) = FFT\left[i_{d\text{-}on}(t)\right] \tag{10}$$

$$I_{d\text{-}off}(s) = FFT\left[i_{d\text{-}off}(t)\right] \tag{11}$$

$$V_{DM\text{-}on}(s) = \frac{Z_2 Z_5 R_N}{(2Z_1 + Z_2)(Z_3 + Z_4 + Z_5) + 2Z_1 Z_2} I_{d\text{-}on}(s) \tag{12}$$

$$V_{DM\text{-}off}(s) = \frac{Z_2 Z_5 R_N}{(2Z_1 + Z_2)(Z_3 + Z_4 + Z_5) + 2Z_1 Z_2} I_{d\text{-}off}(s) \tag{13}$$

where $Z_1 = R_N + (1/j\omega C_N)$, $Z_2 = 2j\omega L_N Z_3 = R_{c1} + j\omega L_{c1} Z_4 = R_{c2} + j\omega L_{c2} Z_5 = R_F + j\omega L_F + (1/j\omega C_F)$.

Since this paper focuses on the temperature effect on conducted EMI signals during the turn-on and turn-off processes of SiC MOSFET, the relationship between temperature and conducted EMI signals in the system is obtained. Based on this, this paper should measure the conducted EMI spectrum during the turn-on and turn-off processes of SiC MOSFET, and compare the results with the theoretical analysis results. However, the SiC MOSFET works in continuous mode under working conditions, and the spectrum analyzer cannot independently measure the conducted EMI signals during the turn-on and turn-off process. Therefore, the average mode is chosen for the conducted EMI test in this paper, so that the measured spectrum includes both the turn-on and turn-off processes. According to the homogeneity and additivity of the Fourier algorithm, the DM interference voltage V_{DMave} generated by the drain current during the SiC MOSFEFT switching process is shown in Eq. (14)

$$V_{DM\text{-}ave} = \frac{V_{DM\text{-}on} + V_{DM\text{-}off}}{2} \tag{14}$$

2.2. CMInterference Analysis

2.2.1. Temperature Variation Mechanism of CM Interference Spectrum

During the t_2t_3 stage, when V_{gs} reaches V_{miller} the reverse recovery current of the freewheeling diode reaches the maximum, and the drain-source voltage v_{ds} decreases rapidly. The change rate of v_{ds} in this stage is shown in Eq. (15) [27].

$$\frac{dv_{ds\text{-}on}}{dt} = \frac{V_{th} - V_{g\text{-}on} + I_L/g_{fs}}{R_G C_{GD}} \tag{15}$$

During the t_8–t_9 stage, V_{gs} remains at V_{miller}, and v_{ds} increases rapidly. The change rate of v_{ds} in this stage is shown in Eq. (16) [27].

$$\frac{dv_{ds\text{-}off}}{dt} = \frac{V_{th} - V_{g\text{-}off} + I_L/g_{fs}}{R_G C_{GD}} \tag{16}$$

Combining the temperature variation characteristics of V_{th} and g_{fs} with Eqs. (15) and (16), dv_{ds}/dt has negative temperature dependence during both the turn-on and turn-off processes. Since $dv_{ds\text{-}on}/dt$

is negative, with the increase of temperature, the falling rate of v_{ds} increases, which increases the CM interference generated in the turn-on process; since $dv_{ds\text{-}off}/dt$ is positive, with the increase of temperature, the rising rate of v_{ds} decreases, which decreases the CM interference generated in the turn-off process. To further clarify the difference of dv_{ds}/dt changes during the turn-on and turn-off process, it is necessary to analyze the relationship between $dv_{ds\text{-}on}/dt$ and $dv_{ds\text{-}off}/dt$ with temperature.

Differentiate Eqs. (15) and (16) with respect to temperature, respectively, to obtain Eqs. (17) and (18).

$$\frac{d^2v_{ds\text{-}on}}{dtdT} = \frac{1}{R_GC_{GD}}\frac{dV_{th}}{dT} - \frac{I_L}{R_GC_{GD}g_{fs}^2}\frac{dg_{fs}}{dT} \tag{17}$$

$$\frac{d^2v_{ds\text{-}off}}{dtdT} = \frac{1}{R_GC_{GD}}\frac{dV_{th}}{dT} - \frac{I_L}{R_GC_{GD}g_{fs}^2}\frac{dg_{fs}}{dT} \tag{18}$$

According to Eqs. (17) and (18), the temperature sensitivity coefficients of dv_{ds}/dt are the same during the turn-on and turn-off processes of SiC MOSFET. With the increase of temperature, the increase of dv_{ds}/dt during the turn-on process is the same as the decrease of dv_{ds}/dt during the turn-off process. The drain-source voltage waveforms of the switching process at different temperatures are obtained through double pulse test experiment, as shown in Fig. 6.

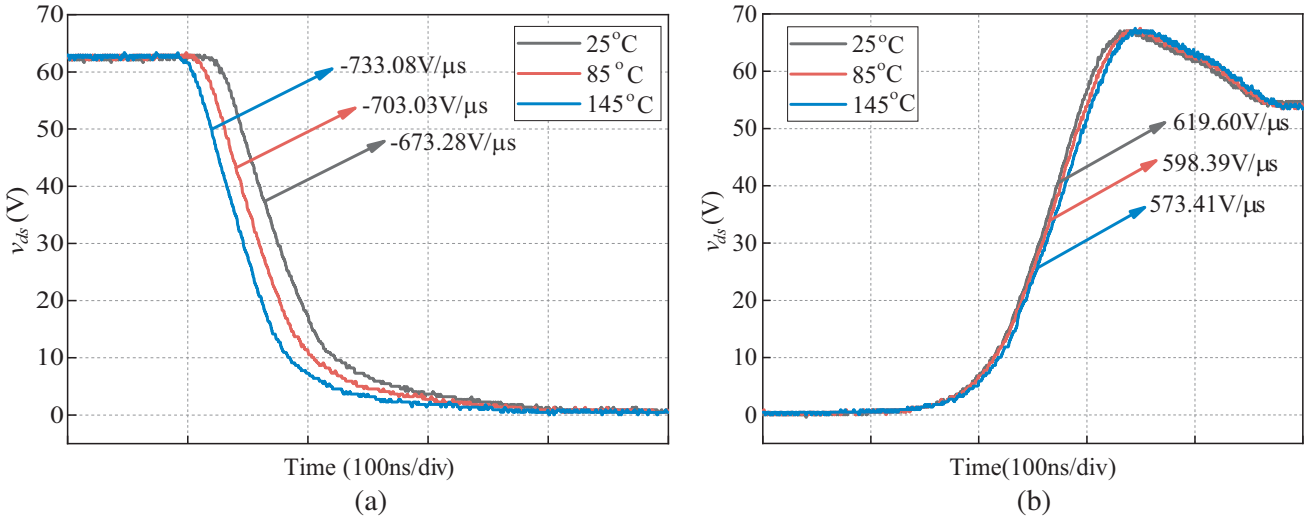

Figure 6. Drain-source voltage waveforms at different temperatures. (a) Turn-on, and (b) Turn-off.

It can be seen from the figure that with the increase of temperature, the falling rate of v_{ds} during the turn-on process of SiC MOSFET increases, and the rising rate of v_{ds} during the turn-off process decreases. When the temperature increases from 25°C to 145°C, $|dv_{ds}/dt|$ increases by 8.89% during the turn-on process and decreases by 7.45% during the turn-off process. Therefore, the temperature dependences of dv_{ds}/dt are almost the same during the turn-on and turn-off processes of SiC MOSFET. In general, the temperature change has almost no effect on the CM interference source.

2.2.2. Acquisition of Temperature Variation Characteristics of CM Interference Spectrum

The coupling path of the CM interference in the system is shown in Fig. 7 [3].

In Fig. 7, R_{line3} and L_{line3} are the resistance and inductance of the connecting line between C_F and SiC MOSFEFT, respectively. $V(s)$ is the frequency domain expression of the CM interference source $v_{ds}(t)$, and V_{CM} is the CM interference voltage. The drain-source voltage $v_{ds\text{-}on}(t)$ during the turn-on process, the drain-source voltage $v_{ds\text{-}off}(t)$ during the turn-off process [31], the corresponding

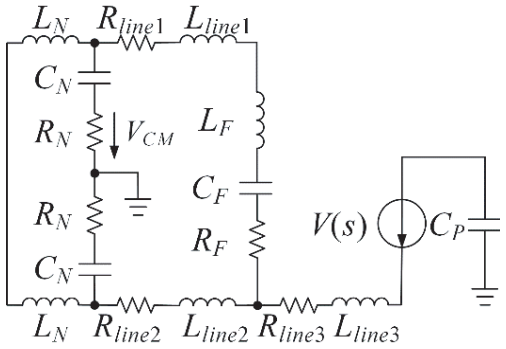

Figure 7. Coupling path of CM interference.

frequency domain expression, and the corresponding CM interference voltage are shown in Eqs. (19)–(24), respectively.

$$v_{ds\text{-}on}(t) = \left[V_{DC} - (L_S + L_D)\frac{di_{d\text{-}on}}{dt}\right] - \frac{dv_{ds\text{-}on}}{dt}t \quad (t_2 < t < t_3) \tag{19}$$

$$v_{ds\text{-}off}(t) = V_{miller} - V_{th} + \frac{dv_{ds\text{-}off}}{dt}t \quad (t_8 < t < t_9) \tag{20}$$

$$V_{ds\text{-}on}(s) = FFT\left[v_{ds\text{-}on}(t)\right] \tag{21}$$

$$V_{ds\text{-}off}(s) = FFT\left[v_{ds\text{-}off}(t)\right] \tag{22}$$

$$V_{CM\text{-}on}(s) = \frac{0.5R_N}{Z_6 + Z_{eq}}V_{ds\text{-}on}(s) \tag{23}$$

$$V_{CM\text{-}off}(s) = \frac{0.5R_N}{Z_6 + Z_{eq}}V_{ds\text{-}off}(s) \tag{24}$$

where $Z_6 = R_{c3} + j\omega L_{c3} + (1/j\omega C_P)$, $Z_{eq} = [Z_1(Z_1 + Z_2)(Z_3 + 2Z_4 + Z_5) + Z_4(Z_3 + Z_4 + Z_5)(2Z_1 + Z_2) + Z_1^2 Z_2]/(2Z_1 + Z_2)(Z_3 + 2Z_4 + Z_5) + 2Z_1 Z_2)$.

The CM interference voltage $V_{CM\text{-}ave}$ generated by the drain-source voltage during the SiC MOSFEFT switching process is shown in Eq. (25).

$$V_{CM\text{-}ave} = \frac{V_{CM\text{-}on} + V_{CM\text{-}off}}{2} \tag{25}$$

In summary, the DM interference voltage and CM interference voltage versus temperature are shown in Fig. 8.

It can be seen from the figure that the increase of temperature leads to increasing n_i and then decreasing ψ_B, which is further characterized by the decrease of V_{th} and the increase of g_{fs}. Under

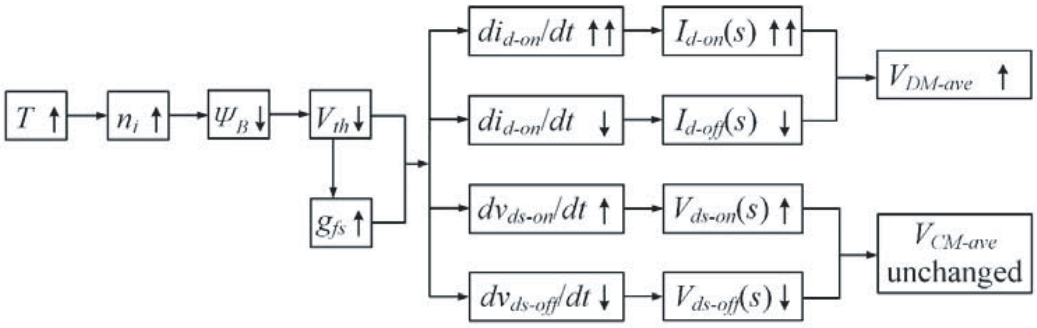

Figure 8. DM interference voltage and CM interference voltage versus temperature.

the common influence of V_{th} and g_{fs}, the temperature dependence of di_d/dt and the corresponding frequency domain expression $I_d(s)$ during the turn-on process are stronger than that of the turn-off process, and the temperature dependence of dv_{ds}/dt and corresponding frequency domain expression $V_{ds}(s)$ are the same as that of the turn-off process. Therefore, with the increase of temperature, the DM interference voltage in the system increases, and the CM interference voltage basically remains unchanged.

3. EXPERIMENTAL VERIFICATION AND ANALYSIS

3.1. Experimental Platform

To avoid inaccurate experimental results caused by external interference, a conducted EMI test platform is built in an electromagnetic shielding room. The schematic diagram and experimental platform are shown in Fig. 9 and Fig. 10, respectively. A buck converter composed of SiC MOSFET is taken as the research object to verify the temperature variation characteristics of conducted EMI in the system. SiC MOSFET 1 (T1) is used as the device under test, and SiC MOSFET 2 (T2) applies a negative gate voltage to turn it off and acts as a freewheeling diode to provide a path for the load current. A 490 µF thin film capacitor is paralleled on both sides of the high-power DC power supply to maintain voltage stability and provide the DC voltage V_{dc} to the converter through the LISN. A programmable DC power supply and signal generator are used to provide driving voltage and signal for the drive board, and the driving resistance is set to 20 Ω. An EMCIS EA-2100 EMI analyzer is used to separate the mixed interference signal into DM interference signal and CM interference signal. A SIGLENT SSA3032X PIUS spectrum analyzer is used to measure the interference signal output of the EMI analyzer, and a 40 dB attenuator is connected to the input end of the spectrum analyzer to ensure its safe operation.

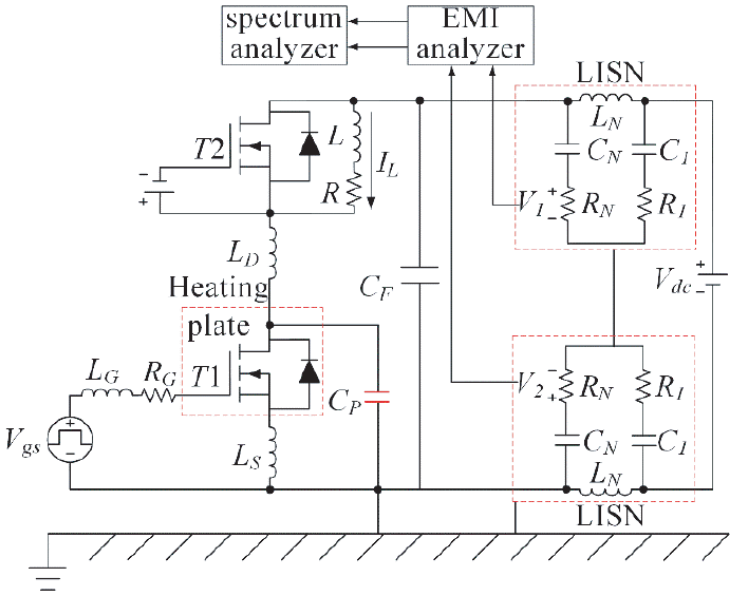

Figure 9. Schematic diagram of conducted EMI test.

3.2. Verification of Temperature Variation Characteristics of Conducted EMI Spectrum

The switching frequency of SiC MOSFET is set to 50 kHz, and the duty cycle is set to 50%. The working temperature of SiC MOSFET is controlled by the heating plate at 25°C, 85°C, and 145°C, respectively. When the heating plate reaches the preset working temperature, stabilize for another 5 minutes to ensure that the shell temperature is equal to the chip temperature. The interference signal measured in the circuit is generated by the drive board and the switching behavior of SiC MOSFET. To

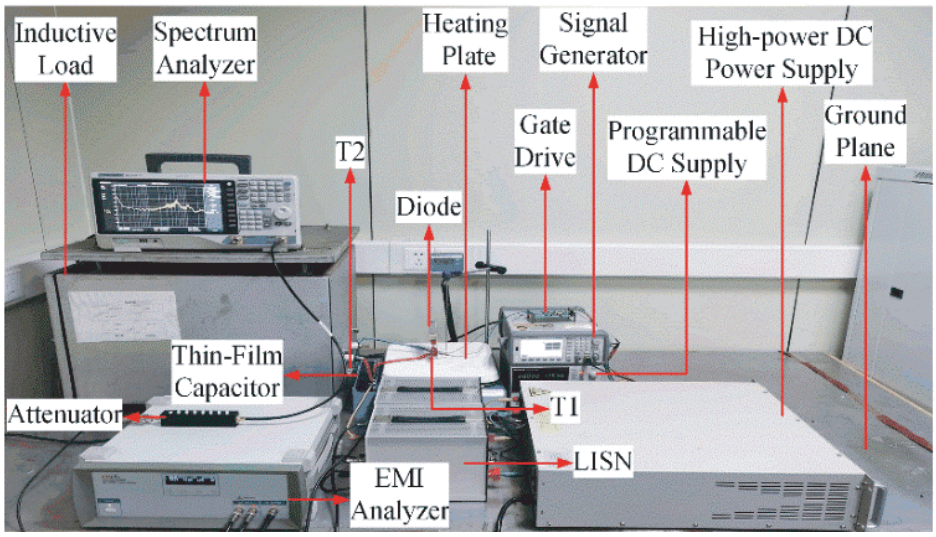

Figure 10. Experimental platform of conducted EMI test.

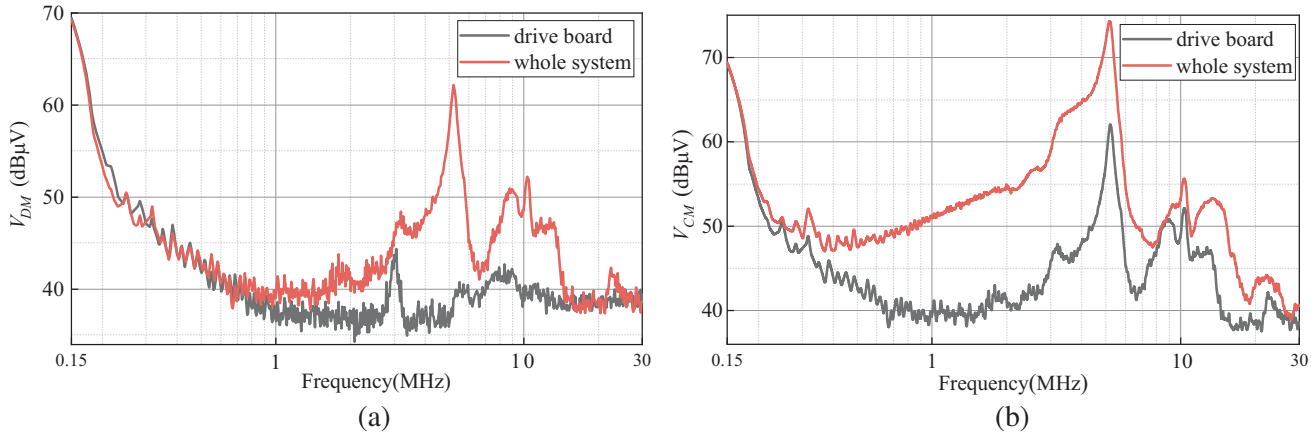

Figure 11. Conducted EMI spectrum generated by whole system working and only drive board working. (a) DM voltage, and (b) CM voltage.

obtain the interference signal generated only by the switching behavior of SiC MOSFET, it is necessary to eliminate the interference generated by the drive board. Firstly, the interference signal generated by the joint working of the drive board and SiC MOSFET is measured, and then the interference signal generated by only the working of the drive board is measured. The difference between the two is the interference signal generated by the switching behavior of SiC MOSFET. The conducted EMI spectrum generated by the working of the whole system and the working of only the drive board is shown in Fig. 11.

It can be seen from the figure that there is a big difference between the conducted EMI spectrum generated by the working of the whole system and the working of only the drive board. To obtain the conducted EMI signal generated only by the switching behavior of SiC MOSFET, the interference signal generated by the driver board must be eliminated.

To reduce the effect of device self-heating, SiC MOSFET works in 1A low current mode with short working time. The conducted EMI spectrum generated only by the switching behavior of SiC MOSFET at different temperatures is shown in Fig. 12.

In the range of conducted EMI frequency, according to Fig. 12(a), the DM voltage increases with the increase of the working temperature of SiC MOSFET. When the working temperature increases from

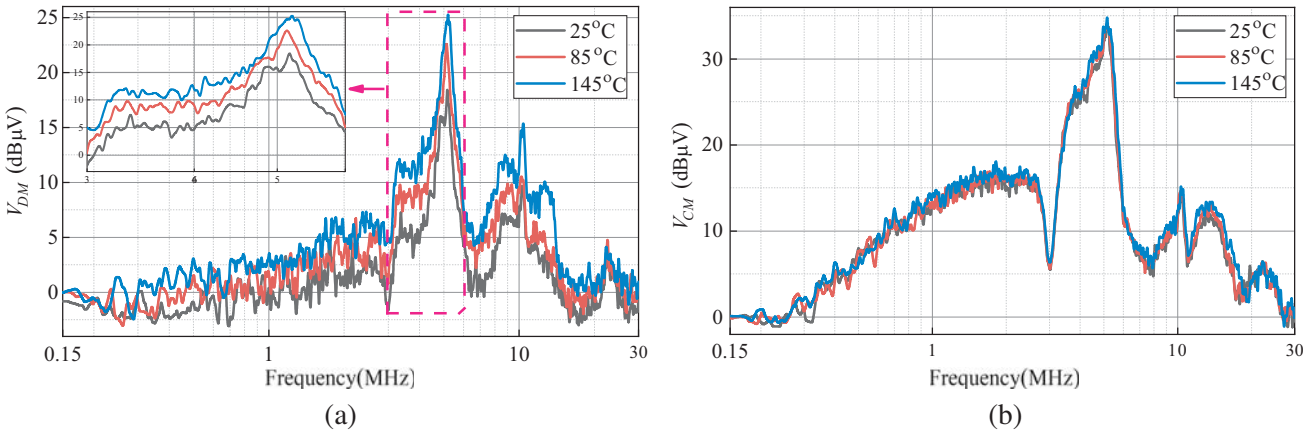

Figure 12. Conducted EMI spectrum generated by SiC MOSFET at different temperatures. (a) DM voltage, and (b) CM voltage.

25°C to 145°C, the peak value of DM voltage increases by 6.7 dBμV. According to Fig. 12(b), the CM voltage hardly changes with the increase of the working temperature. When the working temperature increases from 25°C to 145°C, the peak value of CM voltage changes less than 1.4 dBμV. Therefore, compared with the DM voltage which changes obviously with temperature, it can be considered that temperature has no effect on the CM voltage. In addition, both the DM voltage and CM voltage reach the peak at 5.1 MHz, which is related to the ringing frequency during the SiC MOSFET switching process.

3.3. Temperature Variation Characteristics of Peak Value of DM Voltage under Load Condition

When the working temperature of SiC MOSFET is 25°C, 55°C, 85°C, 115°C, and 145°C, the peak values of DM voltage under different load currents are extracted. Taking the peak values at 25°C as the reference, the relationship between the peak value change of DM voltage $V_{DM\text{-}peak}$ and temperature under different load currents is plotted, as shown in Fig. 13.

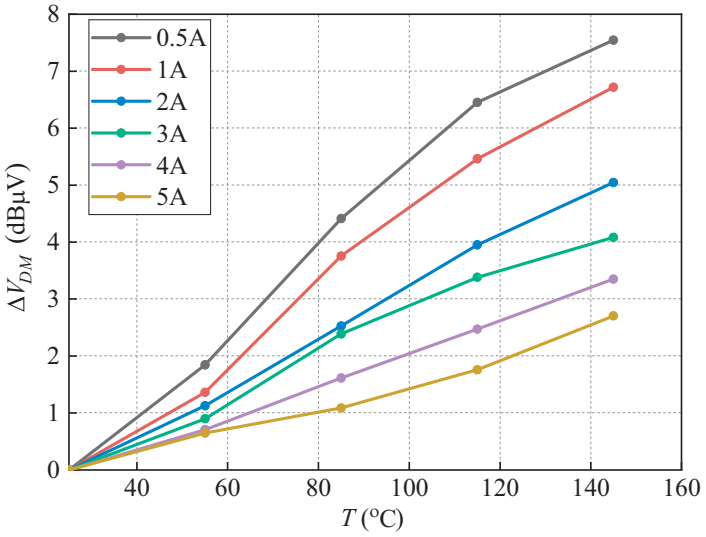

Figure 13. Relationship between peak value change of DM voltage and temperature under different load currents.

It can be seen from Fig. 13 that under different load currents, the peak value of DM voltage increases with the increase of temperature. When the working temperature increases from 25°C to 145°C, the $V_{DM-peak}$ is 7.5 dBμV at $I_L = 0.5$ A, and $V_{DM-peak}$ is 2.7 dBμV at $I_L = 5$ A. Therefore, the temperature dependence of the peak value of DM voltage decreases with the increase of load current. According to Eqs. (5) and (6), the temperature dependence of di_d/dt increases with the increase of load current during both the turn-on and turn-off processes. In the case of large load current, the temperature dependence of di_d/dt during the turn-off process will become non-negligible. Therefore, the temperature dependence of the DM voltage decreases with the increase of load current.

According to the EMC test standards, the product safety margin is mostly set to 6 dB. However, with the increase of temperature, the $V_{DM-peak}$ in the system will exceed 6 dB, which will lead to the EMC environment no longer meeting the standards and affecting the safe operation of the system and the surrounding equipment. Therefore, in the early stage of converter design, the temperature effect on the EMI in the system must be considered, and the safety margin should be appropriately increased to make the factory standards of the converter stricter so as to ensure that it also meets the EMC test standards even at the maximum junction temperature.

4. CONCLUSION

In this paper, by analyzing the temperature variation characteristics of the conducted EMI signals during the SiC MOSFET switching process, it is shown that the temperature dependence of the CM interference sources during the turn-on and turn-off processes are the same, while the temperature dependence of the DM interference source during the turn-on process is higher than that during the turn-off process. On this basis, combined with the coupling paths of conducted EMI in the buck converter system, the conclusion that the DM interference in the system increases and the CM interference almost remains unchanged with the increase of temperature is obtained. The conducted EMI test platform is built in the electromagnetic shielding room. The experimental results show that the DM interference in the system has a positive temperature dependence, and the dependence decreases with the increase of load current; the CM interference is almost unaffected by temperature. In practical applications, the increase in the junction temperature of the device will cause the EMI in the system to increase and may even exceed the maximum specified by the EMC standards. Therefore, the junction temperature effect on EMI in the system should be considered in the early stage of converter design.

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