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Optimization Technique for Lumped-Element LC Resonator Constructed on Multilayer Substrate

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Abstract—Parasitic effects in a lumped-element multilayer LC resonator are analyzed with an equivalent circuit. An optimization technique is proposed. With this technique, undesired influences of parasitic effects may be reduced. Meanwhile, some of the parasitic effects may be used for the size-reduction and performance improvement. A lumped-element multilayer LC resonator is used for demonstration. The optimized resonator outperforms the resonator before optimization in both performance and size. A multilayer filter composed of four LC resonators is used for verification. The measurement results agree very well with circuit results. The measured parasitic resonances are higher than the third harmonic frequency. These facts show the effectiveness of the proposed technique.

1. INTRODUCTION

In multilayer filter design, parasitic effects always have great influences on performance [1]. To reduce the influences of parasitic effects, EM simulation software is usually used [2]. Meanwhile, many useful structures and design methods have been proposed. In [3], spurious spikes suppressed Vertically-Interdigital-Capacitor (VIC) is proposed. By adding a via between interval fingers, influences of parasitic inductor are reduced, and operating bandwidth is extended. In [4], the shorted ends of the feeding line are realized by connecting the end to the vertical ground on the side rather than to the ground with vias because via may cause the parasitic effect at the millimeter-wave frequency band. In [5], a $\lambda_g/8$ short-ended transmission line is used to displace the lumped inductor because the lumped inductor introduces parasitic parameters in high frequencies.

Parasitic effects in a multilayer LC resonator result in multiple resonances, which makes the design procedure complex. In this paper, an optimization technique for multilayer LC resonator is proposed and discussed with equivalent circuits. This technique has two advantages. Firstly, the undesired influences of parasitic effects may be reduced, and the overall performance may be improved. Secondly, some parasitic effects may be used for the size-reduction. A multilayer LC resonator example is used to demonstrate the whole optimization process. The optimized resonator outperforms the resonator before optimization in both performance and size. A multilayer filter composed of four LC resonators is used for verification. The measurement results agree very well with desired results. The parasitic resonances are higher than the third harmonic frequency. These facts show the effectiveness of the proposed technique.

2. PROPOSED TECHNIQUE AND EXAMPLE

Take the LC resonator shown in Figure 1(a) as an example. The theoretical component values are $C_0 = 6.2\,\text{pF}$ and $L_0 = 1.4\,\text{nH}$. Figure 1(b) is the multilayer realization (initial layout), which is composed of a 1.4 nH half-turn inductor and a 6.2 pF Metal-Insulator-Metal (MIM) capacitor from [6].

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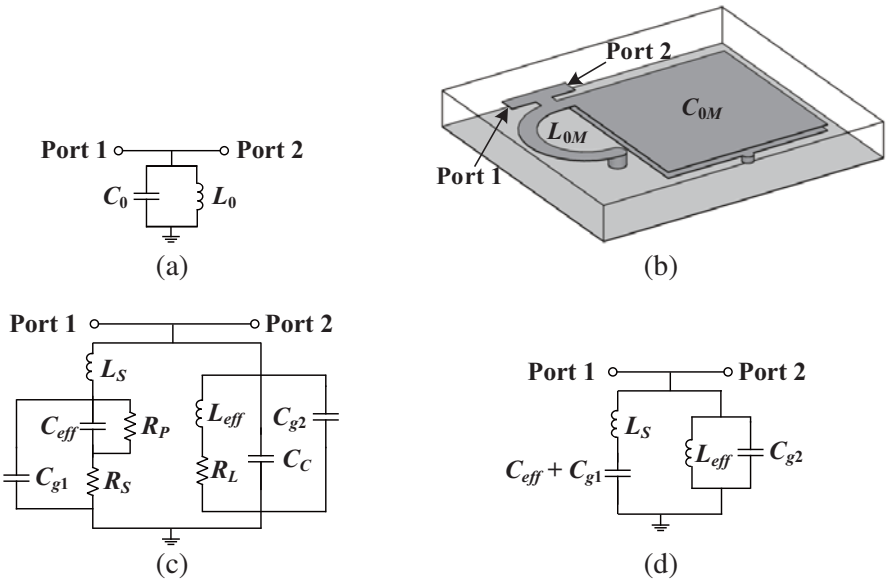

Figure 1. (a) LC resonator. (b) Initial multilayer layout. (c) Equivalent circuit of initial layout. (d) Simplified equivalent circuit.

Figure 1(c) shows the equivalent circuit of the initial layout, which is composed of the circuit models from [6]. C_{eff} and L_{eff} are effective capacitor and inductor, respectively. C_{g1} and L_S are parasitic components of C_{0M}. C_{g2} and C_C are parasitic components of L_{0M}. R_S and R_L represent conductor loss while R_P represents dielectric loss.

Ignoring resistors and small coupling capacitor C_C, Figure 1(c) can be simplified as Figure 1(d). According to data given in [6], $C_{eff} = C_0 = 6.2\,\text{pF}$, $C_{g1} = 0.1\,\text{pF}$, $L_S = 0.4\,\text{nH}$, $L_{eff} = L_0 = 1.4\,\text{nH}$, $C_{g2} = 0.15\,\text{pF}$.

The theoretical resonance frequency of initial layout is

$$f_0 = \frac{1}{2\pi\sqrt{C_0 L_0}} = 1.71\,\text{GHz} \tag{1}$$

But according to Figure 1(d), the initial layout has four resonance frequencies, namely:

$$f_1 = \frac{1}{\pi\sqrt{2S}} \tag{2}$$

$$f_2 = \frac{1}{2\pi\sqrt{L_S(C_{eff} + C_{g1})}} \tag{3}$$

$$f_3 = \frac{1}{2\pi\sqrt{L_{eff} C_{g2}}} \tag{4}$$

$$f_4 = \frac{\sqrt{S}}{2\pi\sqrt{L_{eff} C_{g2} L_S (C_{eff} + C_{g1})}} \tag{5}$$

where

$$S = \Delta + \sqrt{\Delta^2 - 4L_S (C_{eff} + C_{g1}) L_{eff} C_{g2}} \tag{6}$$

$$\Delta = L_S (C_{eff} + C_{g1}) + L_{eff} C_{g2} + L_{eff} (C_{eff} + C_{g1}) \tag{7}$$

In this example, $f_1 = 1.48\,\text{GHz}$, $f_2 = 3.17\,\text{GHz}$, $f_3 = 10.98\,\text{GHz}$, and $f_4 = 23.5\,\text{GHz}$.

f_1 is the usable resonance of the initial layout. f_2 and f_3 are self-resonances of C_{0M} and L_{0M}, respectively. f_4 may be ignored because it is very far away from usable resonance f_1.

According to Eq. (2), because of parasitic components, usable resonance f_1 is lower than the theoretical resonance frequency f_0. To increase f_1 to desired resonance frequency, the sizes of C_{0M} and L_{0M} should be decreased, which may lead to size-reduction. In other words, parasitic components may be used for the size-reduction.

According to Figure 1(d), there are several parasitic components. But only some of them may be tuned easily, like L_S (parasitic inductor of C_{0M}) and C_{g2} (parasitic grounding capacitor of L_{0M}).

Self-resonance of C_{0M} (namely f_2) results in a Zero, which has a great influence on performance. According to Eq. (3), to move this Zero to high-frequency end, L_S should be as small as possible. To this end, we may increase the diameter of via or use multiple vias. Therefore, Step 1 of the proposed technique is to decrease the parasitic inductor of multilayer capacitor.

Self-resonance of L_{0M} (namely f_3) does not result in a Pole or Zero. According to Eq. (4), it is very far away from usable resonance f_1, so we may make full use of it for the size-reduction. Parasitic capacitor C_{g2} may be tuned by controlling the distance between metal strips and ground. Therefore, Step 2 of the proposed technique is to increase the parasitic capacitor of multilayer capacitor appropriately.

Step 3 is to decrease multilayer components for desired resonance frequency. Both C_{0M} and L_{0M} may be tuned in this step. But C_{0M} is a good candidate because decreasing C_{0M} may move the Zero to high-frequency end further.

Figure 2 shows a flowchart of the proposed technique. Step 2 and Step 3 may be repeated several times to try different parasitic components. Fine tunings may be performed for accurate resonance frequency.

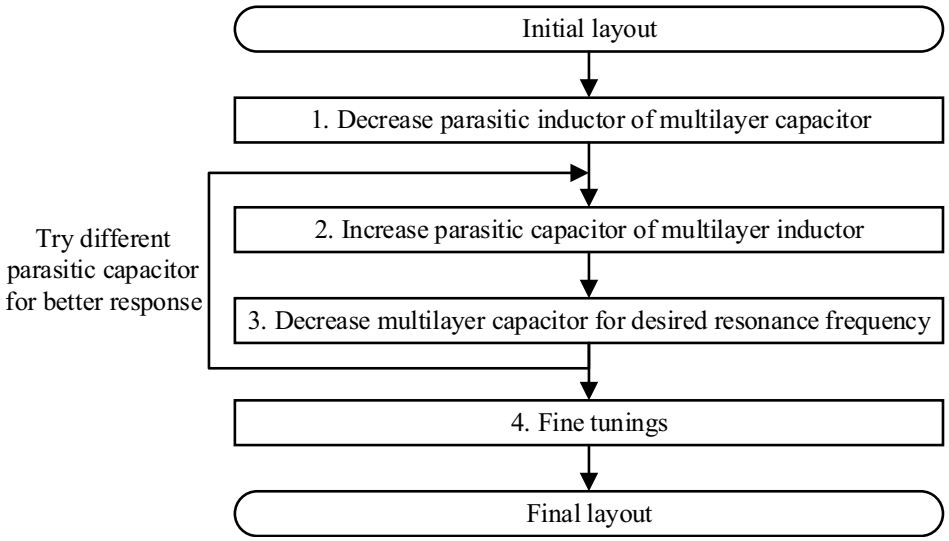

Figure 2. Flowchart of proposed optimization technique.

3. LC RESONATOR OPTIMIZATION EXAMPLE

The initial layout shown in Figure 1(b) is optimized with the proposed technique. Figure 3 shows the EM simulation results after each step during optimization. The detailed data are shown in Table 1.

Figure 3(a) compares the frequency responses of the initial layout and LC resonant circuit. Differences between them may be easily observed. The usable resonance frequency of the initial layout is about 1.48 GHz rather than predicted 1.71 GHz. An undesired Zero is observed at about 3.15 GHz. The size of the initial layout is about 3.4 mm $\times$ 4.2 mm $\times$ 0.2 mm or $6.38 \times 10^{-6}\lambda_g$.

Figure 3(b) shows the responses after Step 1. In this step, the via of C_{0M} is removed for less parasitic inductor [7]. Meanwhile, the bottom plate of MIM capacitor is removed. GND is used as the other plate. Because parasitic inductor is decreased, both usable resonance and Zero are increased. The Zero is increased from 3.15 GHz to 4.2 GHz.

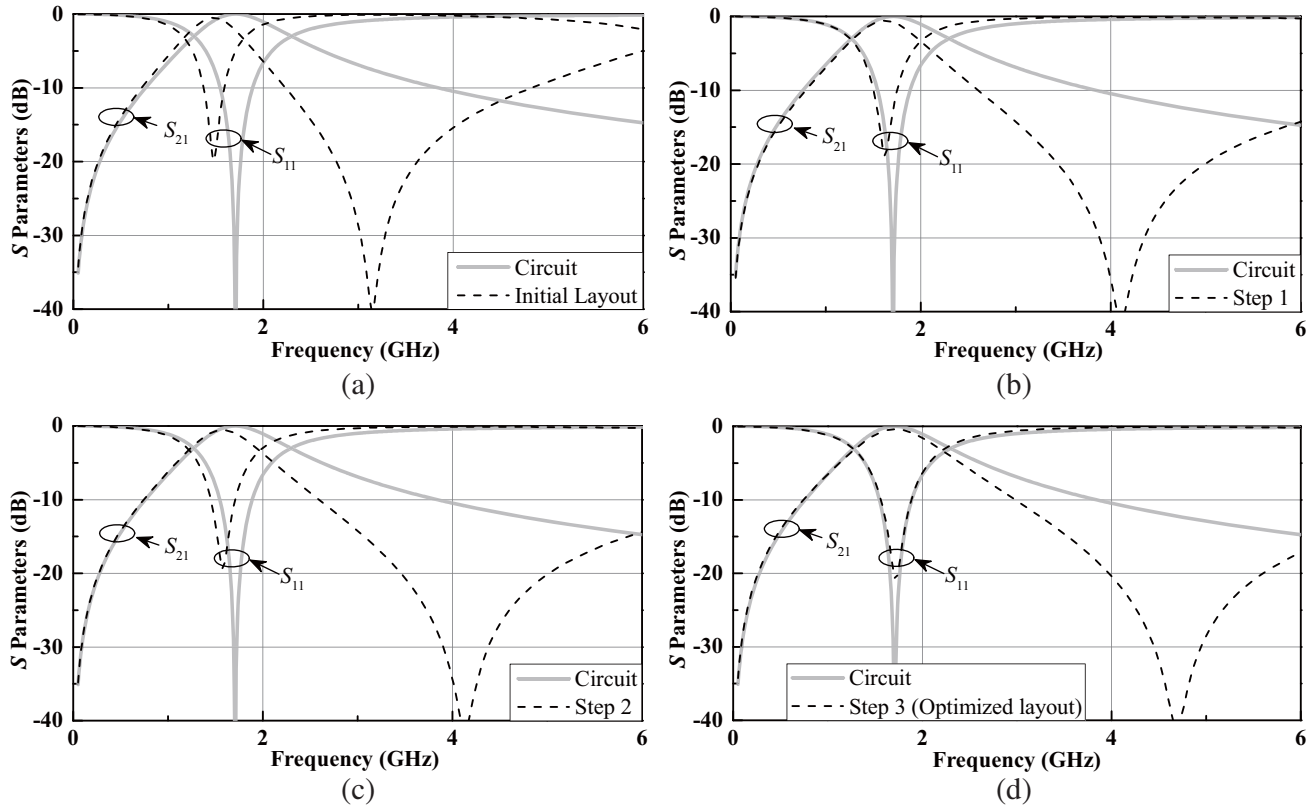

Figure 3. EM simulation results during optimization. (a) Before optimization. (b) After Step 1. (c) After Step 2. (d) After Step 3 (final results).

Table 1. Detailed data of LC resonator optimization example.

	Usable resonance (GHz)	Undesired Zero (GHz)	Size ($\times 10^{-6}\lambda_g$)
Circuit	1.71	-	6.38
Initial layout	1.48	3.15	-
Step 1	1.63	4.20	-
Step 2	1.51	4.19	-
Step 3 (Optimized layout)	1.71	4.70	4.96

Figure 3(c) shows the responses after Step 2. In this step, distance between L_{0M} and GND is decreased by 7.2 mil. Because the parasitic grounding capacitor is increased, the usable resonance is decreased from 1.63 GHz to 1.51 GHz. The undesired Zero is almost not influenced in this step.

Figure 3(d) shows the responses after Step 3. In this step, the size of C_{0M} is decreased from 101 mil to 87 mil. The usable resonance is accurate. The Zero is increased to about 4.70 GHz. Its influences on performance are reduced further. The response of the optimized layout outperforms that of the initial layout. The size of the optimized layout is about 3 mm $\times$ 3.7 mm $\times$ 0.2 mm or $4.96 \times 10^{-6}\lambda_g$. Compared to initial layout, the size of the optimized layout is reduced by about 23%.

4. FILTER DESIGN AND EXPERIMENTAL VERIFICATION

A third-order elliptic filter operating at 800 MHz with 260 MHz 3 dB-bandwidth is used for verification. The filter circuit is shown in Figure 4(a). It is composed of four LC resonators, which are noted as r_1, r_2,

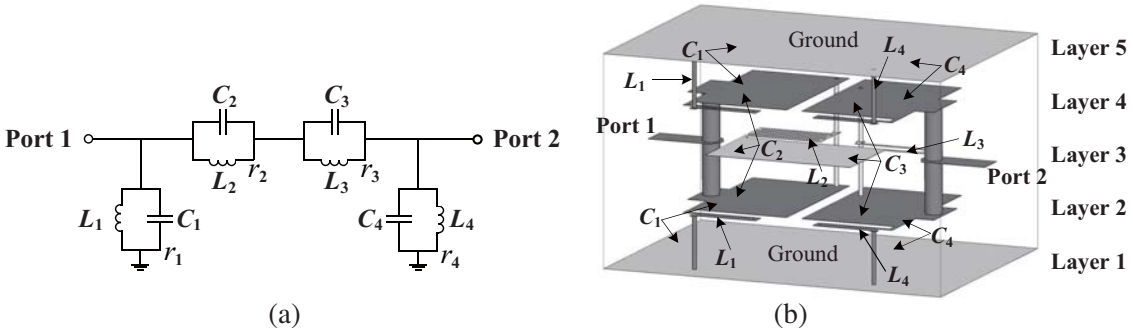

Figure 4. Filter design. (a) Filter circuit. (b) Proposed physical layout.

r_3, and r_4. The theoretical component values are $C_1 = C_4 = 12.0\,\text{pF}$, $L_1 = L_4 = 3.30\,\text{nH}$, $C_2 = 6.08\,\text{pF}$, $L_2 = 12.3\,\text{nH}$, $C_3 = 3.23\,\text{pF}$, and $L_3 = 6.51\,\text{nH}$.

r_2 (as well as r_3) is a parallel resonator. Its input impedance at resonance frequency is infinite. As a result, it introduces a transmission Zero at its resonance frequency [8]. In this filter, Zeros introduced by r_2 and r_3 are located at 582 MHz and 1.1 GHz, respectively. They can be separately controlled by tuning corresponding resonant frequency.

Figure 4(b) is the proposed physical layout. C_1 (as well as C_4) is the capacitance between layers 1 and 2, and the capacitance between layers 4 and 5. C_2 (as well as C_3) is a three-layer VIC located on layers 2, 3, and 4. Diameter of via in VIC is increased for less parasitic inductor. Inductors are composed of a meander strip line and a via [9]. L_1 (as well as L_4) is composed of two sub-inductors. Each sub-inductor is composed of a meander strip line and a metalized grounding via. L_2 (as well as L_3) is composed of a meander strip line on layer 3 and a metalized via. These vias are a part of an inductor. Their diameters are decreased to increase the inductance. The meander strip lines are placed close to the grounds for larger parasitic capacitors.

Ports are designed as 50 Ω striplines [9]. A stripline-microstrip transition is used to make this model easy to connect with the measurement instruments. To achieve field confinement, a via fence that connects two grounds is adopted (not illustrated in figure). It surrounds the whole model except for two ports.

Due to the limitation of experiment conditions, PCB technology was used to fabricate the prototype. The selected substrate is 1 mm-thickness Rogers 5880 ($\epsilon_r = 2.2$). All layers are manually stacked and fixed. The size of the core, namely the structure shown in Figure 4(b), is about $1.94 \times 10^{-4}\lambda_g$. A calibrated Agilent 8720ET Vector Network Analyzer is used for the measurement.

In the proposed layout, all resonators are designed and optimized with the proposed optimization technique. Figure 5 shows the EM simulation results of r_2. With the proposed technique, the frequency

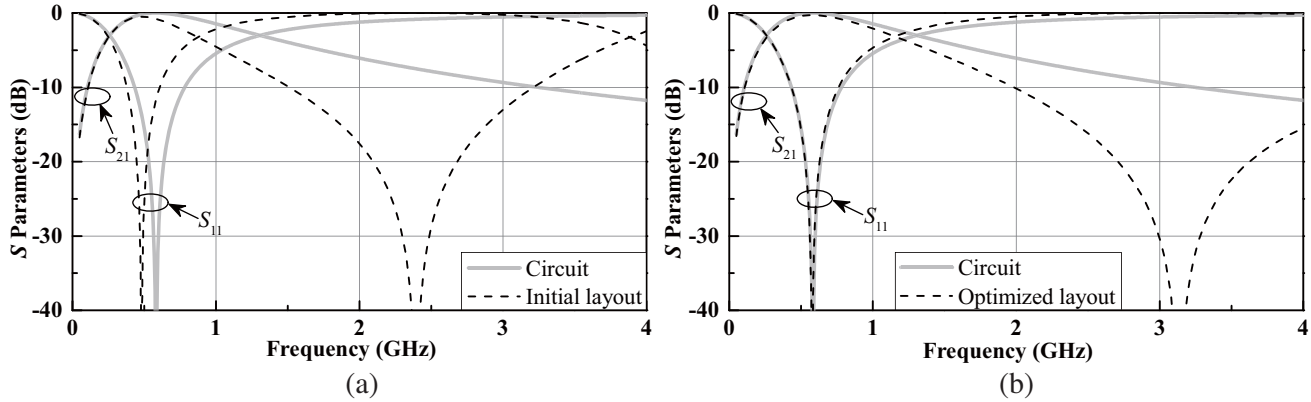

Figure 5. EM simulation results of resonator r_2. (a) Before optimization. (b) After optimization.

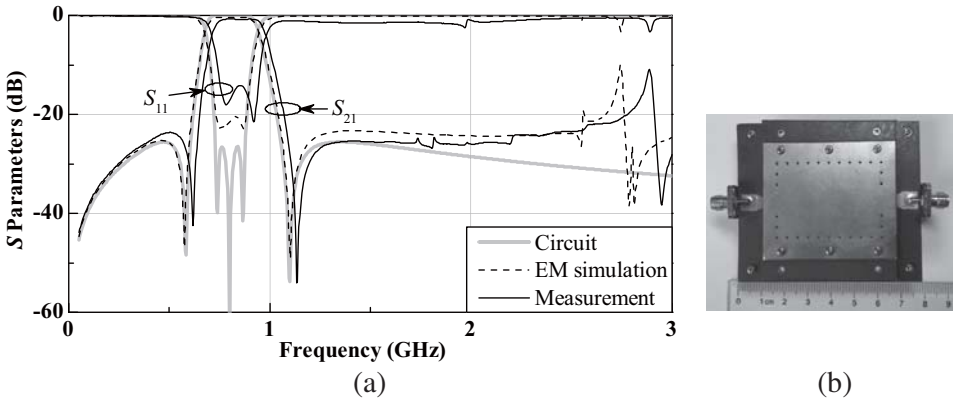

Figure 6. Experimental prototype. (a) Measurement results and simulation results. (b) Photograph.

responses of r_2 are improved obviously. The undesired Zero is increased by about 0.8 GHz. Meanwhile, the size of r_2 is reduced by about 11%.

Figure 6(a) shows the results of the prototype while Figure 6(b) shows the photograph. In Figure 6(a), circuit results, EM simulation results, and measurement results are compared. Besides the slight frequency shift, the measurement results agree very well with circuit results and simulation results. The measured central frequency and 3 dB bandwidth are 835 MHz and 263 MHz, respectively. Those of circuit results are 800 MHz and 261 MHz, respectively. The measured insertion loss and return loss are about 0.75 dB and 16 dB, respectively. Those of circuit results are about 0.4 dB and 20 dB, respectively. The differences between simulation and measurement results may be caused by the stacking shift. Parasitic resonances of the filter are higher than the third harmonic frequency.

5. CONCLUSION

Parasitic effects of lumped-element multilayer LC resonator are analyzed in detail with the equivalent circuit. An optimization technique is proposed. With this technique, the performance of multilayer LC resonator may be improve,d and the size of multilayer LC resonator may be reduced. A multilayer LC resonator is used for demonstration. The optimized resonator outperforms the resonator before optimization in both performance and size. A multilayer filter composed of four LC resonators is used for verification. Good agreements between measurement results and circuit results can be observed. The parasitic resonances are higher than the third harmonic frequency. These facts show the effectiveness of the proposed technique.

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