

A UWB Dual Band-Notched On-Chip Antenna and Its Equivalent Circuit Model

Sanjukta Mandal*, Sujit K. Mandal, Ashis K. Mal, and Rajat Mahapatra

Abstract—This paper presents a CPW-fed, UWB-extended bandwidth, dual band-notched on-chip antenna with its equivalent circuit model. The UWB-extended bandwidth is realized by truncating the bottom corners of a rectangular patch radiator while a 90°-rotated ‘C’-shaped slot in the patch and a ‘U’-shaped slot in the feedline are used to achieve two notch bands for mitigating the signal interference in the frequency bands of 5.15 to 5.925 GHz and 7.9 to 8.8 GHz. Based on the fundamental theory, different parasitic as well as distributed circuit parameters associated with the designed on-chip antenna are extracted, and then the corresponding equivalent circuit model is configured from them. The resultant circuit is validated with the well approved full-wave electromagnetic simulation result and is found in close approximation with each other.

1. INTRODUCTION

In the recent past, on-chip antenna (OCA) has been found to be suitable for integrating a complete system on a single chip, known as system-on-chip (SoC). It helps to transmit data over the internet of things (IoT) based network without human intervention [1]. The traditional off-chip antennas are normally kept outside the IC chip owing to their large volume. Consequently, bond wires are needed to connect the integrated circuits (ICs). The introduction of OCAs in the system chip extrudes the need of such bond wires which have several limitations. For example, they possess higher propagation delay, consume additional space, and apparently bring significant power loss. In this regard, on-chip antenna is going to be an alternative option for the traditional off-chip counterparts of an IC module. The OCA with UWB characteristics is useful for different applications like short-range radar [2], intra/inter-chip communication [3], and high-speed data communication [4]. However, designing such UWB OCAs with a stable radiation pattern throughout the entire operating band and satisfactory time-domain characteristics is a challenging task.

Moreover, interferences from the existing narrowband licensed spectra put forward a serious matter of concern to the UWB antenna designers. The use of multiple band reject filters to mitigate such interferential effects increases the circuit complexity and system cost. On the other hand, such band rejection property can be obtained by incorporating band notch functionality within the UWB antenna itself. This can be achieved by employing several techniques like defected ground structure (DGS) [5, 6], slots in the radiating patch [7–10] and feedline [11], slit on the radiator [12], parasitic strips above the ground plane [13], split-ring resonator (SRR) [14], capacitively-loaded loop (CLL) resonators [15], etc. The incorporation of the slot is the preferable option getting notch characteristics for its simple design implementation step. Antennas with single [6–10], dual [16–18], triple [15, 19], and quad [20, 21] notch bands by using different combinations of various slots have been reported in the recent decades. Researchers working in this domain are now aiming to extend the antenna’s operating bandwidth beyond the UWB region to cope with today’s modern high-speed data communication [22]. To achieve

Received 26 July 2022, Accepted 18 October 2022, Scheduled 25 October 2022

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this target, an inverted T-shaped notch is introduced in the ground plane in [23], and a pair of L-shaped slots in the patch, an E-shaped step-impedance slot resonator in the feedline, and a pair of L-shaped conductor-backed plane in the ground are incorporated in [24].

However, the above-mentioned conventional methods of introducing notch functionality are not suitable in IC environment. For example, to realize DGS, defects are created by etching slots in the ground plane of the microstrip fed antenna. In contrast, microstrip feeding is consciously avoided for designing the OCAs as the ground layer below the substrate may adversely affect other circuit components designed in the silicon wafer, and if any of the intermediate metal layers available in the CMOS process is chosen as the ground plane, it causes inefficient radiation due to the formation of the image current for the minimum separation between the patch and the ground plane. So, the incorporation of slots in the radiating patch or feedline of an OCA is the optimum solution to achieve notch functionality.

Since the era of on-chip antenna has started a few years back, prior knowledge about the equivalent circuit configuration of the antenna is limited. Though various approaches like numerical techniques, curve fitting, and empirical formulae have been reported, so far to model an on-chip inductor [25, 26], the on-chip antenna's equivalent circuit model by considering its physical geometry is rarely found. This article enlightens the physical insight into each equivalent circuit component in terms of the corresponding antenna geometry and its configuration in the equivalent circuit model. Therefore, this article will be helpful for identifying the critical design parameters and achieve the targeted antenna characteristics in an efficient, time-saving way by their proper tuning. To illustrate the concept, taking a reference UWB antenna on silicon, two band-notched characteristics are realized first. Then, analytically, an equivalent circuit model for the reference UWB on-chip antenna is constructed with the concepts of fundamental physics of the antenna geometry. Finally, using input impedance characteristics and iterative method, the different circuit components associated with the two notched bands of the proposed antenna have been extracted.

2. ANTENNA DESIGN AND ANALYSIS

The layered view of the antenna is depicted in Fig. 1. A monopole antenna is designed on 675 μm thick silicon wafer ($\rho = 8 \text{ k}\Omega\text{-cm}$) having dielectric constant (ϵ_r) of 11.8 and dielectric loss tangent ($\tan \delta$) of 0.01. The radiating patch is made of a 2 μm thick aluminium (Al) layer. DC magnetron sputtering is used to deposit the metal as a top layer. In between the silicon substrate and Al layer, a 2 μm thick SiO_2 layer ($\epsilon_r = 4$) is used as an insulating layer.

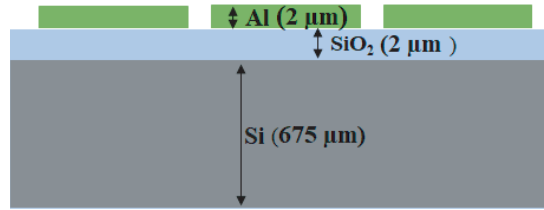


Figure 1. Layered view of the antenna.

2.1. UWB Reference Antenna Design

The top view of the basic UWB antenna is shown in Fig. 2(a). The antenna size is $8.8 \times 8.2 \text{ mm}^2$. The rectangular radiating patch with truncated bottom corners is used to achieve wideband characteristics. This corner truncation approach causes multiple reflections of the surface current from the edged corners, thus helps operating bandwidth to extend beyond the specified UWB range (3.1 to 10.6 GHz). Co-planar waveguide feeding technique is chosen for exciting the on-chip antenna as only one metal mask is required to realize this whole antenna structure. It reduces both manufacturing time and cost. The simulation

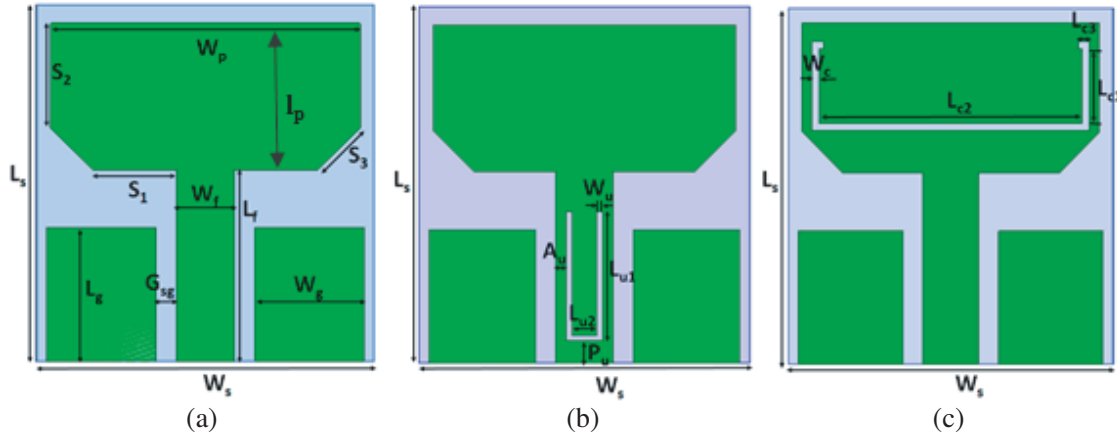


Figure 2. Top view of (a) UWB reference monopole on-chip antenna, where $L_s = 8.8$ mm, $W_s = 8.2$ mm, $L_g = 3.3$ mm, $W_g = 2.64$ mm, $G_{sg} = 0.51$ mm, $L_f = 4.73$ mm, $W_f = 1.4$ mm, $S_1 = 2.03$ mm, $S_2 = 2.7$ mm, $S_3 = 1.44$ mm, and $w_p = 7.5$ mm, $l_p = 3.72$ mm; (b) Incorporation of a ‘U’ shaped slot in the feedline to mitigate interference from ITU-8 band, where $L_{u1} = 3.355$ mm, $L_{u2} = 0.62$ mm, $P_u = 0.55$ mm, $A_u = 0.25$ mm, and $W_u = 0.14$ mm; (c) Incorporation of a 90°-rotated ‘C’ shaped slot in the radiating patch to mitigate interference from WLAN and DSRC band, where $L_{c1} = 1.84$ mm, $L_{c2} = 6.64$ mm, $L_{c3} = 0.28$ mm, and $W_c = 0.18$ mm.

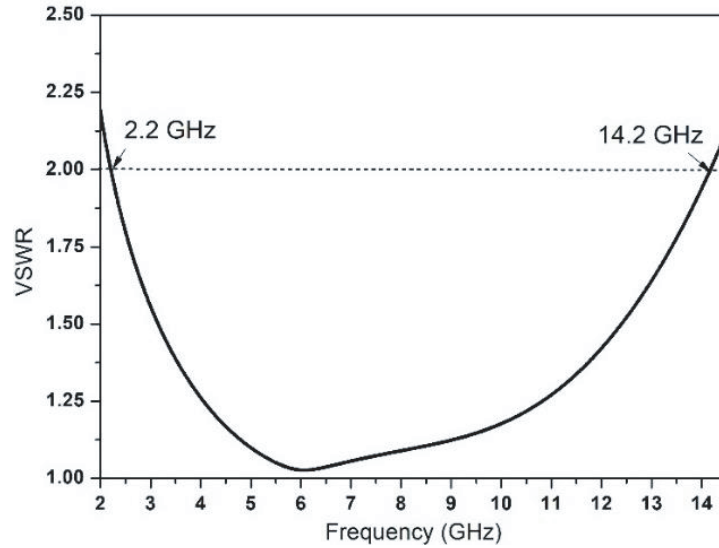


Figure 3. VSWR characteristic of the UWB monopole on-chip antenna.

is carried on using FEM-based EM simulator HFSS v17. VSWR characteristic of the reference antenna is shown in Fig. 3. The antenna achieves $VSWR \leq 2$ for the frequencies ranging from 2.2 to 14.2 GHz.

2.2. UWB Dual Band-Notched Antenna Design

Two slots are incorporated to include notch functionality in the above-mentioned reference UWB antenna. These slots cause confinement of the EM field around them at their corresponding design frequency, and thereby restrict the radiation from the antenna at those frequencies. The effect of the length and width of the two slots on the targeted rejection bands are discussed in the following subsections.

2.2.1. Effect of ‘U’ Shaped Slot in Feedline

To remove all the possibilities of the interference with ITU-8 band (7.9–8.8 GHz) dedicated for satellite communication application, a ‘U’-shaped slot is incorporated in the feedline as depicted in Fig. 2(b). Two main parameters like total slot length (L_{s1}) and slot width (W_u) that affect the position and bandwidth of the targeted notched band are parametrically optimized to produce desired outcomes. The total slot length is calculated using the following equation;

$$L_{s1} = 2L_{u1} + L_{u2} + 2W_u. \quad (1)$$

The effect of L_{s1} variation on the notched band is shown in Fig. 4(a). It is observed that, with the increment of L_{s1} , the notch band is shifted to the left-hand side. This phenomenon is quite expected as we know that the frequency is inversely proportional to the length. On the contrary, W_u determines the position of the notched band as well as the peak of the band as depicted in Fig. 4(b).

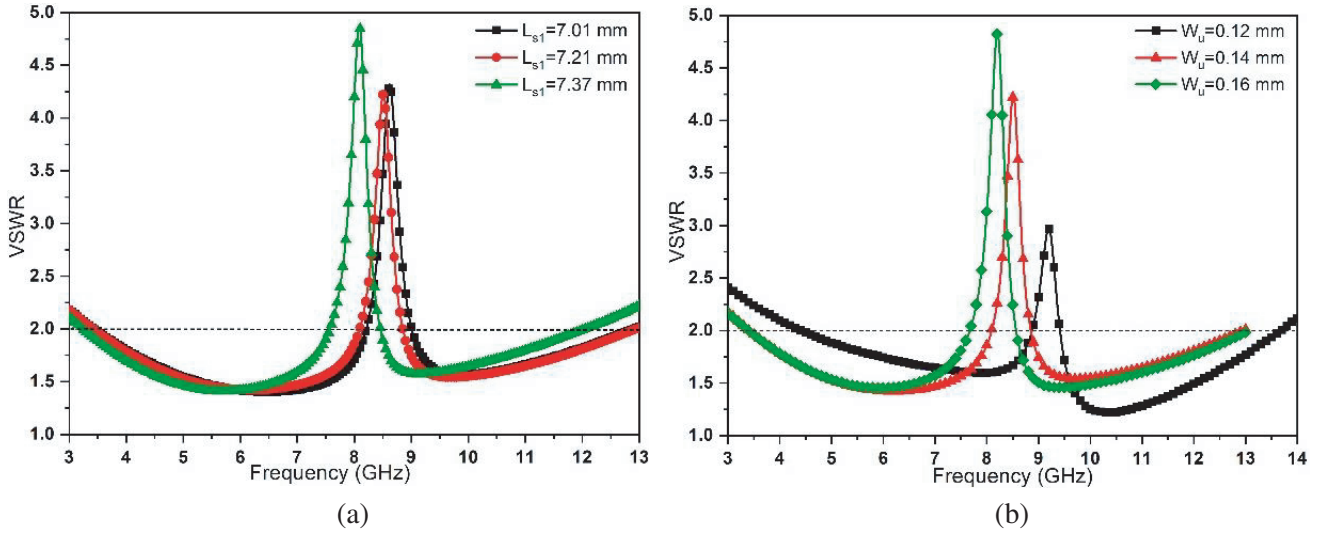


Figure 4. VSWR characteristics for different (a) L_{s1} and (b) W_u values of the ‘U’ shaped slot.

2.2.2. Effect of Rotated ‘C’-Shaped Slot in the Radiating Patch

This section presents the effect of the ‘C’-shaped slot rotated by 90° as shown in Fig. 2(c) on the performance of the notched bands namely wireless local area network (WLAN) band with operating frequency range of 5.15 GHz to 5.825 GHz and dedicated short range communication (DSRC) band with operating frequency range of 5.85 GHz to 5.925 GHz. The two critical parameters like total slot length L_{s2} and slot width W_c are parametrically optimized to obtain the best possible result. L_{s2} is calculated using the following equation;

$$L_{s2} = 2L_{c1} + L_{c2} + 2L_{c3} + 2W_c. \quad (2)$$

Figure 5(a) shows the effect of the variation of L_{s2} from 9.76 mm to 11.16 mm on the position of the notched band. The notch band shifts to the left side with the increment of L_{s2} , which is as per expectation. Fig. 5(b) shows the VSWR characteristics of the antenna for different values of W_c . It is seen that the bandwidth and centre frequency of the notched band vary slightly with the variation of W_c . So, it can be concluded that the length of the slot determines the centre frequency of the notched band. At the same time, the width of the slot is another vital parameter to determine the peak and frequency range of the notched band.

2.2.3. Proposed Antenna

Finally, in the proposed antenna structure, as shown in Fig. 6(a), both rotated ‘C’-shaped slot in the radiating patch and ‘U’-shaped slot in the feedline are incorporated to remove the interferential effect

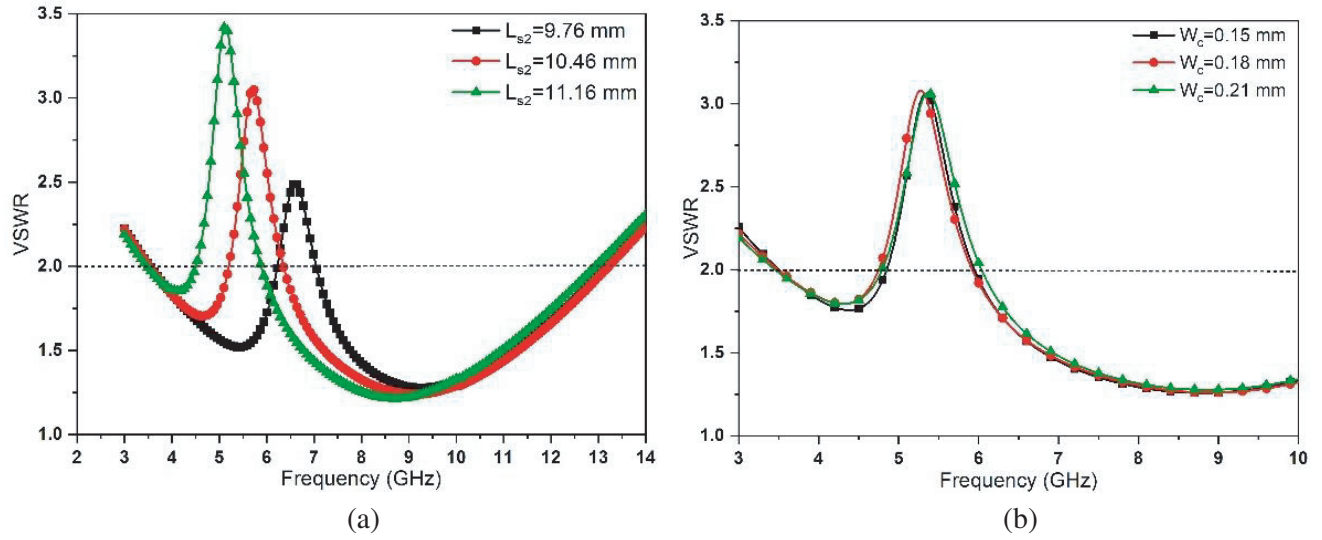


Figure 5. VSWR characteristics for different (a) L_{s2} and (b) W_c values of the ‘C’ shaped slot.

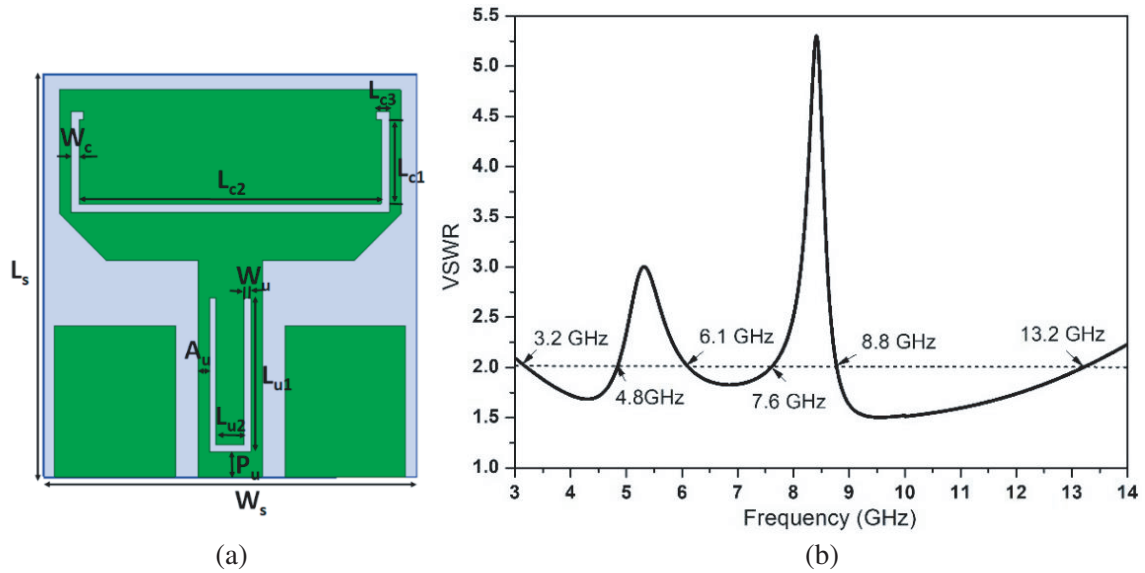


Figure 6. Proposed UWB dual band-notched antenna's (a) schematic view and (b) VSWR characteristic.

caused by WLAN, DSRC, and ITU-8 band. The optimized designed parameters are given as follows: $L_{u1} = 3.355$ mm, $L_{u2} = 0.62$ mm, $P_u = 0.55$ mm, $A_u = 0.25$ mm and $W_u = 0.14$ mm, $L_{c1} = 1.84$ mm, $L_{c2} = 6.64$ mm, $L_{c3} = 0.28$ mm, and $W_c = 0.18$ mm. From the VSWR characteristic of the antenna as shown in Fig. 6(b), it is observed that the proposed antenna covers 3.2 to 13.2 GHz band along with the two notches starting from 4.8 to 6.1 GHz and 7.6 to 8.8 GHz, respectively. It is also noticed that the required slot length to achieve the notch characteristics is approximately half of the guided wavelength ($\lambda_g/2$) corresponding to the desired centre frequency f_c .

3. ANTENNA CHARACTERISTICS

This section presents both frequency-domain and time-domain analyses of the proposed antenna. Frequency-domain parameters like gain, radiation pattern, and surface current distribution along with the time-domain parameters like S_{21} and group delay are depicted in this section. Fig. 7 compares gain of the proposed antenna with the reference UWB antenna. For the UWB antenna, the gain monotonically increases with the increment of the frequency, whereas the gain of the proposed antenna decreases sharply at the notched bands. The proposed antenna achieves a maximum gain of -3.52 dBi.

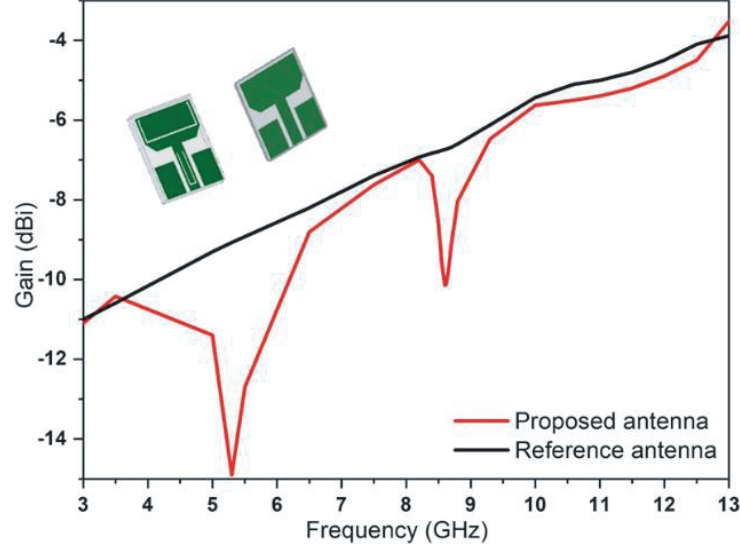


Figure 7. Gain comparison of the proposed antenna with the reference UWB antenna.

Figure 8 shows co-pol and cross-pol components of the radiation pattern in both H plane and E plane at four different frequencies, 3.5 GHz, 5.5 GHz, 8.4 GHz, and 10, GHz lying in the UWB range. In H plane, the co-pol component is omnidirectional and the cross-pol component bidirectional, whereas co- and cross-pol components in E plane are bidirectional and omnidirectional, respectively. A stable pattern and a good separation between co- and cross-pol components are observed throughout the operating band.

Figure 9 depicts surface current distribution of the proposed antenna at centre frequencies of two notched bands such as 5.45 GHz and 8.4 GHz. It is seen that most of the current is confined within the ‘C’-shaped slot at 5.45 GHz, which results in notching of the WLAN and DSRC band. On the contrary, at 8.4 GHz, most of the current is concentrated within the ‘U’-shaped slot, which ensures ITU-8 band notching happen.

Group delay and S_{21} are the two crucial time-domain parameters of a UWB antenna. For performing the time domain analysis, two similar designed antennas are placed at their far-field distance (here, they are placed 60 mm apart). Figs. 10(a) and (b) depict group delay (left side) and S_{21} (right side) characteristics of the antenna in face to face and side by side configurations, respectively. It is observed that the group delays of the proposed antenna in both arrangements are almost constant (variation is less than 0.5 ns) throughout the operating band except at the notch bands. As group delay is defined as a derivative of the far-field phase with respect to the operating frequency, constant group delay indicates a linear variation of the antenna phase with frequency. This phenomenon confirms distortion-less pulse transmission by the proposed antenna.

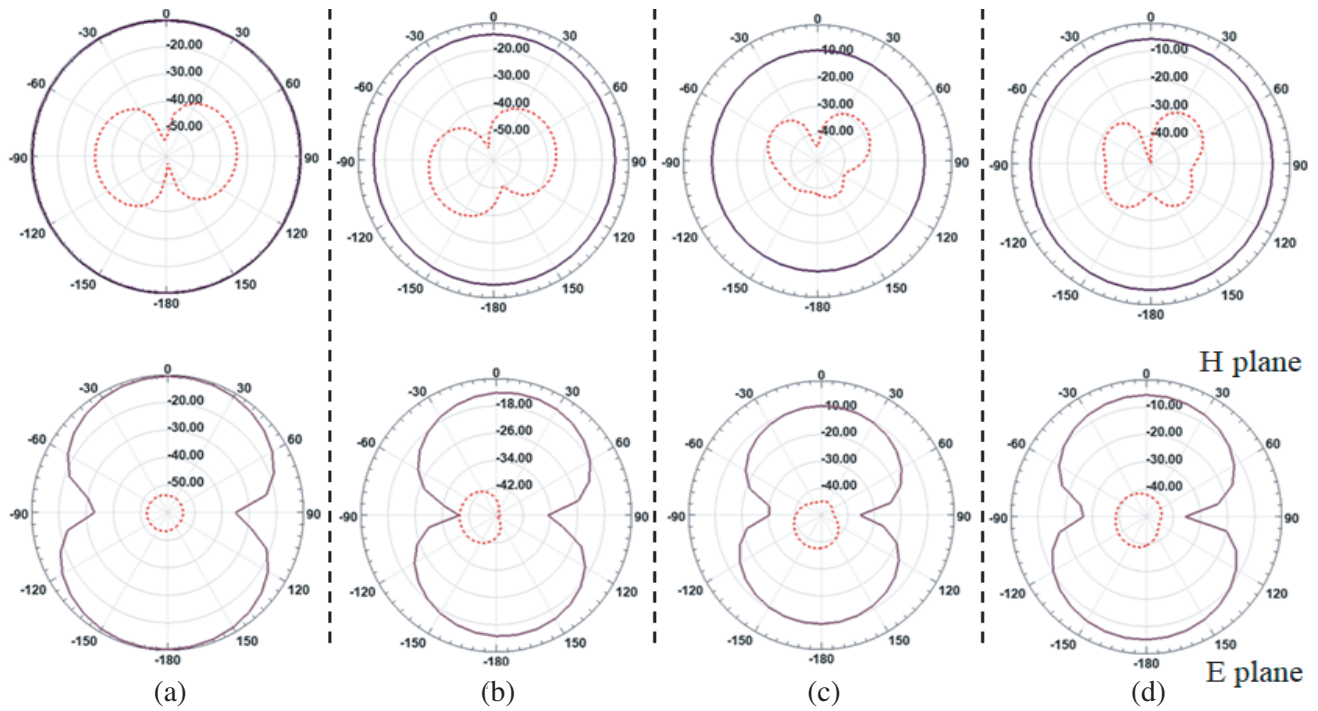


Figure 8. Co-pol and cross-pol radiation pattern in H and E plane at (a) 3.5 GHz, (b) 5.5 GHz, (c) 8.4 GHz, (d) 10 GHz.

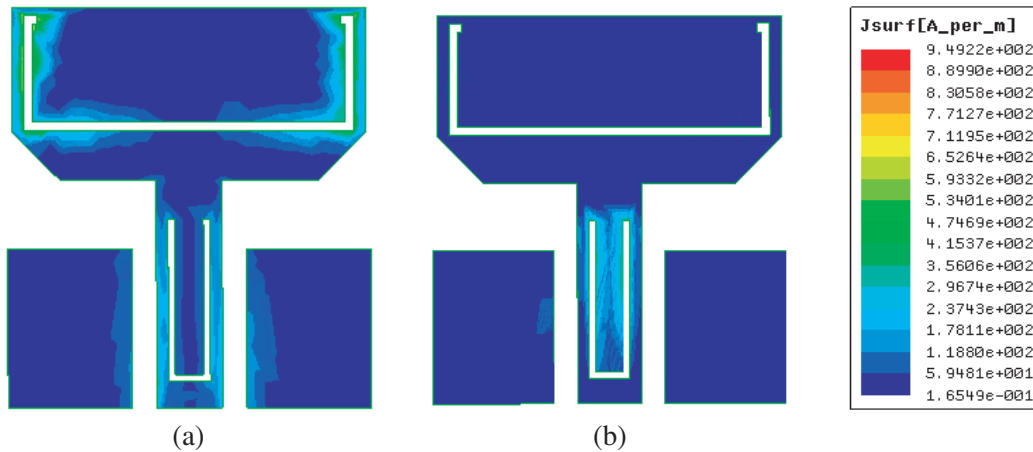


Figure 9. Surface current distribution at (a) 5.45 GHz and (b) 8.4 GHz.

4. EQUIVALENT CIRCUIT MODEL FORMATION OF THE REFERENCE UWB ANTENNA FROM ITS GEOMETRY

This section illustrates the fundamental insight to extract different circuit components associated with the reference UWB antenna from its geometrical configuration and constitutive material properties, and then construct the equivalent circuit model of the antenna. The key point behind an accurate model lies in the precise identification of the distributed and parasitic circuit parameters. The designed UWB on-chip antenna is made with three types of materials with three functionalities: silicon as a substrate, aluminium as a radiating patch, and silicon-di-oxide as an insulator between them. The

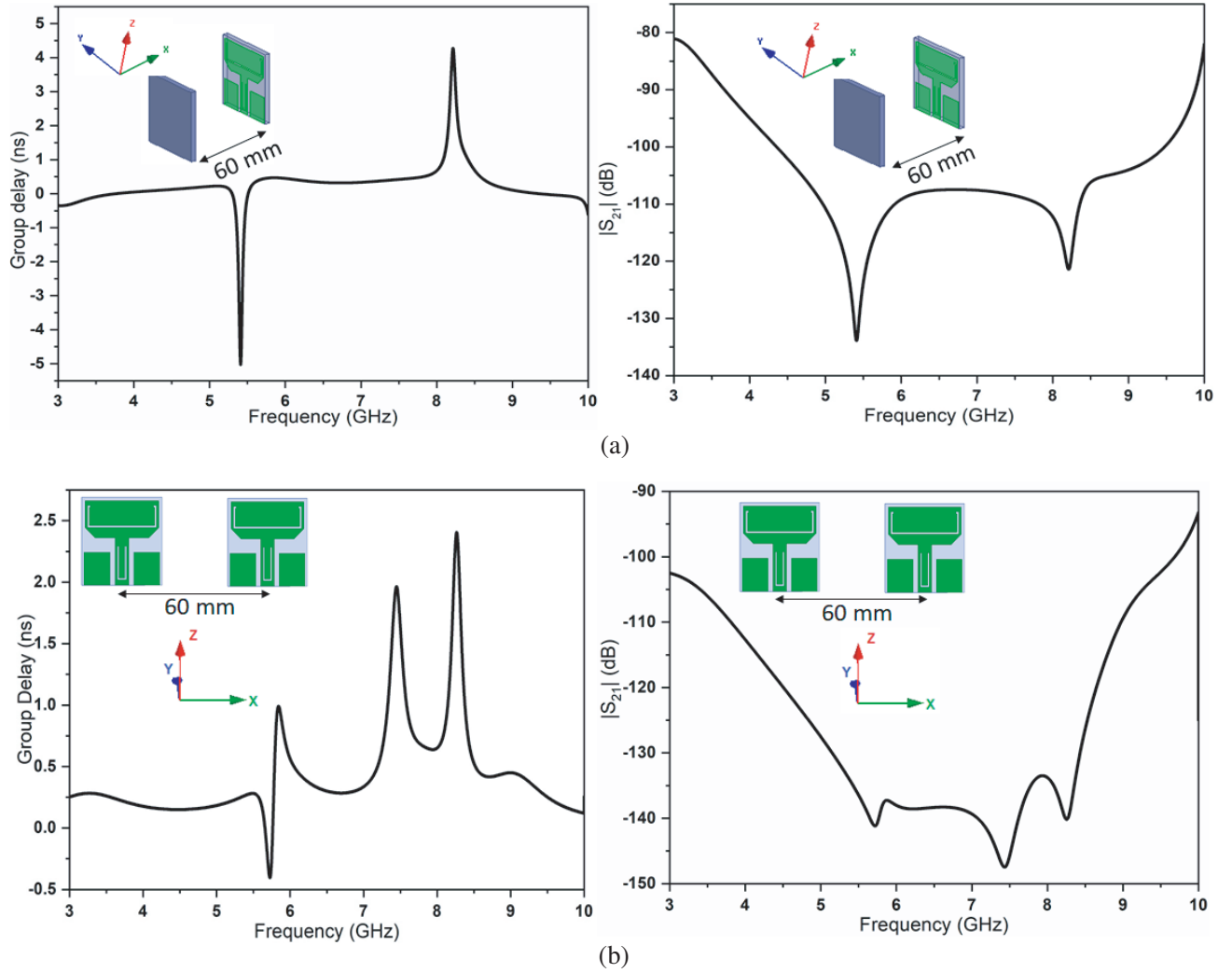


Figure 10. Group delay (left side) and $|S_{21}|$ (right side) of proposed antenna in (a) face to face and (b) side by side configuration.

identified distributed and parasitic circuit components of the CPW feed line on SiO_2 deposited Si wafer are depicted in Fig. 11(a). On the contrary, Fig. 11(b) shows the circuit components associated with the radiating patch. The following subsections elaborately describe how to extract the value of these above-mentioned circuit components.

4.1. The Equivalent Resistance (R_{Si}) and Capacitance (C_{Si}) of Si Wafer

The silicon substrate is basically modelled by two parameters like the equivalent resistance R_{Si} and the equivalent capacitance C_{Si} . The term R_{Si} is originated from the low resistivity property of silicon which is responsible for the substrate ohmic loss. On the other hand, C_{Si} represents the substrate capacitance which is responsible for the energy storing within it, and it is a function of the substrate doping concentration. For a Si wafer of known dimension, the equivalent resistance and capacitance are calculated as,

$$R_{Si} = \frac{\rho L_s}{W_s t_{Si}} \quad (3)$$

where ρ is the resistivity of the wafer; t_{Si} is the substrate thickness; L_s and W_s are the substrate length and width, respectively.

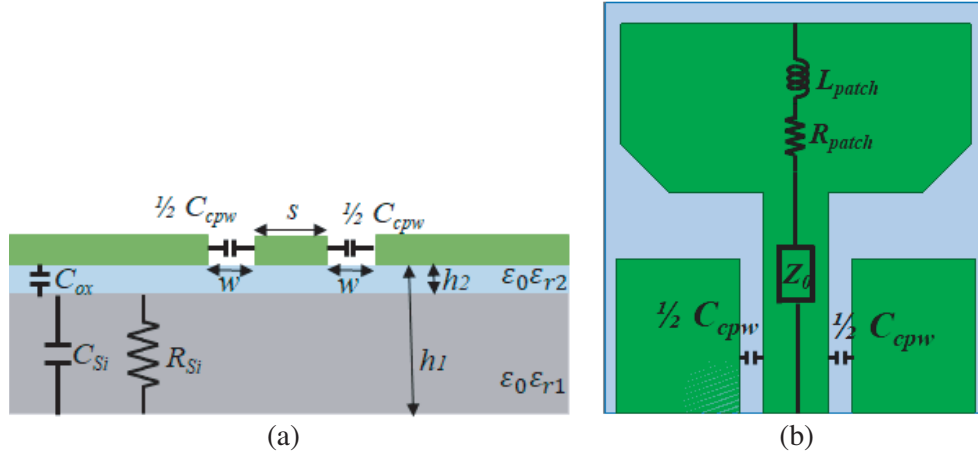


Figure 11. Illustration of model parameter for (a) CPW line on SiO₂ on Si wafer and (b) radiating patch.

The substrate capacitance C_{Si} is obtained as,

$$C_{Si} = C_{sub} L_s W_s \quad (4)$$

where C_{sub} denotes the substrate capacitance per unit area and is calculated as per [27],

$$C_{sub} = \frac{\varepsilon_{Si}}{d} \quad (4a)$$

where ε_{Si} is the permittivity of the silicon wafer, and d is the width of the depletion region that can be obtained by using Eq. (4b),

$$d = 2 \sqrt{\frac{\varepsilon_0 \varepsilon_r \phi_b}{q N_A}} \quad (4b)$$

here, ϕ_b is the bulk potential, q the charge of an electron, and N_A the doping concentration. In this case, N_A is 10^{15} atoms/cm³.

The bulk potential is expressed by the Eq. (4c),

$$\phi_b = (kT/q) \ln \left(\frac{N_A}{n_i} \right) \quad (4c)$$

where k is known as Boltzmann's constant, T the absolute temperature in Kelvin, and n_i the intrinsic carrier concentration which is 1.5×10^{10} atoms/cm³.

4.2. Equivalent Oxide Layer Capacitance (C_{ox})

The metal layer separated from a semiconductor material by an insulating medium forms an MIS (Metal-Insulator-Semiconductor) capacitor which is modelled by the parameter C_{ox} . The oxide capacitance (C_{ox}) is calculated as,

$$C_{ox} = L_s W_s \frac{\varepsilon_{ox}}{t_{ox}} \quad (5)$$

where ε_{ox} is the permittivity of the silicon dioxide, and t_{ox} is the oxide thickness.

4.3. Equivalent CPW Capacitance (C_{cpw})

Since the centre conductor and ground plane of the CPW feedline are in the same plane, conformal mapping is essential to figuring out the equivalent capacitance between them. The conformal mapping is used to map the coplanar electric fields between the ground plane and centre conductor into that of the corresponding parallel plate capacitor. Hence, by transforming the electric field from one geometrical

conformation to another geometrical conformation, it is a straightforward method to calculate the equivalent capacitance.

The CPW structure is designed on a double layer material (SiO₂ deposited Si Wafer) for the proposed OCA, as shown in Fig. 12(a). The total capacitance (C_{cpw}) of such a double-layer CPW structure is obtained by calculating the capacitance due to each layer separately and then summing the obtained results as per [28],

$$C_{cpw} = C_1 + C_2 + C_{air} \quad (6)$$

where C_1 is the partial capacitance due to the existence of the Si layer only while the effect of other layers is not taken into account; similarly, C_2 denotes the partial capacitance due to the presence of another dielectric layer SiO₂ only, and C_{air} represents the capacitance due to the electric field presence in the surrounding air medium. The thicknesses and relative permittivities of the lower (Si) and upper (SiO₂) layers are considered as $h_1 - h_2$, h_2 and ϵ_{r1} , ϵ_{r2} , respectively. The width of the centre conductor and separation between the conductor and the semi-infinite ground plane are taken as S and W , respectively.

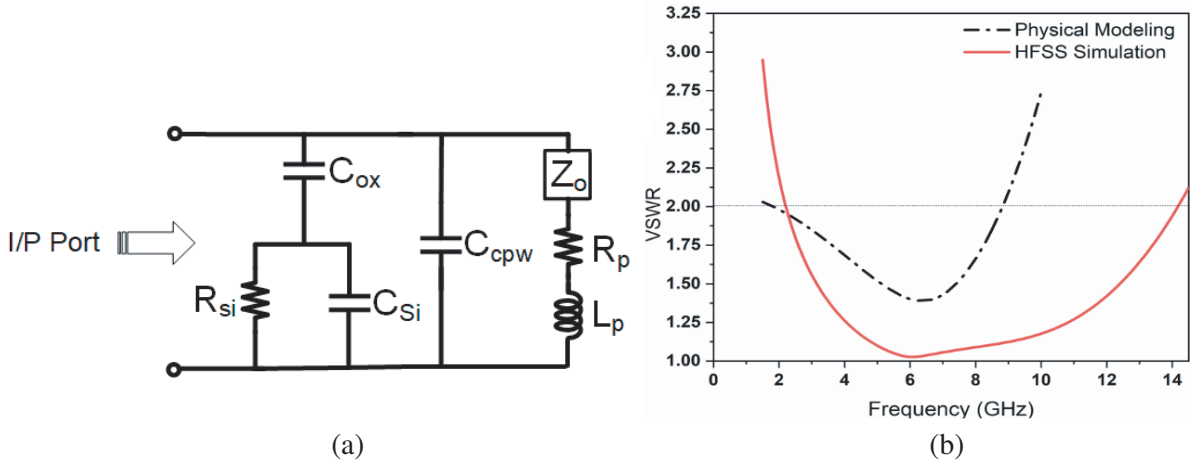


Figure 12. (a) Equivalent circuit model of the UWB on-chip antenna and (b) comparison of the VSWR response obtained from physical model using ADS platform and conventional FEM based HFSS simulation.

For simplicity, let us consider the ideal situation of the CPW line as — top metal with a thickness of zero, propagation of the quasi-static TEM mode of the EM wave along the feedline only, and the existence of the perfect magnetic walls along the boundary of the dielectric layers present in a structure including the CPW slots [29]. Therefore, by applying the conformal mapping, the expression of C_1 , C_2 , and C_{air} as in [30] is given below;

$$C_1 = 2\epsilon_0(\epsilon_{r1} - 1) \frac{K(k_1)}{K(k'_1)} \quad (7)$$

where $K(k_1)$ and $K(k'_1)$ represent the complete elliptic integral with modulus of k_1 and k'_1 , respectively. k_1 and k'_1 can be calculated as,

$$k_1 = \frac{\sinh(\pi S/4h_1)}{\sinh\{\pi(S + 2W)/4h_1\}} \quad (7a)$$

$$\text{and } k'_1 = \sqrt{1 - k_1^2}. \quad (7b)$$

The ratio of $K(k_1)$ and $K(k'_1)$ can be accurately approximated by the following generalised equation given by [31];

$$\frac{K(k'_n)}{K(k_n)} \approx \frac{1}{\pi} \log \left(2 \frac{1 + \sqrt{k'_n}}{1 - \sqrt{k'_n}} \right) \quad \text{for } 0 \leq k_n^2 \leq 0.5, \quad n = 0, 1, 2, \quad (7c)$$

$$\frac{K(k_n)}{K(k'_n)} \approx \frac{1}{\pi} \log \left(2 \frac{1 + \sqrt{k_n}}{1 - \sqrt{k_n}} \right) \quad \text{for } 0.5 \leq k_n^2 \leq 1, \quad n = 0, 1, 2, \quad (7d)$$

C_2 can be calculated as,

$$C_2 = 2\varepsilon_0(\varepsilon_{r1} - \varepsilon_{r2}) \frac{K(k_2)}{K(k'_2)}. \quad (8)$$

Equations (7a) and (7b) are also valid for this case. Only k_1 will be replaced by k_2 , and h_1 will be replaced by h_2 . Therefore, with the help of Eqs. (7a), (7b), (7c), and (7d), C_2 can be calculated from Eq. (8).

C_{air} can be calculated as,

$$C_{air} = 4\varepsilon_0 \frac{K(k_0)}{K(k'_0)} \quad (9)$$

where k_0 can be calculated as,

$$k_0 = \frac{S}{S + 2W} \quad (9a)$$

$$\text{and } k'_0 = \sqrt{1 - k_0^2} \quad (9b)$$

Therefore, with the help of Eqs. (7c), (7d), (9a), and (9b), C_{air} can be calculated from Eq. (9). Finally, the total capacitance due to two dielectric layers and air medium is obtained from the following expression;

$$C_{cpw} = C_1 + C_2 + C_{air} = 2\varepsilon_0(\varepsilon_{r1} - 1) \frac{K(k_1)}{K(k'_1)} + 2\varepsilon_0(\varepsilon_{r1} - \varepsilon_{r2}) \frac{K(k_2)}{K(k'_2)} + 4\varepsilon_0 \frac{K(k_0)}{K(k'_0)}. \quad (10)$$

In our case, h_2 is very thin as compared to h_1 . Therefore, the capacitance due to electric field propagation within the upper oxide layer can be ignored. The lower Si layer and the air medium mainly contribute to calculating the total capacitance. So, the final expression can be approximated as,

$$C_{cpw} \approx 2\varepsilon_0(\varepsilon_{r1} - 1) \frac{K(k_1)}{K(k'_1)} + 4\varepsilon_0 \frac{K(k_0)}{K(k'_0)}. \quad (11)$$

4.4. Characteristic Impedance (Z_0) of the CPW Feed Line

To calculate Z_0 , the following expression given by [29] is used;

$$Z_0 = \frac{1}{cC_{air}\sqrt{\varepsilon_{eff}}} \quad (12)$$

where c is the velocity of the light in free space; C_{air} can be calculated by using Eq. (9); and ε_{eff} can be calculated by using the following expression,

$$\varepsilon_{eff} = \frac{C_{cpw}}{C_{air}} \quad (12a)$$

where C_{cpw} can be obtained from Eq. (11). Therefore, it can be approximated as,

$$\varepsilon_{eff} = \frac{C_{cpw}}{C_{air}} \approx 1 + \frac{(\varepsilon_{r1} - 1)}{2} \frac{K(k_1)}{K(k'_1)} \frac{K(k'_0)}{K(k_0)}. \quad (12b)$$

4.5. Equivalent RF Sheet Resistance (R_p)

When the thickness of a conducting sheet is less than the skin depth of the metal at the lowest operating frequency, Eq. (13) can be used to find the DC resistance of a conductive sheet according to the transmission line theory [32],

$$R_{DC} = \frac{1}{\sigma t_{sheet}} \quad (13)$$

where σ and t_{sheet} represent the conductivity and thickness of the metal sheet, respectively.

The skin depth of the aluminium varies from $1.5 \mu\text{m}$ to $0.8 \mu\text{m}$ when the frequency changes from 3 GHz to 11 GHz. In the proposed antenna, the thickness of the radiating patch is $2 \mu\text{m}$ which is greater than the skin depth value of the aluminium at the lowest operating frequency of the UWB band. So, Eq. (13) is not valid for this case. Therefore, a frequency-dependent model of the sheet resistance as proposed in [33] based on transmission line theory is hereby used to find out the RF sheet resistance.

$$R_p = \frac{1}{\sigma \delta \left(1 - e^{-\frac{t_{sheet}}{\delta}}\right)} \quad (14)$$

where δ denotes the skin depth.

4.6. Equivalent Strip Inductance (L_p)

The model given by [34] has been used in this case to calculate the inductance of the patch and written as follows,

$$L_p = 2.10^{-1} l_p \left[\log \frac{l_p}{w_p + t_{sheet}} + 1.193 + \frac{w_p}{3l_p} \right] \quad (15)$$

l_p and w_p denote length and width of the patch, respectively.

With the help of the Eq. (3)–Eq. (15), all of the model parameters' values are extracted and mentioned as follows: $R_{si} = 110.43 \text{ k}\Omega$, $C_{si} = 8.6 \text{ nF}$, $C_{ox} = 0.65 \text{ pF}$, $C_{cpw} = 1.12 \text{ pF}$, $Z_0 = 21.3 \Omega$, $R_p = 0.26 \Omega$, $L_p = 1.15 \text{ nH}$. Therefore, these circuit components are properly connected to build an exact equivalent circuit model of the UWB reference patch antenna, which is shown in Fig. 12(a). At the same time, antenna's responses obtained from both the analytical approach and FEM-based HFSS simulation are compared in the graph mentioned in Fig. 12(b). It is clearly seen in that graph that the lower cut-off frequency is approximately same in both cases, but the upper cut-off frequency differs to some extent for two different approaches. It is obvious due to several factors, like top metal layer thickness assumed as zero, but it is not zero in the proposed structure. The boundary of the dielectric layers was considered as a pure magnetic wall, but in practice, it is not an absolutely perfect magnetic wall. While metal-insulator-semiconductor capacitance (C_{ox}) is calculated, area of the top metal layer was considered the same as the substrate for straightforward calculation, but it is not so. These factors are responsible for the deviation of the VSWR characteristics of the antenna obtained from two different methods.

5. EQUIVALENT CIRCUIT MODEL FORMATION OF THE PROPOSED UWB DUAL BAND-NOTCHED ANTENNA FROM ITS INPUT IMPEDANCE CHARACTERISTICS

This section discusses the equivalent circuit model formation of the proposed UWB dual band-notched antenna based on its input impedance characteristics. A basic UWB antenna can be modelled by connecting several parallel RLC circuits in series. Each parallel RLC block corresponds to a particular resonance. Thus, combining several adjacent resonances by cascading their corresponding parallel RLC circuits helps in achieving an UWB antenna. The input impedance of a UWB antenna can be calculated from the equivalent circuit model as in [35],

$$Z_e = \sum_{k=1}^n \frac{j\omega R_k L_k}{R_k (1 - \omega^2 L_k C_k) + j\omega L_k}. \quad (16)$$

From Eq. (16), R_k , L_k , C_k can be calculated by using iterative method. This method simply inserts the imported S_{11} data set (magnitude and phase) either from HFSS simulation or measurement into Eq. (16) to transform reflection coefficient (S_{11}) into Z_e [36]. For simplification, only real part of the impedance is considered to calculate the value of R_k , L_k , C_k by using Eq. (17) given below,

$$R_e = \sum_{k=1}^n \frac{R_k}{1 + R_k \left(\frac{1}{L_k \cdot 2\pi f} - C_k \cdot 2\pi f \right)^2}. \quad (17)$$

To make the equivalent circuit further simpler, the last component of any transmission system, i.e., antenna is often represented by a 50Ω load resistance. The input impedance plot of the proposed antenna is demonstrated in Fig. 13.

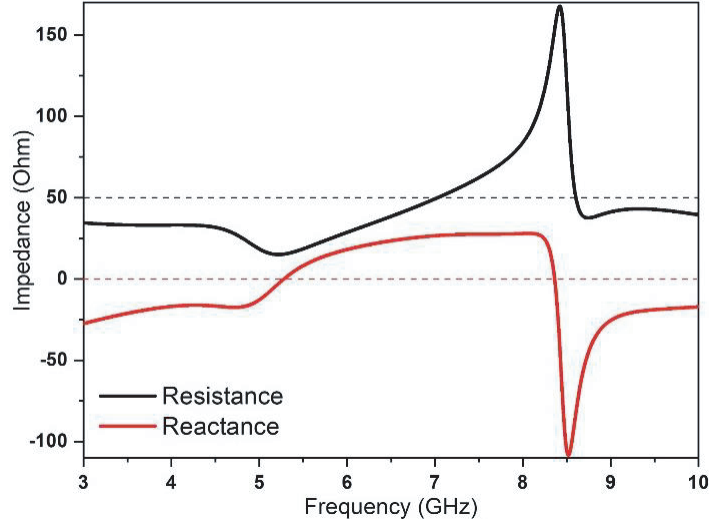


Figure 13. Input impedance plot of the proposed antenna.

The figure indicates that the real part and imaginary part of the input impedance fluctuate around 50Ω and 0Ω , respectively, throughout the entire operating band except at the notched frequencies (WLAN, DSRC, and ITU-8 band), where great deviation is observed. Also, it is noted that the imaginary impedance of the antenna changes from a negative value to a positive value at 5.35 GHz. This type of transition of the graph from negative reactance value (capacitance) to positive reactance value (inductance) can be well justified by a series RLC circuit. The equivalent impedance of a series RLC circuit, i.e., $(R + j\omega L - j\omega C)$ implies that the increment of frequency results in inductive behaviour of that circuit to dominate over the capacitive behaviour. So, WLAN (5.15 GHz–5.825 GHz) and DSRC (5.85 GHz–5.925 GHz) band can be accurately modelled by a series RLC resonance circuit. On the other hand, at 8.4 GHz, the imaginary impedance changes from a positive value to a negative value. This phenomenon can be explained with the help of a parallel RLC circuit. In a parallel RLC circuit, the total impedance, i.e., $j\omega RL \cdot (R + j\omega L - \omega^2 RLC)^{-1}$ will be approximately equal to $(j\omega C)^{-1}$ at high frequency. So, the downward tendency of the graph corresponds to a parallel RLC resonance circuit for ITU-8 band (7.9 GHz–8.8 GHz). Thus, combining the equivalent model of the individual notch band and the basic UWB antenna, the ultimate equivalent circuit model of the proposed antenna is constructed in Fig. 14(a). On the other hand, Fig. 14(b) demonstrates a simplified version of Fig. 14(a) by representing UWB antenna as a simple load resistance Z_a with a value of 50Ω .

Different parameters of that circuit model like R_{pn} , L_{pn} , C_{pn} , R_{sn} , L_{sn} , and C_{sn} can be calculated with the help of the following expression,

$$\omega_{PR} = \frac{1}{\sqrt{L_{pn}C_{pn}}} \quad (18)$$

$$BW_{PR} = \frac{1}{R_{pn}C_{pn}} \quad (19)$$

$$\omega_{SR} = \frac{1}{\sqrt{L_{sn}C_{sn}}} \quad (20)$$

$$BW_{SR} = \frac{R_{sn}}{L_{sn}} \quad (21)$$

where ω_{PR} and ω_{SR} are the resonant frequency of the parallel and series RLC circuit, respectively, and

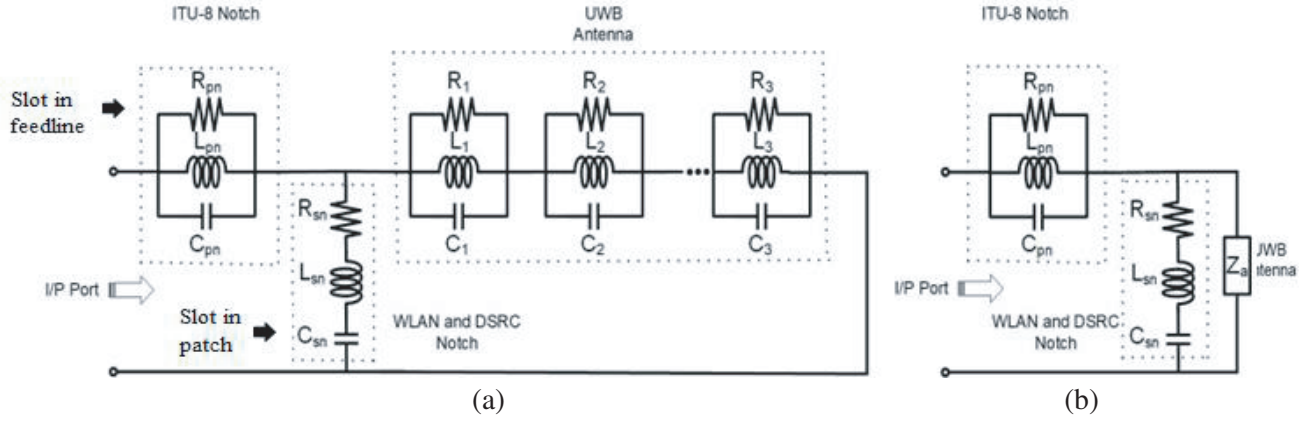


Figure 14. Equivalent circuit model of the proposed antenna; (a) actual model and (b) simplified model.

BW_{PR} and BW_{SR} are their corresponding notched bandwidths. The values of these four parameters are obtained from the HFSS simulation data. At the same time, R_{pn} and R_{sn} are also known quantities whose values are noted down from the impedance plot mentioned in Fig. 13. With the help of these six known quantities, the remaining four parameters like L_{pn} , L_{sn} , C_{pn} , C_{sn} are easily obtained by using the above-mentioned four Eqs. (18)–(21). For reference, taking three different values of the parameters — L_{s1} and L_{s2} , as considered in the parametric studies in Section 2.2.1 and 2.2.2, respectively, the equivalent circuit parameters are calculated and mentioned in Table 1. It can be observed that, with the decrement of the total slot length (L_{s1}), the equivalent parallel RLC block corresponding to the slot in the feedline becomes more capacitive, while the series RLC block corresponding to the slot in the patch becomes more inductive in nature. As per the parametric studies shown in Figs. 4(a) and 5(a), with decreasing the slot lengths the centre frequency of the respective notch band increases. Further, the impedance characteristic in Fig. 13 represents that, with increased frequency, the series and parallel RLC circuits provide inductive and capacitive reactance, respectively. Thus, the parametric studies and impedance characteristics justify the effect of variation of L_{s1} and L_{s2} on the equivalent circuit parameter values. With each set of the parameter values as mentioned in Table 1, the equivalent circuit model shown in Fig. 14(b) is simulated in circuit simulation platform namely Advanced Design System (ADS). The VSWR characteristics of the antenna obtained from HFSS and that obtained from ADS are compared in Fig. 15. The close agreement between the two validates the method of modeling the equivalent circuit of the designed antenna.

Table 1. Effects of L_{s1} and L_{s2} on series and parallel RLC circuit elements.

Cases	R_{pn} (Ω)	L_{pn} (pH)	C_{pn} (pF)	R_{sn} (Ω)	L_{sn} (nH)	C_{sn} (pF)
1. $L_{s1} = 8.02$ mm and $L_{s2} = 11.24$ mm	117.6	41	10	15.1	11.7	0.08
2. $L_{s1} = 7.62$ mm and $L_{s2} = 10.84$ mm (proposed)	66.6	29	12	16.1	13.4	0.06
3. $L_{s1} = 7.22$ mm and $L_{s2} = 10.44$ mm	65.1	23	14	18.1	16.8	0.04

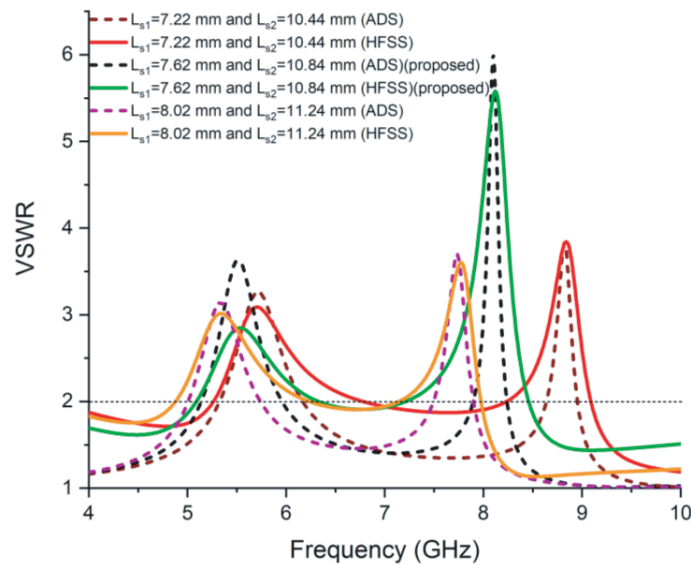


Figure 15. VSWR comparison of the dual band-notched UWB antenna obtained from HFSS simulation and equivalent circuit model using ADS software for three different combinations of L_{s1} and L_{s2} .

6. CONCLUSION

This article focuses on designing a compact UWB-extended bandwidth (3.2–13.2 GHz) antenna of size $8.8 \times 8.2 \times 0.679 \text{ mm}^3$ on silicon wafer with the inbuilt capability to mitigate interferences caused by WLAN (5.15–5.825 GHz), DSRC, (5.85–5.925 GHz), and ITU-8 band (7.9–8.8 GHz). As per the authors' best knowledge, analytically an equivalent circuit model formation of the UWB on-chip antenna has been reported in this article for the first time. Moreover, using iterative method, the proposed UWB dual band-notched antenna has been presented by its equivalent circuit model. As the proposed antenna covers such a vast bandwidth, it is applicable to short range application like intra/inter chip high-speed wireless communication system where the communication range is not more than a few centimeters.

ACKNOWLEDGMENT

The authors gratefully acknowledge financial support provided by Visvesvaraya PhD scheme, Ministry of Communications and Information Technology, Govt. of India, Grant No. PhD-MLA/4(29)/2015-16/01 and Special Manpower Development Programme for Chips-to-System Design (SMDP-C2SD) under Govt. of India, Grant No. 9(1)/2014-MDD (Vol. III).

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