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Inverse-Designed Metamaterials for On-Chip Combinational Optical Logic Circuit

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Abstract—Optical analog computing has recently sparked growing interest due to the appealing characteristics of low energy consumption parallel processing and ultrafast speed, spawning it complementary to conventional electronic computing. As the basic computing unit, optical logic operation plays a pivotal role for integrated photonics. However, the reported optical logic operations are volumetric and single-functional, which considerably hinders the practical cascadability and complex computing requirement. Here, we propose an on-chip combinational optical logic circuit using inverse design. By precisely engineering the scattering matrix of each small-footprint logic gate, all basic optical logic gates (OR, XOR, NOT, AND, XNOR, NAND, and NOR) are realized. On this foundation, we explore the assembly of these basic logic gates for general purpose combinational logic circuits, including optical half-adder and code converter. Our work provides a path for the development of integrated, miniaturized, and cascadable photonic processor for future optical computing technologies.

1. INTRODUCTION

With the increasing volume of information generated every day, the existing electronic computers have become increasingly difficult to meet the requirement of processing data with high speed and efficient energy. The dilemma of electronic computers mainly stems from the interconnect delay and large heat generation. Optical analogy computing, taking photons as the information carriers instead of electrons, heralds a superior alternative in information processing [1]. Due to its unique characteristics of processing data with light speed, low energy consumption, and massive parallel processing ability, optical computing has great potential in a host of practical scenarios, including autonomous driving and augmented reality, which involves high-throughput and low-latency data processing [2, 3]. In this respect, optical computing composed by integrated optical circuit promises to be complementary to the digital counterpart. As the basic computing element, optical logic gates are of particular importance to realize a general-purpose integrated optical circuit. It has been attracting substantial attention to achieve a small-footprint and cascadable optical logic gate [4].

Metamaterials, as artificial composite materials with engineered atoms, offer a versatile platform to enable a myriad of functional optical computing components [5–29]. Recent examples include equation-solver [30], spatial differentiation [31], and optical neural network [32]. Previous designs about optical logic gate have centered on two routes: linear or nonlinear interference effect, embodied as free-space and on-chip appearances. For nonlinear optical logic gates, they typically necessitate high signal powers and large interaction lengths, because the optical nonlinearities of natural materials are relatively weak [33, 34]. For linear optical logic gates, a variety of logic gates have been demonstrated using

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photonic crystals nanowire networks and metasurfaces [35–47]. Previous studies mainly focus on the implementation of individual logic gate, while the combinational logic circuit has not yet been extensively studied. Furthermore, most optical logic gates rely on the constructive or destructive interferences within three-dimensional volume, making their integration and miniaturization very difficult. It is thus highly desirable to achieve a cascadable and small-footprint logic gate that provides sufficient levels of cascadability and meets user-defined demand for a variety of combinational optical logic circuits [4].

In this work, we propose an on-chip combinational optical logic circuit composed of different logic gates. Each logic gate is physically constructed by a small-footprint inhomogeneous metamaterial. By inversely designing the spatial metamaterial layout, the scattering matrix of the logic gate can be arbitrarily engineered to mimic the behavior of logic operation. The logic gate is strongly optimized using topology optimization algorithm, whose average element error (AEE) is reduced to 10^{-5}. Both output amplitude and phase of the logic gate can be accurately controlled. We realize all basic optical logic gates (OR, XOR, NOT, AND, XNOR, NAND, and NOR) as the fundamental building block for optical combinational logic circuit. Furthermore, we explore the cascadability of logic gate to facilitate optical half-adder and code converter. This universal design strategy has the potential to enable compact and cascadable photonic processors for general purposes.

2. RESULTS

A single optical logic gate only has fixed and limited functionality. To enable a flexible and complex functionality, it is highly anticipated to assemble different optical logic gates, analogous to electronic circuit. Fig. 1 shows the schematic diagram of the combinational optical logic circuit. The geometry and metamaterial layout of each logic gate should be carefully designed. As shown in Fig. 2(a), the physical geometry of the logic gate consists of a two-dimensional (2D) domain sandwiched by planar metallic waveguides. The top and bottom parts are electromagnetic (EM) absorber. We consider the fundamental TE10 mode to carry information operating at $f = 5\,\mathrm{GHz}$ (the working wavelength $\lambda = 6\,\mathrm{cm}$). Two inputs (rectangular waveguides, port 1 and port 2) and one output (port 3) are attached on the left and right sides, so the transmission matrix of the logical gate can be described

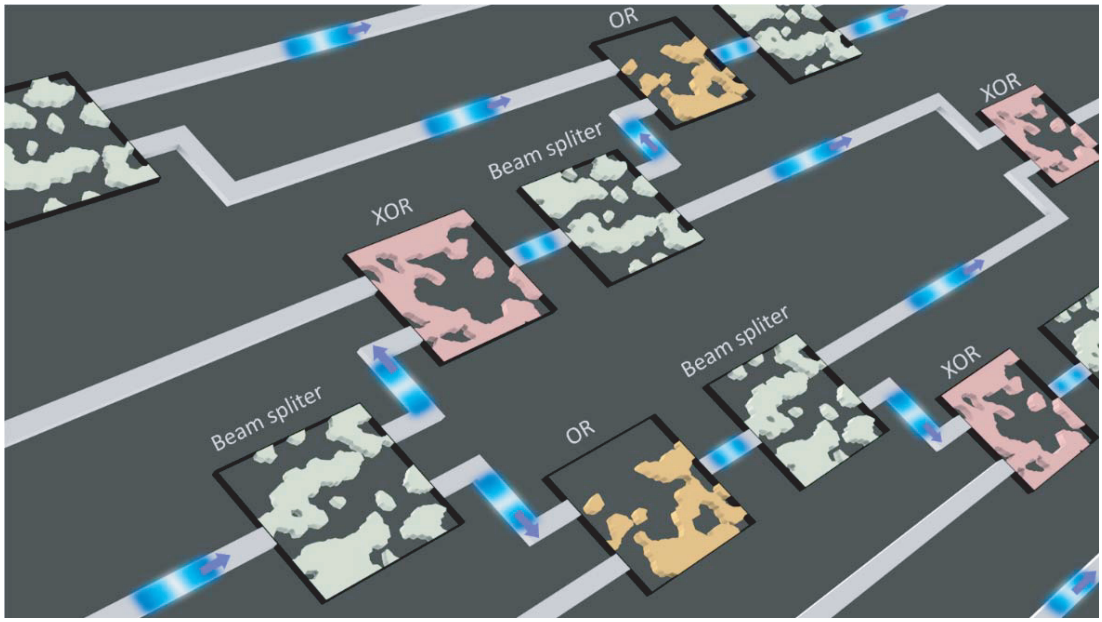


Figure 1. Schematic of the combinational optical logic circuit. Each optical logic gate is inversely designed with topology optimization to mimic the behavior of electronic logic gate. Different optical logic gates are physically assembled in a certain rule to build up a combinational logic circuit for user-defined functionality.

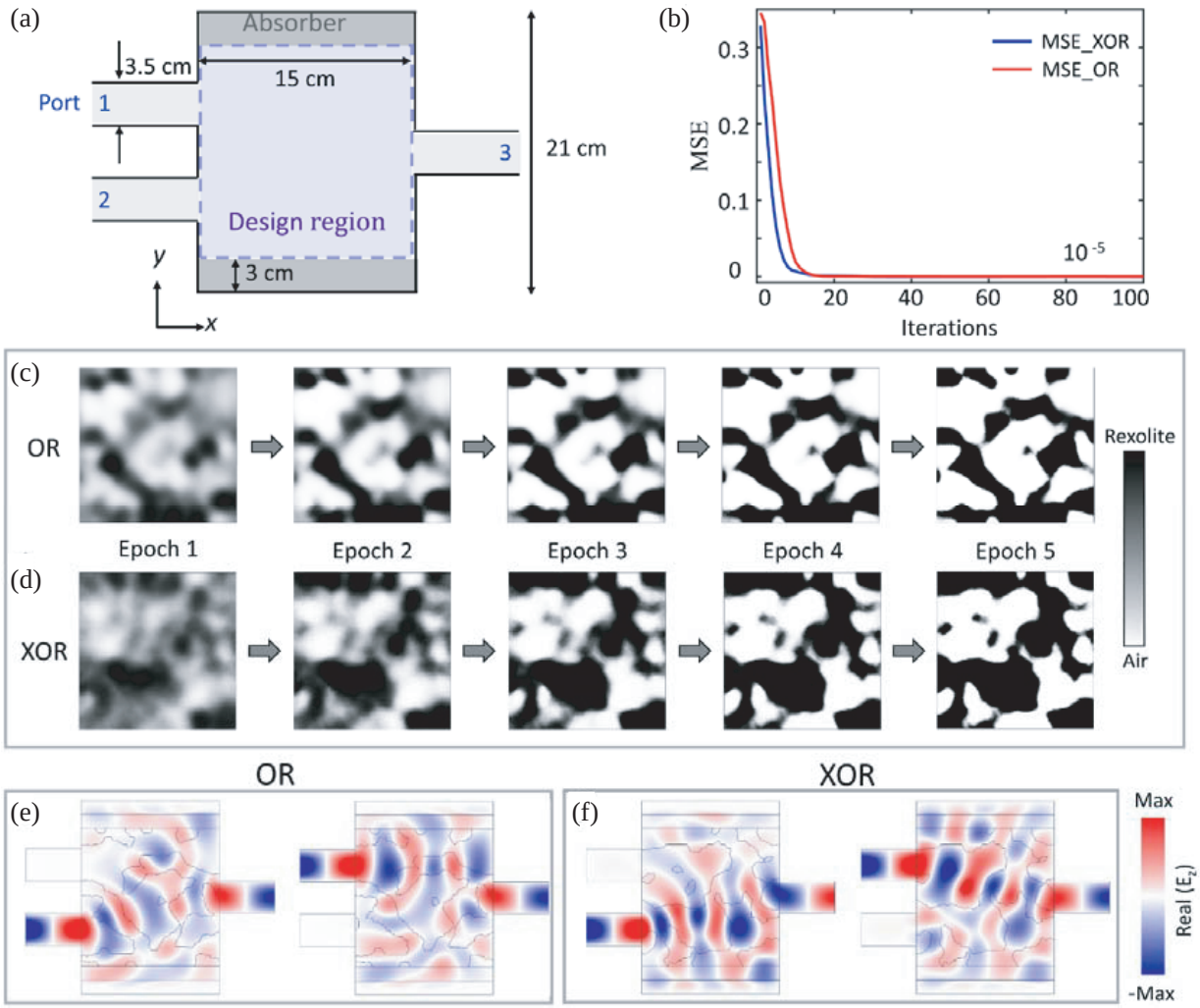


Figure 2. Design of the optical logic gate. (a) The physical geometry of optical logic gate. It contains two input ports and one output port on either side of the design region, which is surrounded by absorption boundary on top and bottom. The inverse design aims to find the needed material distribution in the design region. (b) The AEE over iterations. (c), (d) Time-evolution of the material density of (c) OR gate and (d) XOR gate. (e), (f) The simulation results of electric field distribution with different input modes of (e) OR gate and (f) XOR gate.

as a 2×1 matrix ($\begin{bmatrix} S_{31} \\ S_{32} \end{bmatrix}$). In addition, there is a 2×2 reflection matrix ($\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$), which shall be miniaturized to near zero. The central purple highlighted region is the design region (15 cm $\times$ 15 cm, $2.5\lambda \times 2.5\lambda$), where the dielectric distribution associated with the expected scattering matrix needs to be found during the optimized procedure.

The EM optimization that finds the dielectric distribution associated with the scattering matrix of the logical gate is undertaken using topological optimization method [48]. Comparatively, deep learning enabled inverse design always needs to discretize the design region into a number of fixed elements, such as circular and square ones, and the ultimate optimized result is generated from a combination of these pixels [49, 50]. With the increase in the number of degrees of freedom, the solution space increases exponentially, leading to the burdensome task of large dataset collection and complex algorithm modeling. Topology optimization can obtain the optimal dielectric distribution without constraint on the geometry and huge cost on data collection. In our work, we adopt the density-based

method to inversely design the dielectric distribution of the logic gate. The design domain is discretized into arbitrarily shaped N elements, which is different from the pixel design region. A random initial density distribution is given inside the design region. To facilitate the topology optimization, we deploy a loss function AEE defined as the complex-plane "distance" between the S parameters and their expected values. Evidently, for OR logic gate, the transmission matrix is set as $\begin{bmatrix} S_{31} \\ S_{32} \end{bmatrix} = \begin{bmatrix} a \\ a \end{bmatrix}$ to ensure the output phases are identical with different input modes. The identical amplitudes of S_{31} and S_{32} lay the foundation for the following cascaded circuit. For XOR logic gate, the transmission matrix is correspondingly set as $\begin{bmatrix} S_{31} \\ S_{32} \end{bmatrix} = \begin{bmatrix} a \\ -a \end{bmatrix}$. This results in zero output field when the two input ports are excited simultaneously, which is analogous to the characteristics of XOR logic gate. The optimization goal is to minimize the AEE of logic gate. The optimization variable is defined by the relative permittivity at each spatial point in the design region, which is bounded between air with the relative permittivity of 1 and Rexolite, a low-loss polystyrene with the relative permittivity of 2.53. After dozens of iterations, convergence is obtained, and the AEE is decreased to 10^{-5}, indicating that the OR and XOR logic gates can implement the target matrix with negligible errors (Fig. 2(b)). Having a satisfactory convergence, the next optimization step is performed using penalty function to enforce the relative permittivity binarized as air or Rexolite. The iterative process of binaryzation is displayed in Figs. 2(c), (d), where each epoch contains 100 iterations. We stop the optimization process when the error in the binarized structure is satisfactory. Finally, we obtain the dielectric distribution that almost only contains two materials, without intermediate value, which is friendly for practical fabrication. The transmission matrices of OR and XOR logic gates are $\begin{bmatrix} 0.685 \\ 0.685 \end{bmatrix}$ and $\begin{bmatrix} 0.685 \\ -0.685 \end{bmatrix}$, respectively, and the reflection matrices of these two logic gates are almost zero. The electric field distributions of the optical OR and XOR logic gates with different input modes are plotted in Figs. 2(e), (f). For OR logic gate (Fig. 2(e)), the output amplitudes and phases under different input excitations are identical. For XOR

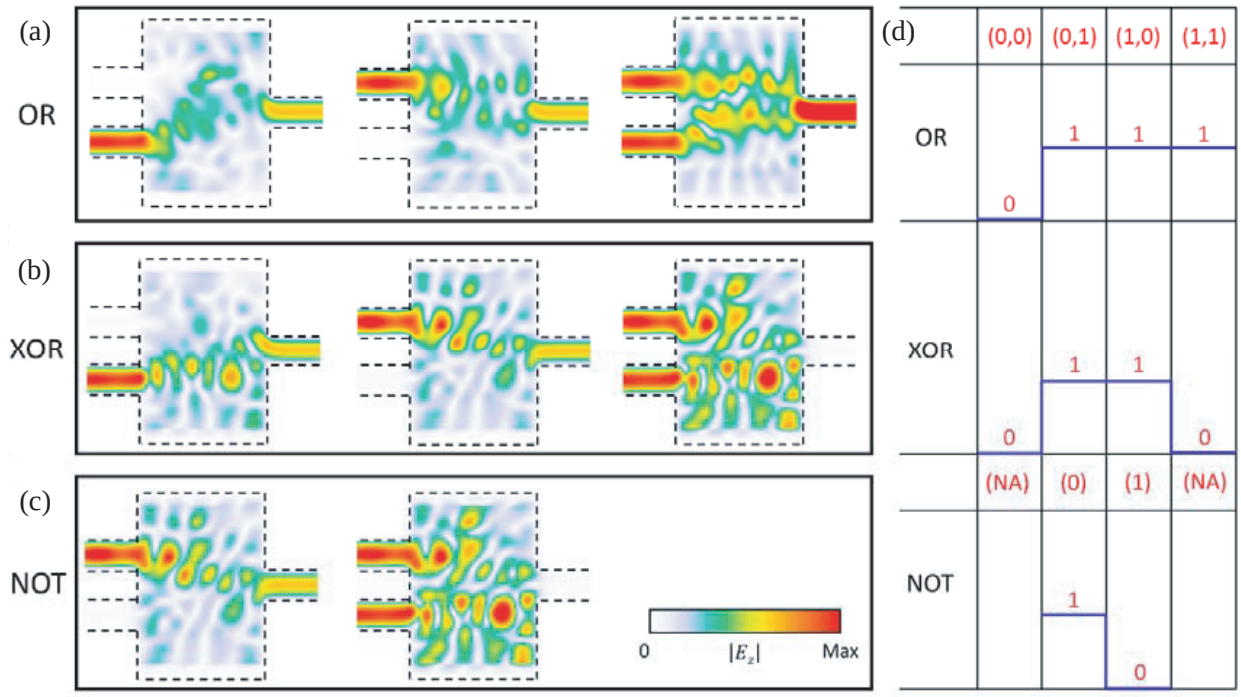
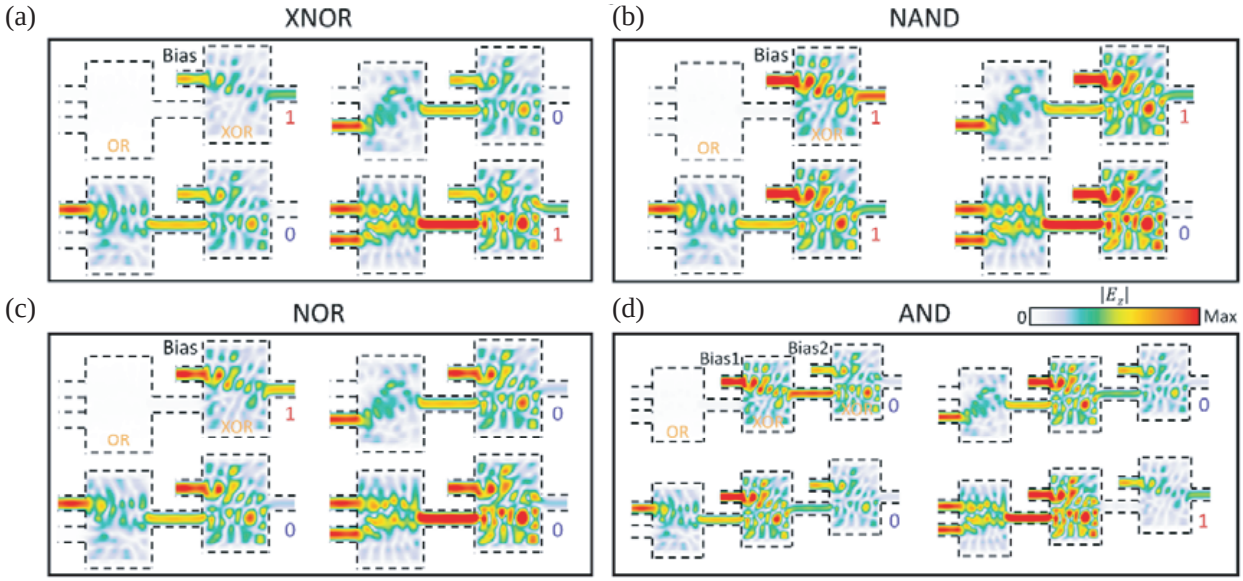


Figure 3. Result of the optical OR, XOR and NOT logic gates. (a), (b), (c) The electric magnitude distribution of (a) OR gate, (b) XOR gate, and (c) NOT gate with different input modes. (d) The truth table of the proposed optical OR, XOR, and NOT gates.

logic gate (Fig. 2(e)), the amplitudes are the same while the output phases are opposite under different input excitations. In addition, we can see that there are almost no reflection waves inside OR and XOR logic gates, which is crucial for cascaded photonic system. The electric field distributions of optical OR and XOR gates are well matched with the target scattering matrices.

Figures 3(a), (b), (c) show the simulation results of the electric field magnitude ($|E_z|$) with different input modes. All simulation results are consistent with the target results. If we employ one input port of XOR logic gate as a bias input, it behaves as NOT gate, as presented in Fig. 3(c). Fig. 3(d) shows the truth table of the optical OR, XOR and NOT gates. Other optical logic gates can be achieved by cascading these OR, XOR, NOT logic gates with a certain rule. Fig. 4 shows the simulation results of XNOR, NAND, NOR and AND logic gates, implemented by cascaded photonic element. For the design of XNOR, we cascade OR and XOR and set bias input with the field amplitude being 0.685 times input amplitude. The output field is zero when only one input port is activated. As for the other two cases, the output field is nonzero, meaning that the XNOR gate is realized, as shown in Fig. 4(a) For the design of NAND gate, we cascade OR and XOR and set bias input with the field amplitude being 1.37 times input amplitude. Only when all input ports are excited the output field is zero, as shown in Fig. 4(b). For the design of NOR gate, we cascade OR and XOR and set bias input with the field amplitude being 1.03 times input amplitude. In particular, when both input ports are activated, only the electric fields from the bias input contributes to the output power. For other three cases, the output power is significantly reduced as shown in Fig. 4(c). The ratio of output power between the



(e)

Input	NOR	NAND	XNOR	AND	Bias Input	
(0,0)	1	1	1	0	NOR	1.03
(0,1)	0	1	0	0	NAND	1.37
(1,0)	0	1	0	0	XNOR	0.685
(1,1)	0	0	1	1	AND	1.37 (Bias1) 0.7 (Bias2)

Figure 4. Results of the optical XNOR, NAND, NOR, and AND logic gates. (a), (b), (c), (d) The electric magnitude distribution of (a) XNOR gate, (b) NAND gate, (c) NOR gate, and (d) AND gate with different input modes. These logic gates are designed with two- or three-level cascaded structure, by adding a permanent bias channel. (e) The truth table of the proposed optical XNOR, NAND, NOR and AND gate. The values of needed bias inputs are listed for different optical logic gates.

output states 1 and 0 is up to 9 : 1. For the design of AND gate, we cascade one OR and two XOR and set bias1 input with the field amplitude being 1.37 times and bias2 input with the field amplitude being 0.7 times input amplitude, as shown in Fig. 4(d). Similar to NOR gate, the output power of logic state 1 is almost 9 times that of logic state 0. Fig. 4(e) presents the truth table of the proposed optical XNOR, NAND, NOR and AND gate, and the values of needed bias inputs corresponding to different optical logic gates.

We then progress to the design of optical half adder as the first demonstration of optical combinational logic circuit. Fig. 5(a) exhibits conventional digital logic circuit of half adder, which is composed of AND and XOR gates. The parallel connection is marked by red dotted box in Fig. 5(a). We innovatively replace it with the beam splitter achieved by the designed photonic structure shown in Fig. 5(c). The two outputs have the identical phase with different inputs, and their amplitudes are the same which is half of the input magnitude. Such characteristics make the proposed beam splitter a useful tool in combinational logic circuit. Based on this, Fig. 5(b) shows the optical half adder where ports A and B are the input ports, and ports C and S are carry bit and sequence bit, respectively. The proposed optical half adder has an excellent agreement with conventional digital combinational circuit. Fig. 6 shows the simulation results of the optical half adder under four different input cases ((a) $A = 0$, $B = 0$; (b) $A = 0$, $B = 1$; (c) $A = 1$, $B = 0$; (d) $A = 1$, $B = 1$). We can see that the truth value of carry bit is 1 only when two ports are both turned on. The simulated results demonstrate that the optical half adder coincides with the truth value of digital half adder.

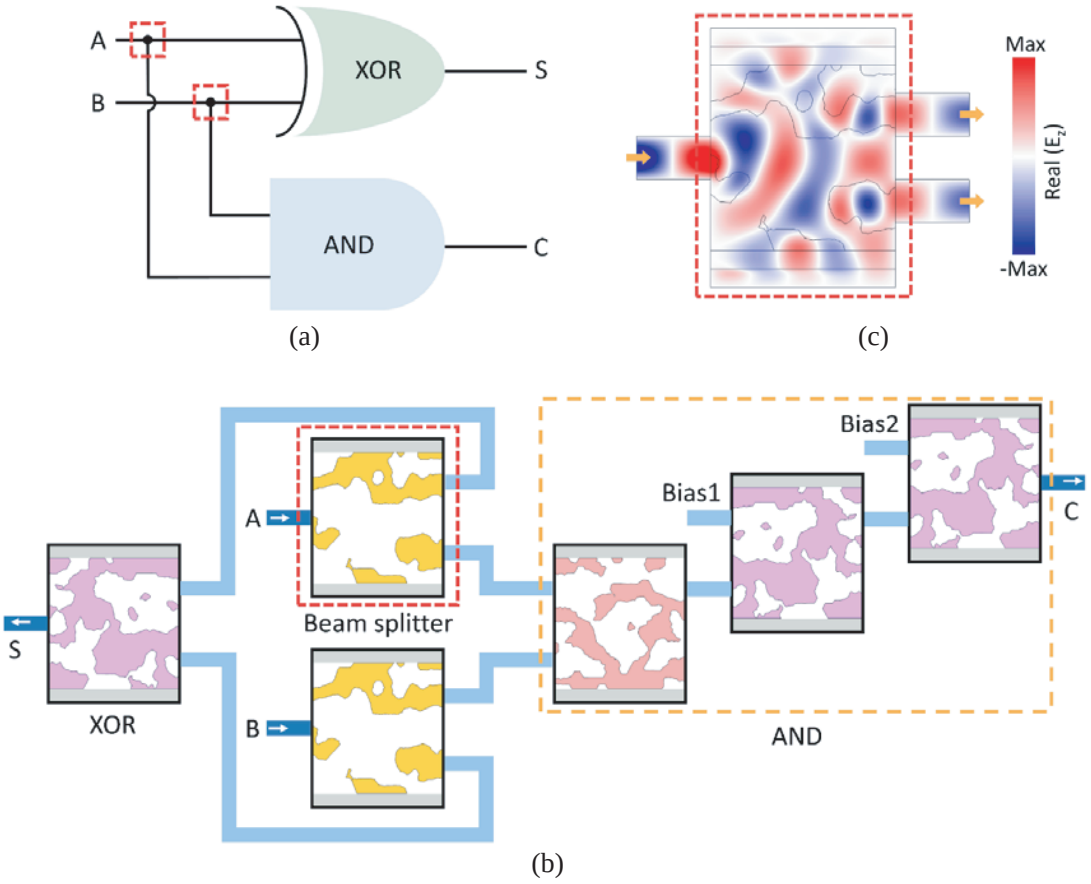


Figure 5. Design of the optical half adder. (a) The architecture of conventional digital half adder, which is composed of AND and XOR gates. (b) The optical half adder. A and B are the input ports, and C and S are carry bit and sequence bit, respectively. The inputs from A and B ports are split into two by a beam splitter and then simultaneously pass through AND and XOR gate. (c) The simulation result of the beam splitter. The output phase and amplitude at two output ports are exactly the same.

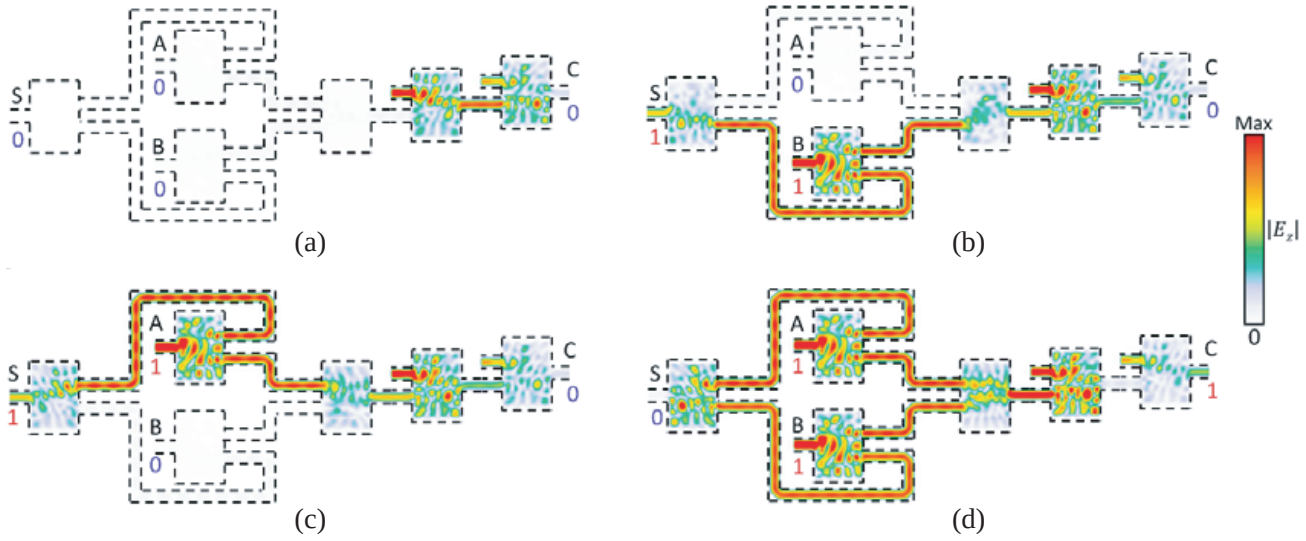


Figure 6. Results of the optical half adder. The electric magnitude distribution of the optical half adder with four different input modes (a) $A = 0$, $B = 0$, (b) $A = 0$, $B = 1$, (c) $A = 1$, $B = 0$ and (d) $A = 1$, $B = 1$.

In order to further benchmark the optical combinational logic circuit, we design a code converter to convert four bit Gray code to four bit natural binary code. The truth value table of such a converter is listed in Fig. 7(a). According to the truth table, we design the corresponding optical combinational logic circuit composed of connected beam splitters and XOR gates, as shown in Fig. 7(b). The four input ports are G3, G2, G1, and G0, and the output ports are B3, B2, B1, and B0. Fig. 8 shows the simulation results of the electric field magnitude with 15 different input modes (except the input case of 0000). We regard the truth value as 0 when the output fields are almost zero. Otherwise, the truth value is 1. From the simulation results, the proposed optical code converter has a good agreement with the truth value table in Fig. 7(a). It should be noted that the values of four inputs from G0 to G3 are increased (G0 = 1, G1 = 2.9, G2 = 8.5, G3 = 17) due to the utilization of beam splitters. The output fields are nearly zero when the truth value is 0, because the S parameters of optical logic gate are strongly optimized to make the error negligible.

Gray code	Natural binary code	Gray code	Natural binary code
$G_3G_2G_1G_0$	$B_3B_2B_1B_0$	$G_3G_2G_1G_0$	$B_3B_2B_1B_0$
0000	0000	1100	1000
0001	0001	1101	1001
0011	0010	1111	1010
0010	0011	1110	1011
0110	0100	1010	1100
0111	0101	1011	1101
0101	0110	1001	1110
0100	0111	1000	1111

(a)

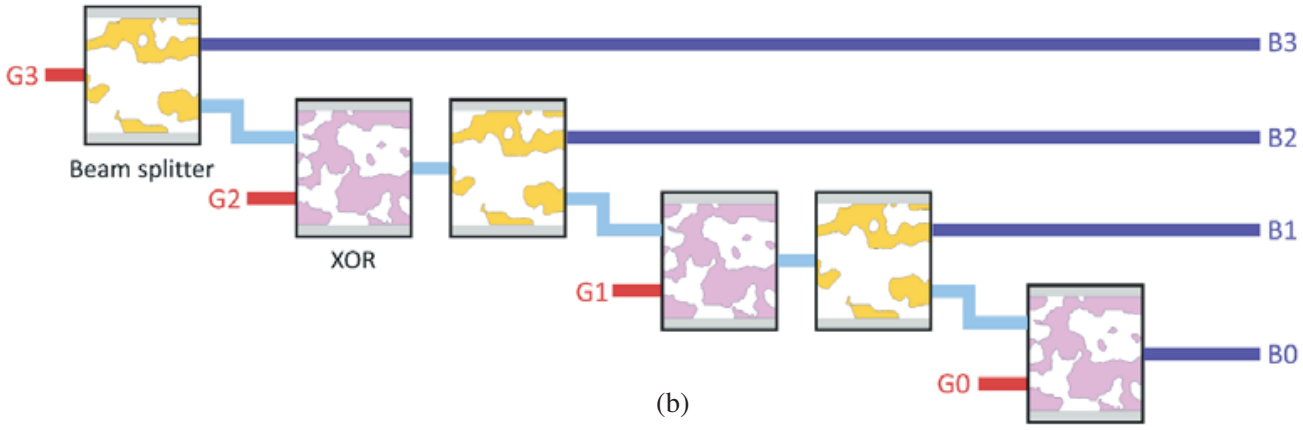


Figure 7. Design of the optical code converter. (a) The truth value table of the code converter that transforms four bit Gray code to four bit natural binary code. (b) The optical implementation of code converter. The four input ports are G3, G2, G1, and G0, and the output ports are B3, B2, B1, and B0.

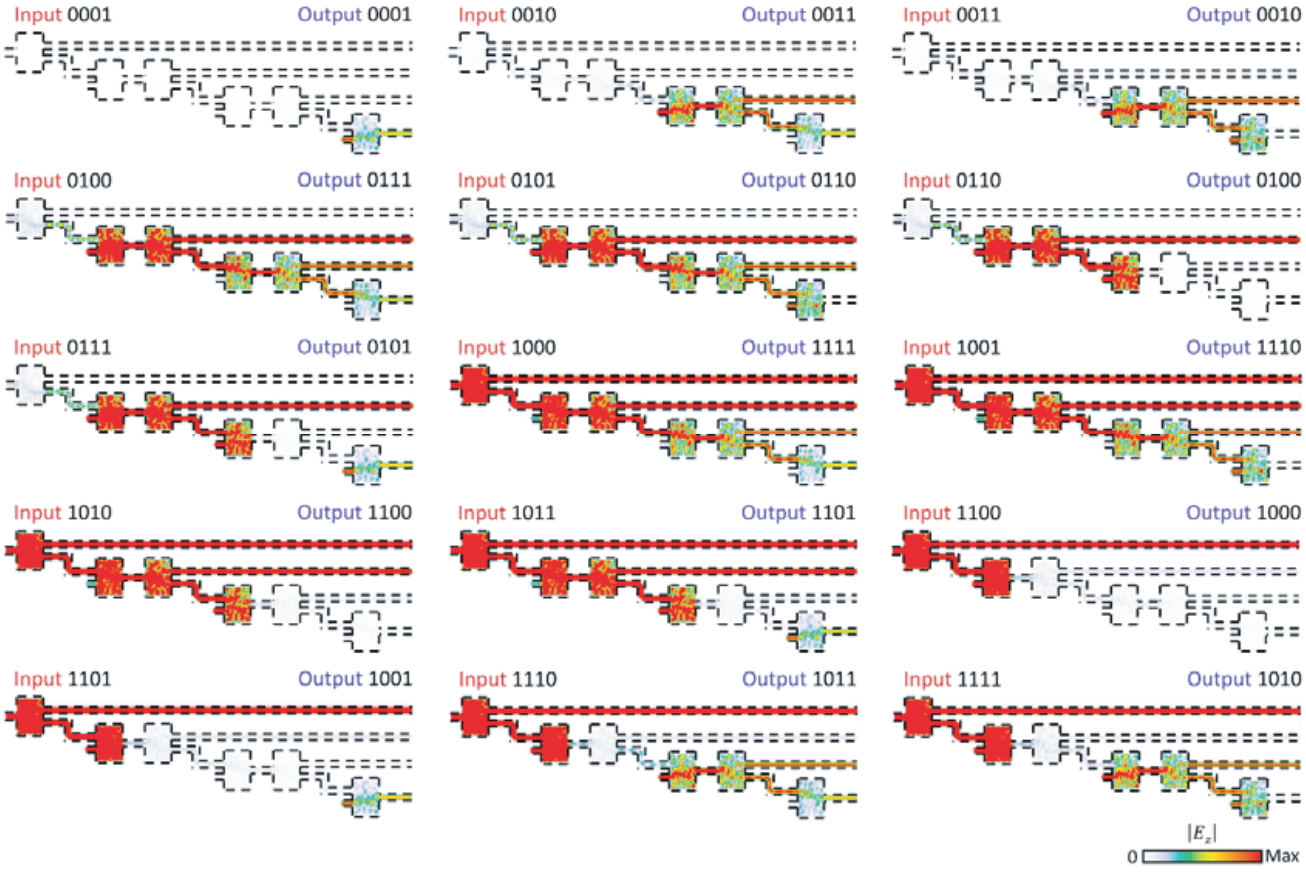


Figure 8. Results of the optical code converter. All the results are consistent with the expectation. For the case of input 0000, the output is certainly 0000 (not shown).

3. CONCLUSION

In conclusion, we proposed an on-chip combinational optical logic circuit assembled of different logical gates. The optical logical gate is inversely designed to make the scattering matrix identical to the logical operation, utilizing topology optimization to obtain the metamaterial profile. We imposed a realistic dielectric parameter to logical gate to ensure that they are friendly for practical fabrication. We demonstrated all kinds of basic optical logic gates, OR, XOR, NOT, AND, XNOR, NAND, and NOR with high contrast ratios, some of which must be realized by adding a bias channel to ensure, such as '0 NOR 0 = 1' and '0 NAND 0 = 1'. The involvement of bias channel is also helpful for loss compensation in an optical cascaded system. We cascaded these logic gates in a certain rule to build upcom binational logic circuit, including optical half-adder and code converter. Beyond that, other functional optical circuit can be readily achieved with a more sophisticated network based on the designed optical logic gates. Although the designed logic gate was demonstrated in the microwave, the concept is relevant and can be readily generalized to higher frequencies with a similar framework. These findings will lead to various optical logic modules and benefit dense on-chip integration applications. Alongside, the inverse-designed metamaterials provide a flexible platform for precise manipulation of EM waves and multichannel data processing.

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