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Wafer Level 3D-Stacked Integration Technology with Coplanar Hot Via MMIC for mm-Wave Low-Profile Applications

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ABSTRACT: Wafer-level three-dimensional stacked integration technology is demonstrated in this paper, employing three gallium arsenide (GaAs) monolithic integrated circuits (MMICs) and gold (Au) bumps, and specifically designed for high-density and low-profile applications operating at millimeter-wave frequencies. A ground coplanar waveguide to ground coplanar waveguide (GCPW to GCPW) hot via interconnect has been developed to facilitate vertical transitions within a multi-stacked electromagnetic (EM) environment. Electrical connection between the upper and lower layers is achieved through 70 µm-height Au bumps. Compared to 2.5D packaging, this innovative structure exhibits an increased integration capability of more than three times within the same area, with a thickness of 0.451 mm. Ultra-wideband transmission between RF chips is achieved within a compact area of 0.16 square millimeters, enabling extremely short-distance interconnect for system-in-package configurations. Appropriate utilization of ground metal within the package ensures strict electromagnetic field confinement, preventing interference from adjacent circuits. The designed transitions were fabricated and characterized. The measured result has an insertion loss of less than 0.65 dB and return loss of better than 20 dB up to 40 GHz for a back-to-back structure. This integration technology can further enhance integration capability, reduce transmission loss, and improve electromagnetic isolation. The presented approach holds significant potential for applications requiring high-density integration and reliable performance in the millimeter-wave regime.

1. INTRODUCTION

The increase of operating frequencies has led to the substantial increase in the number of analog devices, resulting in a heightened demand in the sized reduction of mm-wave system. To enhance performance and reduce size, weight, and power consumption, multiple types of active and passive devices, each serving different functions, need to be integrated in an assembly or tile. In recent years, wafer-level three-dimensional integration technology has emerged as an attractive method for achieving higher performance and higher density of radio frequency (RF) components [1–3]. Concurrently, several vertical interconnect technologies for RF chips have undergone continuous evolution [4]. An advanced interconnect solution is crucial for the new packaging approach to achieve its ultimate aim of low profile, superior integration, and high performance.

In general, flip-chip technique and hot-via technology are the two most appropriate technologies for wafer-level 3D transition, which have demonstrated excellent results in terms of insertion loss, return loss, and bandwidth [5–7]. However, the flip-chip technology employed in traditional wafer-level stacking structures can only achieve two layers of interconnection. Fortunately, hot-via MMIC offers an optimal solution for stacking more than three layers, connecting the RF signal to the substrate background through via holes [8].

Microstrip (MS) to coplanar waveguide (CPW) hot-via flip-chip interconnects have been demonstrated on various substrates, such as Al_2O_3 [5], Si [9], and PCB [10, 11]. A single-stacked low noise amplifier with MS to CPW hot via has been designed and evaluated between chip and the silicon carrier [12]. The above research about hot via interconnect is for a single stacked GaAs MMIC. However, the electromagnetic environment in the three-dimensional low-profile structure is very complex, and the performance of the quality of the interconnects between the dies at mm-wave frequencies can be severely impacted by their package environment. Therefore, it is necessary to further optimize hot-via in the multi-layer wafer-level stacking structure.

In this paper, we present a novel GCPW to GCPW hot-via interconnect technology designed for high-density wafer-level package structures, effectively reducing interconnection distances. Section 2 introduces a model for vertically stacked structures, employing wafer-level integration technology that utilizes hot-via and Au bump techniques for the vertical stacking of three-layer coplanar GaAs MMICs. Additionally, ANSYS HFSS was employed for the three-dimensional full-wave simulation in the design of GCPW transmission lines, and an equivalent circuit model of the GCPW to GCPW hot-via interconnect is provided, along with testing methods. In Section 3, a comprehensive analysis of the test results is presented. Section 4 delves into potential improvements, contributing to the ongoing discourse on advancing this technology.

2. MODELING AND TRANSMISSION DESIGN

2.1. Modeling

Figure 1(a) illustrates the wafer-level stacked integration with three face-up GaAs MMICs. A large number of Au bumps are

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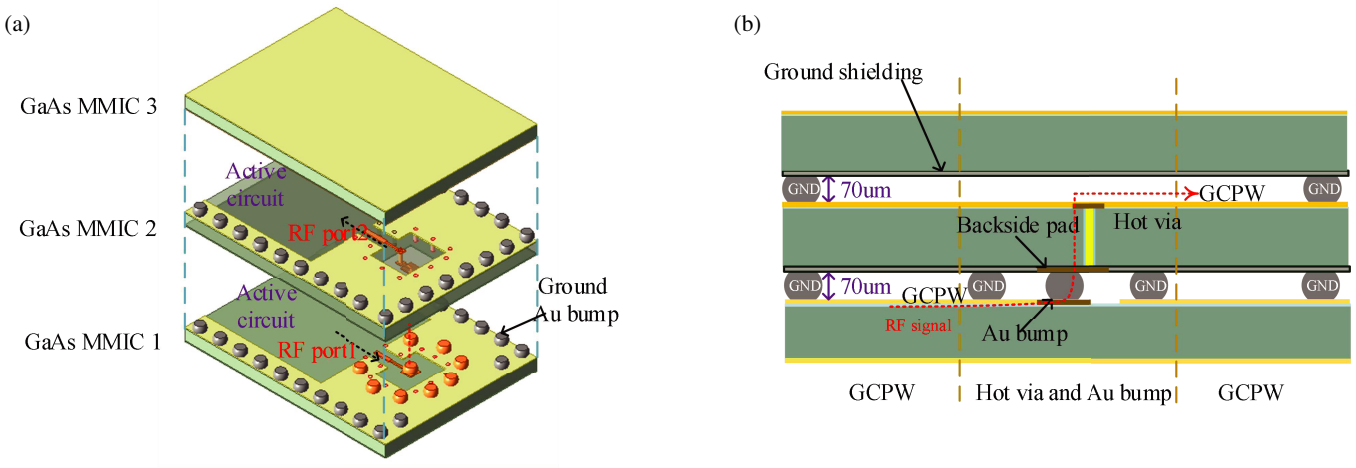

FIGURE 1. Vertical stacked structure of three face-up GaAs MMICs with GCPW to GCPW coplanar hot via interconnect: (a) Three-dimensional view of port to port transmission. (b) The cross-section of GCPW to GCPW hot via interconnect.

employed to establish both physical and electrical connections between layers, also serving as ground points. In Fig. 1(b), the cross-section of the GCPW to GCPW transition within this low-profile structure is appropriately presented. A contact pad is on the backside metallization of hot via MMIC, and the isolation between the hot via and the back metal ground plane is achieved through an additional process, utilizing a dicing method to remove extraneous metal. The signal is transmitted from the front-side pad to the backside pad through the hot via, and then directly connected to low-profile GCPW on bottom layer through Au ball bump. The entire signal transition path is completely surrounded by ground metal. Hot via is a cylindrical structure with a diameter of 50 µm according to the process rules, showing a structure with a smaller top and a larger bottom. Au bumps, with height of 70 µm and diameter of 100 µm, are fabricated using standard micro-nano processing on the bottom of GaAs MMIC with thickness of 100 µm.

From the model in Fig. 1(a), it is evident that the RF signal from the lower chip is directly transmitted to the upper layer through a hot via with an Au ball bump, without any additional routes. This allows the system to achieve extremely short-distance interconnect, resulting in a higher density integration area.

2.2. Design of the Low-Profile GCPW Transition Structure

The electromagnetic environment of low profile three-dimensional stacked structure is very complex in mm-wave. The primary challenge of RF transition in flip-chip is to reduce parasitic effect such as radiation [13], which is also the focus of hot via interconnect. Therefore, the primary consideration in 3D transition design is the horizontal transmission line. Open line structures, such as microstrip (MS) and coplanar waveguide (CPW), are susceptible to radiation losses and detuning at high frequency. It is difficult to avoid the influence of other layers in multi-layer stacked structures; especially the spacing between layers is only 70 µm here. Typically, GCPW is utilized in place of them since it provides electromagnetic separation between several channels.

For a standard transmission line, it is easy to calculate its dimensions. For instance, a 50-ohm microstrip transmission line on a GaAs substrate with a height of 100 µm has a line width of 70 µm. However, in scenarios with minimal spacing between layers, the GCPW transmission might be influenced by adjacent layers, introducing various interference factors that are challenging to calculate directly. In such cases, three-dimensional full electromagnetic simulation can be used for precise modeling and analysis.

Figure 2 illustrates the geometries of GCPW. Firstly, a standard GCPW 50-ohm line is selected, with both line width and line spacing set at 50 µm. It is used to compare the simulation results before and after stacking. The simulation results indicate that the other layers have little effect on the insertion loss of the transmission line, but a serious influence on the return loss, which is reduced by more than 10 dB. In this case, the line spacing or line width can be adjusted in the stacked structure for EM full-wave simulation. Fig. 2(c) is the cross-section of rematching, with a line width of 50 µm and a line spacing of 70 µm, which has an excellent performance in the low profile structure.

The modified structure effectively supports interconnection transmission but may pose limitations in complex designs, requiring a distinct three-dimensional full-wave simulation for each horizontal transmission. Hence, identifying a more universally applicable design approach is crucial. As illustrated in Fig. 3, standard 50-ohm grounded coplanar waveguide (GCPW) lines with varying line widths of 20 µm, 30 µm, 40 µm, and 50 µm are simulated under a 70 µm high ground shielding, respectively. The simulation results reveal a gradual reduction in S_{11} as the line width (W) decreases. When the line width (W) is below 30 µm, the GCPW transmission performance closely resembles that of a 50-ohm transmission line. However, this improvement is accompanied by an increase in insertion loss (S_{21}) as the line width decreases.

Reducing the line width and spacing implies stronger grounding constraints on the electromagnetic field, resulting in less interference and reduced radiation. Nevertheless, excessively small line width leads to increased insertion loss, making it unsuitable for RF interconnection with high

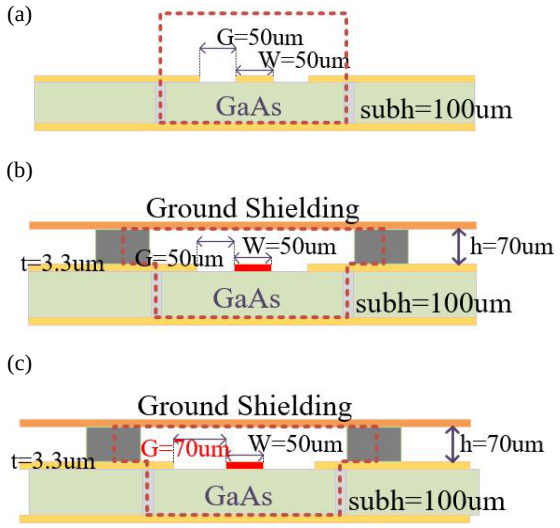

FIGURE 2. The geometries of GCPW transmission lines: (a) Standard 50 ohm GCPW. (b) Mismatched GCPW with ground shielding. (c) Modified 50 ohm GCPW with ground shielding.

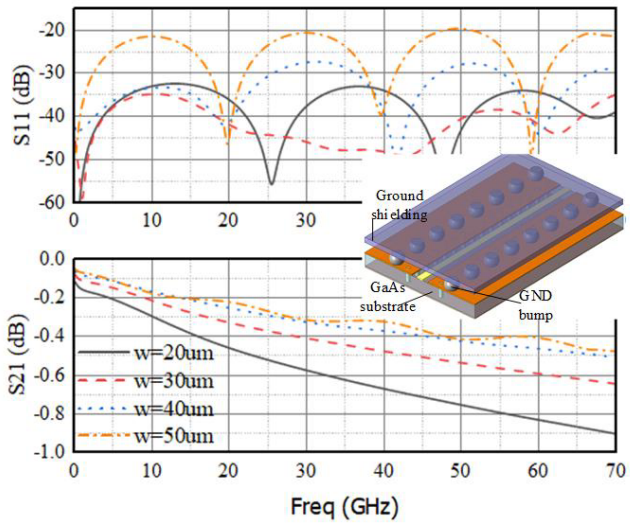

FIGURE 3. Simulated S-parameter of standard 50 ohm GCWP with line widths of 50 µm, 40 µm, 30 µm and 20 µm in 70 µm-height low profile structure.

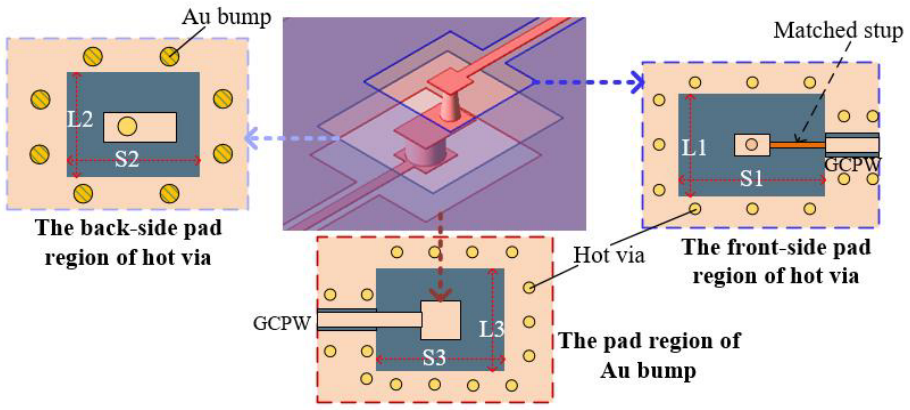

FIGURE 4. Schematic diagram of the GCPW to GCPW hot via transition.

loss requirements. Balancing insertion loss and interference considerations, the GCPW with a line width of 30 µm and a line spacing of 24 µm is chosen as the horizontal transmission structure.

2.3. Design of GCPW to GCPW Hot Via Transition

Poor transmission performance is often caused by the discontinuity of transmission, and it is necessary to optimize the transmission structure to achieve impedance matching. Insertion loss and return loss are the most important performance indicators for vertical transmission design. To achieve a transition between GCPW and a discontinuous vertical conversion structure with minimal reflection, the geometries of both the signal and return path were meticulously analyzed.

Figure 4 illustrates the hot via transition along with several crucial dimensions. In the signal path, the size of the top pad (L1, S1) which connects to the GCPW line on the surface of the MMIC was analyzed first, and the hot-via backside pad (L2, S2) and the pad region of Au bump (L3, S3) was analyzed. Following from this, in the return path, the position of the ground via and ground bump was analyzed. To achieve impedance matching, a stub was inserted between the GCPW and the vertical transmission structure, ensuring a 50-ohm match at the port. The conductor of the transmission RF signal path is entirely surrounded by a grounded hot via, grounded Au bump, and the grounded metal on the backside of the chip. Beyond serving as a pathway for signal return, this configuration significantly isolates the signal from the external electromagnetic environment, effectively achieving interference shielding. Furthermore, the complete grounding of the backside of the chips ensures the isolation of the circuits on the front side of both the upper and lower layers of chips.

The precise prediction of parasitic effects is crucial within a system for achieving impedance matching. Numerical methods assist circuit designers in understanding the design phase

C_1 (fF)	C_2 (fF)	C_3 (fF)	L_1 (pH)	L_2 (pH)	R_1 (Ω)
50.1	45.9	26.6	148.2	123.4	0.05

TABLE 1. Extracted parameters of GCPW to GCPW hot via transition structure.

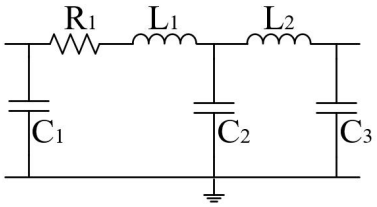

FIGURE 5. Equivalent circuit model of GCPW to GCPW hot via interconnect.

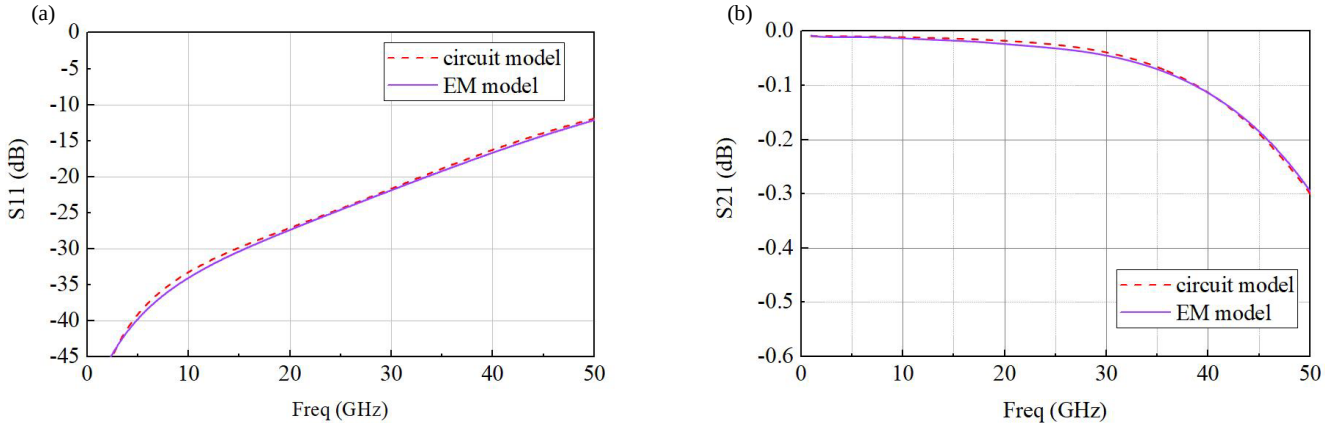

FIGURE 6. S parameters matching of EM modelling and equivalent circuit: (a) S_{11}. (b) S_{21}.

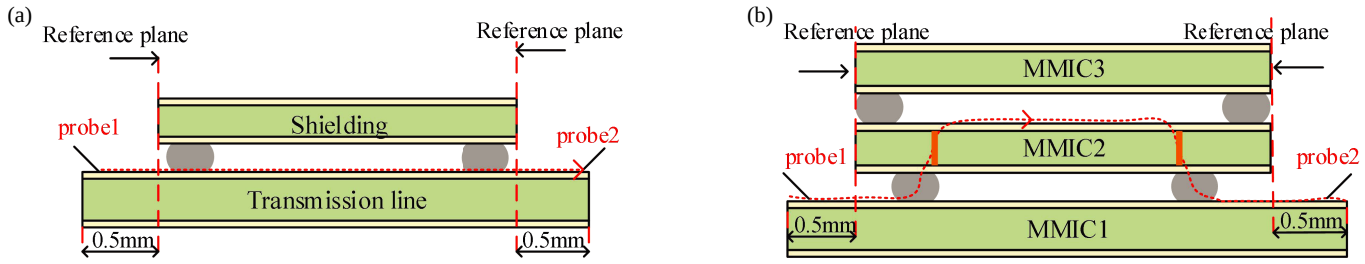

FIGURE 7. The test structure of important transition: (a) GCPW with ground shielding. (b) GCPW to GCPW coplanar hot via interconnect with back to back structure.

and even enable the direct implementation of designs [14]. By extracting equivalent circuit parameters from the electromagnetic (EM) model and establishing an equivalent circuit model, it becomes possible to comprehend and optimize circuit designs using circuit analysis methods.

In Fig. 5, the equivalent circuit model of GCPW to GCPW hot via interconnect is presented [15]. The RLC values are simulated and tuned to match the S-parameters of the circuit with those obtained from EM extraction. Table 1 presents the extracted equivalent circuit parameters in the model. Fig. 6 illustrates the matching of S_{11} and S_{21}. Through the extracted equivalent circuit, further insights into the GCPW to GCPW hot via interconnect model are gained, allowing for adjustments to parameters and structures to achieve impedance matching.

2.4. Test Methods

Whether it is a horizontal transmission or a vertical transmission structure, it is difficult to directly probe test after stacking. Therefore, the appropriate test method is also very important. Fig. 7(a) shows the test structure of the horizontal transmission line. The backside metallized chip is stacked on the transmission line to be tested for shielding. The lower layer of the transmission line being tested is extended by 0.5 mm on both sides to ensure that the upper shielding does not obstruct the test pad. After the probe testing, the data is de-embedded to the actual reference surface using through-reflect-line (TRL) calibration method [16]. Fig. 7(b) shows the back-to-back test structure of GCPW to GCPW hot via interconnect, which also extends the bottom MMIC to both sides by 0.5 mm. The selected CPWG transmission line is used to connect in GaAs MMIC.

length	Insert loss
1 mm	0.17 dB
2 mm	0.33 dB
3 mm	0.50 dB

TABLE 2. Comparison of the measured insertion loss at 40 GHz.

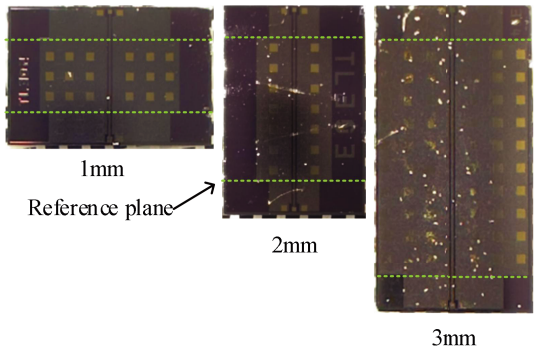

FIGURE 8. The photo of 1 mm, 2 mm, 3 mm GCPW without ground shielding.

(a) (b)

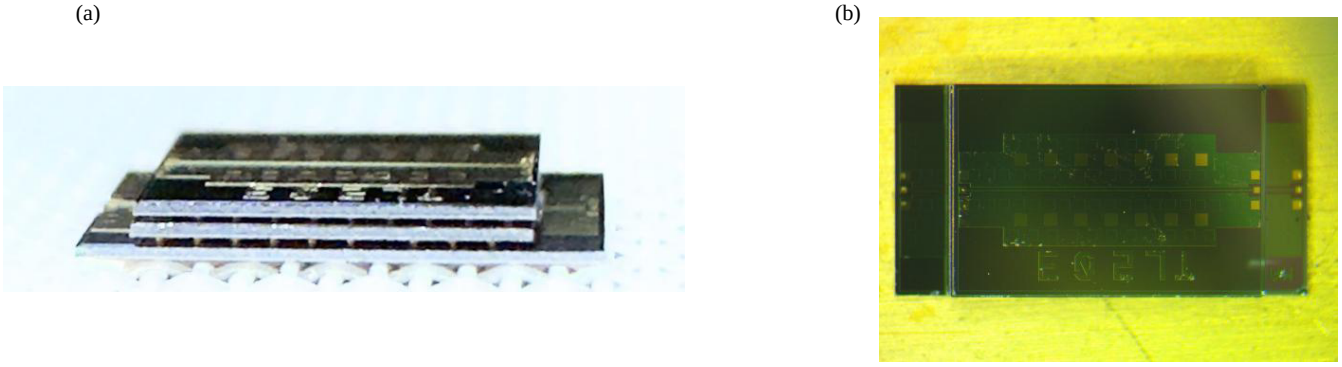

FIGURE 9. The photo of the back to back hot via vertical transitions: (a) Three-dimensional view. (b) Top view.

3. FABRICATION AND MEASUREMENT

The GCPW of 1 mm, 2 mm, and 3 mm lengths are processed respectively, and the two-port test was completed after assembly. Fig. 8 shows the photos of different lengths of GCPW with 30 µm line width under the microscope. To facilitate the probe test, all GCPW transmission lines are extended by 0.5 mm in the unshielded area. Consequently, the test results are de-embedded to shift the reference plane structure. The measured results are shown in Table 2. The insertion loss is 0.17 dB, 0.33 dB, and 0.50 dB at 40 GHz, respectively. Therefore, the average loss of 1 mm length GCPW with 30 µm line width at 70 µm height shielding is about 0.17 dB at 40 GHz.

Figure 9 presents microscopic images in a three-dimensional view and the top view of the back-to-back GCPW to GCPW coplanar hot via transition. S-parameters for the transition were measured on a probe station, and the results are depicted in Fig. 10. In the back-to-back configuration, the insertion loss is less than 0.65 dB, and the return loss is superior to 20 dB. The measured results closely match the electromagnetic-simulated results from DC to 40 GHz.

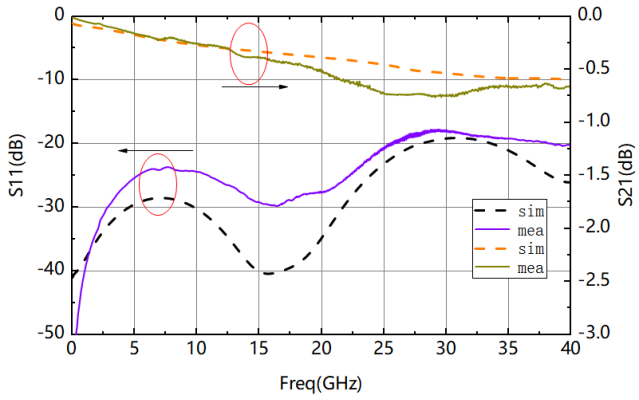

FIGURE 10. Measured S_{11} and S_{21} of the GCPW to GCPW hot via vertical transitions in back to back structure.

4. CONCLUSION

This paper introduces a coplanar Grounded Coplanar Waveguide (GCPW) to GCPW hot via interconnect, designed for low-profile, high-density integration. Horizontal transmission line is explored in a low profile 3D integration structure. The whole interconnect structure with three-stacked MMICs was demonstrated to have the insertion loss within 0.65 dB and return loss below 20 dB from DC to 40 dB, where the hot-via and bump transitions only accounted for 0.19 dB loss. A single discontinuous vertical transition structure occupies only 0.16 square millimeters. The close agreement between the measurements and simulations validated the presented design approach for the transitions. The implementation of multi-layer GaAs substrate vertical stacking will further drive the potential to save plane integration area and improve performance, representing a highly suitable solution for electronic steering arrays constrained by lambda/2 spacing limitations for individual element areas. The

assembly method of this technology is essentially similar to the established 2.5D process, ensuring reasonable control over production costs.

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