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A Design Approach for High-Efficiency Hybrid Continuous Extended Inverse Class-F Broadband Power Amplifier Using Band-Pass Network Topology

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ABSTRACT: A hybrid continuous extended-mode inverse class-F power amplifier is designed with band-pass filtered matching networks to match transistor inputs. This design methodology increases the impedance space by incorporating free factors into the current equation of the traditional inverse class-F power amplifier (PA). The suggested matching network in this article is a reliable alternative to the commonly used low-pass structured matching network, and this synthesis method simplifies the deployment of the distributed network compared to the LC low-pass network. High efficiency is guaranteed by the constructed output band-pass matching network. To verify the validity and superiority of this design method, a broadband power amplifier operating at 2.6–4.0 GHz was designed and fabricated. Large-signal measurement results indicate that the drain efficiency (DE) ranges from 60% to 81%, 40–42.3 dBm output power, and 10.5–11.5 dB power gain across this frequency range.

1. INTRODUCTION

The swift progress of wireless communication technology, propelled by GaN technological breakthroughs and the evolution of broadband high-efficiency matching theory, has rendered the design of broadband high-efficiency power amplifiers a prominent research focus in recent years [1–3].

Many related research results have been published for use in the main candidate modes for realizing high-efficiency power amplifiers, which need to accurately control the voltage-current waveforms so that the voltage-current waveforms do not overlap as much as possible to improve the amplifier's efficiency. However, the bandwidth of amplifiers designed under stringent criteria is usually narrow. To solve the above problems, researchers have gradually proposed Class-J [4–7], continuous Class-F [8, 9], and continuous inverse Class-F [10–12] modes of operation. For example, [13] proposes a broadband high-efficiency class J power amplifier based on a multi-segment quarter-wavelength line and a short-circuited microstrip structure. Although the design approaches proposed in the above studies can realize high-performance power amplifiers, the disadvantage of insufficient design space limits the achievable operating bandwidth to some extent. In this paper, two free design parameters are added to the drain current expression of the conventional continuous inverse class F power amplifier to further improve the impedance design space for output matching. In addition, so far, many research organizations have demonstrated their broadband impedance matching networks [14–18], and the input-matching network synthesis methods and output-matching networks are invariably mostly LC low-pass ladder networks. However, such a design process is inappropriate since the input impedance of the transistor is constrained to be an LC impedance series resonance. As a result, the frequency characteristics of the optimum source impedance of the transistor are in many ways different from those of the most loaded impedance. In this paper, an attempt is made to discuss the problem of suitable broadband input matching through equivalent circuit approximation and nonlinear model validation.

Objectively, the key factor in ensuring that the design of the input matching network is not overly worrisome lies in the role of the output matching network, which primarily ensures good efficiency and output power over the entire frequency range. Input matching network, on the other hand, focuses on ensuring the stability of the system and the reliability of the gain performance [19]. Usually, poorer input matching has less impact on the efficiency and saturated output power of the system [20]. In this case, the traditional design focuses mainly on tuning the frequency response of the output network. However, the selected transistors need to achieve high efficiency at rated power, sufficient power output, minimize nonlinear distortion, and ensure gain uniformity over the frequency range while maintaining good input and output return loss (RL). To achieve these design goals, accurate input and output matching must be performed simultaneously. To effectively meet these requirements, the matching network needs to balance the dominant reactance constraints with an appropriate topology.

Therefore, in this paper, we propose a reasonable input structure based on the equivalent circuit approximation and equivalent modeling while adopting the inverse class-F mode of oper-

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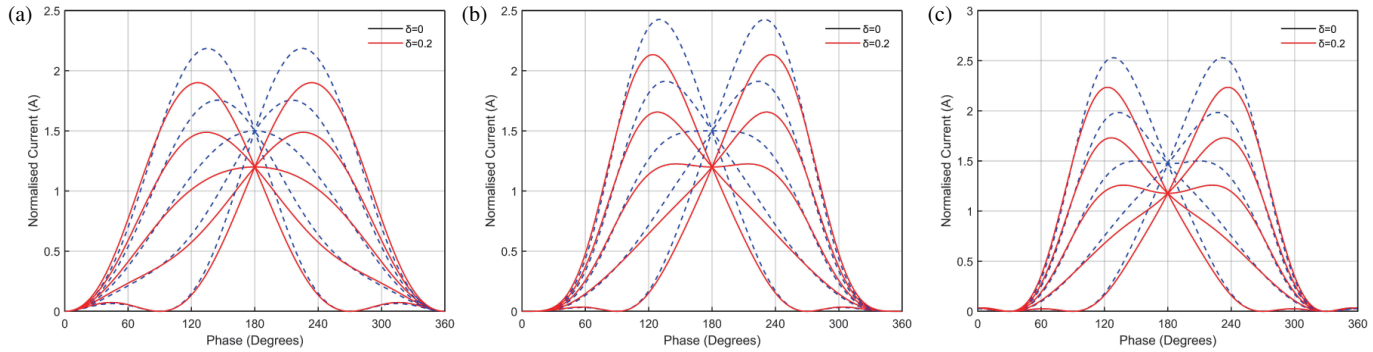

FIGURE 1. Hybrid continuous extended inverse F-class normalized drain current. (A) $\alpha = 1, \beta = 0$. (B) $\alpha = \frac{9}{8}, \beta = \frac{1}{8}$. (C) $\alpha = \frac{2}{\sqrt{3}}, \beta = \frac{1}{3\sqrt{3}}$.

ation to design a broadband (2.6–4 GHz) power amplifier. The proposed demonstration aims to achieve broadband operation within the octave bandwidth, taking into account impedance overlap and performance degradation issues. The proposed power amplifier shows good performance in terms of gain flatness (±1 dB) and gain (> 10 dB). As expected, a well-designed input matching network not only corrects gain fluctuations within the target bandwidth but also effectively suppresses gain at out-of-band frequencies, resulting in an excellent frequency response.

2. THEORETICAL ANALYSIS

2.1. Extended Hybrid Continuous Inverse Class-F Operating Mode

The extended expression for the current waveform of the continuous inverse class F power amplifier is given below:

$$I(\theta) = [i_{DC} - i_1\cos(\theta) + i_3\cos(3\theta)] \times [1 - \gamma\sin(\theta)] \times [1 + \delta\cos(\theta)] \quad (1)$$

In the above equation, I_{DC}, i_1, and i_3 denote the DC, fundamental, and third harmonic current components, respectively. $(1 - \gamma\sin(\theta))$ and $(1 + \delta\cos(\theta))$ are the reactance factors that change the conventional impedance design space. In this paper, the design factors are added to the above currents to further extend the impedance design space. The expression of the drain current extended to is as follows:

$$I(\theta) = \frac{i_{MAX}}{2} \times [1 - \alpha\cos(\theta) + \beta\cos(3\theta)] \times [1 - \gamma\sin(\theta)] \times [1 + \delta\cos(\theta)] \quad (2)$$

$$V(\theta) = V_{DC}\left[1 + \sqrt{2}\cos(\theta) + \frac{1}{2}\cos(2\theta)\right] \quad (3)$$

In Eq. (2), i_{MAX} is the maximum transistor current, and α and β are used as the real part coefficients of the fundamental and third harmonic currents. Since the expression satisfies the "Zero-Grazing" [21] condition, distortion and nonlinear effects are minimized. Therefore, α and β are also subject to the following relationship:

$$\begin{cases} \alpha - \beta = 1 & 1 \le \alpha \le \frac{9}{8} \\ \alpha\left[\left(\frac{2}{3} + \frac{2\beta}{\alpha}\right)\sqrt{\frac{1}{4} + \frac{\alpha}{12\beta}}\right] = 1 & \frac{9}{8} < \alpha \le \frac{2}{\sqrt{3}} \end{cases} \quad (4)$$

According to the "Zero-Grazing" [22] condition, it is deduced that the drain current is non-negative. Meanwhile, to ensure that the expanded continuous inverse F-type second harmonic impedance solution space is distributed within the Smith circle diagram, the value of δ should be restricted to be between 0 and 1, and γ should take the value of -1 to 1. To take a value greater than a certain drain efficiency, we take the upper limit of δ to be 0.2 and thus determine the range of values of γ and δ. Meanwhile, Eq. (3) shows the standard half-wave rectified sinusoidal voltage waveform at the peak of the second harmonic. Fig. 1 depicts the theoretical current waveforms for the case of α and β taken as boundary conditions with γ step of 0.5 and δ equal to 0 and 0.2, respectively. Both the fundamental and second harmonic conductances are kept constant, although changing the parameters leads to changes in the desired fundamental and second harmonic conductances. Using Eqs. (2) and (3), the fundamental conductance (Y_1), second harmonic conductance (Y_2), and third harmonic conductance (Y_3) are calculated from the voltage-current expressions as follows:

$$Y_2 = \delta(\alpha - \beta) + j\gamma(\delta - \alpha - \beta) \quad (5)$$

$$Y_1 = \frac{1}{\sqrt{2}}(\alpha - \delta) + j\frac{1}{\sqrt{2}}\gamma\left[1 - \frac{\delta}{4}(\alpha - \beta)\right] \quad (6)$$

$$Y_3 = \infty \quad (7)$$

Figure 2 demonstrates the impedance solution space for the extended hybrid continuum mode. In this section, the three boundary conditions in Eq. (4) are selected for the impedance solution space demonstration, while only the part with $0 \le \delta \le 0.2$ is shown. From Fig. 2, it can be seen that the third harmonic impedance is infinite in this mode, and the fundamental and second harmonics appear with variable real and imaginary parts, which further extends the design freedom.

By Eqs. (2) and (3), the expression for the drain efficiency of the extended hybrid continuous mode can be obtained as follows:

$$\eta_D = \frac{\sqrt{2}(\alpha - \delta)}{2 - \alpha\delta} \quad (8)$$

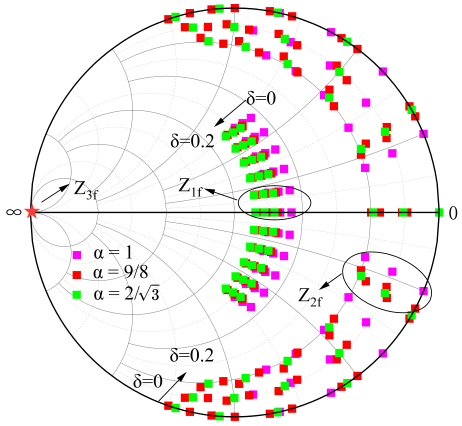

FIGURE 2. Theoretical fundamental, second harmonic, and third harmonic impedances for extended hybrid continuous inverse class-F mode.

Figure 3 shows the drain efficiency versus α and δ. The range of α was chosen to be 1–1.3, and the range of δ was chosen to be 0–0.3. As can be seen from the figure, the lowest drain efficiencies in this range are generally close to 60%.

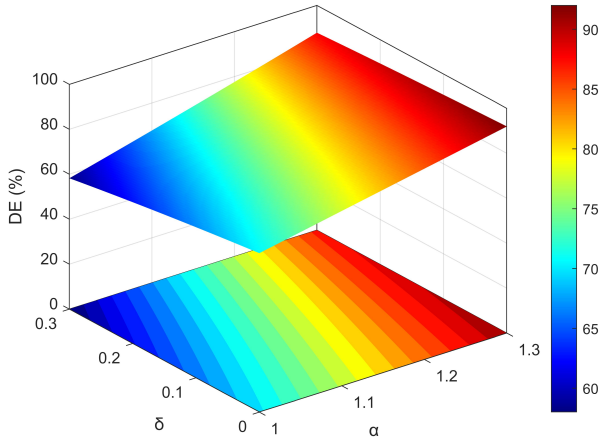

FIGURE 3. Drain efficiency varying with α and δ.

2.2. GaN Power Device Model Analysis

In this article, the GaN HEMT device equivalent model proposed in [22] is used. Although there may be some differences in circuit topology between the different models, it has become a widely accepted consensus to connect the gate-source capacitance (C_{GS}) in series at the input and the gate-drain capacitance (C_{GD}) in parallel at the output. A schematic of the simplified model is shown in Fig. 4.

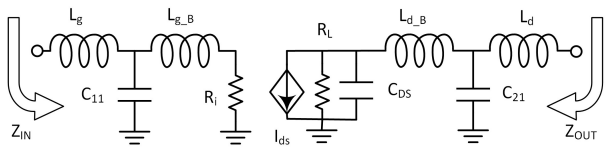

FIGURE 4. Schematic of the simplified GaN HEMT model.

In this model, the intrinsic parameters include the gate-source capacitance (C_{GS}) and gate-drain capacitance (C_{GD}), which are internal parameters typically affected by device bias conditions. The external parasitic parameters include parasitic inductances ($L_g, L_{g_B}, L_{d_B}, L_d$) caused by the gold wire from the electrode to the flange/pad, and parasitic capacitance (C).

On the input side, the main parasitic parameter is the capacitance (C_{GS}), while the parasitic capacitance (C_{11}) of the package has less effect on the circuit [21]. To achieve the best broadband matching effect, the input of the circuit diagram should have a series resonant structure and be designed as a broadband matching network with a band-pass structure to achieve the desired broadband matching at the input of the tube core. This band-pass type of matching circuit can effectively optimize the load matching of the resonant characteristics.

3. OUTPUT WIDE-BAND HIGH-EFFICIENCY HARMONIC NETWORK DESIGN

The matching network at the class F amplifier's drain output consists of three parts: a parasitic compensation circuit, a harmonic control network, and a band-pass filtering network. The parasitic compensation circuit and the broadband high-efficiency harmonic network in this class-F amplifier circuit will be discussed in depth next, and the circuit topology at the transistor output is shown in Fig. 5.

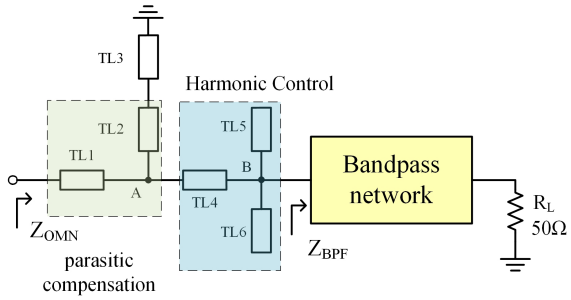

FIGURE 5. Extended hybrid continuous inverse class-F amplifier outputs.

In Fig. 5, the harmonic tuning network comprises TL4, TL5, and TL6 with lengths of $\lambda/4$, $\lambda/8$, and $\lambda/12$, respectively, where λ is the fundamental wavelength, and λ_1 and λ_2 are the fundamental wavelengths of the desired second harmonic to be suppressed. TL5 and TL6 cause a short-circuit at the second harmonic [23]. In the design, the electrical length of the transmission line TL4 is 180° and 270° at the second and third harmonic frequencies, which correspond to half wavelength at the second harmonic frequency and one-third wavelength at the third harmonic frequency. This design assures that the transmission line may transform the impedance from short-circuit to open-circuit at both harmonic frequencies.

To accomplish this, TL4 is used to convert short-circuit conditions at the second and third harmonic frequencies at point B into second harmonic short-circuit and third harmonic open-circuit conditions at point A. The electrical length of TL4 is accurately determined to guarantee that the desired impedance conversion occurs at the ideal frequency. In the extended con-

tinuous inverse Class-F mode, a wide tolerance range for the second harmonic impedance is allowed in the design, accommodating some mismatch in the lower frequency bands. This adaptable design approach helps to simplify the impedance matching requirements for the second harmonic. Therefore, 6 GHz and 9 GHz are selected as the two suppression frequencies, and the electrical lengths of TL4 and TL5 are designed based on these frequencies so that they are quarter-wavelengths of 3 GHz and 4.5 GHz, respectively [24].

Z_{fS1} and Z_{fS2} denote the input impedances from point B to TL6 and TL5, respectively. Their values can be calculated by the following equations:

$$Z_{f_{S1}} = -jZ_6 \cot \theta_6^{@f_1} \tag{9}$$

$$Z_{f_{S2}} = -jZ_5 \cot \theta_5^{@f_{S2}} \tag{10}$$

In the design, θ_6 and θ_5 denote the electrical lengths of transmission lines TL6 and TL5, respectively, and these lengths are set to quarter wavelengths corresponding to frequencies F_{s1} and F_{s2}. In addition, Z_6 and Z_5 are the characteristic impedances of TL6 and TL5, which are tuned as free parameters in the design.

Considering that the transistor's parasitic parameters may have an impact on performance, an L-shaped parasitic network is introduced in the design to compensate. This compensation is intended to improve the accuracy of large-signal tests. By adjusting the traction of the load, the optimum load impedance of the transistor is chosen to be $15.6 + j \cdot 13.8\,\Omega$. The filter network realizes the conversion of the real impedance, and $Z_{LPF} = 15\,\Omega$ is taken for ease of computation. According to the transmission line theory, the relationship between Z_{OMN} and Z_{BPF} in Fig. 5 is as follows:

$$Z_{\text{OMN}} = \frac{Z_1 Z_{\text{A}}(Z_2 - Z_1 \tan\theta_1 \tan\theta_{13}) + jZ_1 Z_2(Z_1 \tan\theta_1 - Z_2 \tan\theta_2)}{Z_2(Z_1 - Z_2 \tan\theta_1 \tan\theta_2) + jZ_{\text{A}}(Z_2 \tan\theta_1 - Z_1 \tan\theta_2)} \tag{11}$$

$$Z_{\text{A}} = \frac{-Z_{\text{BPF}} Z_5 Z_6 \cot\theta_5 \cot\theta_6}{-jZ_{\text{BPF}} Z_5 \cot\theta_5 - jZ_{\text{BPF}} Z_6 \cot\theta_6 - Z_5 Z_6 \cot\theta_5 \cot\theta_6} \tag{12}$$

4. DESIGN METHODS FOR MATCHING NETWORKS USING BAND-PASS TOPOLOGIES

4.1. Network Topology for Broadband Matching

Based on the input, the transistor circuit diagram can be approximated as an RLC series resonant circuit. The primary purpose of the matching network is to resonate with the transistor equivalent capacitance over the bandwidth. As a result, the best matching effect at the tube's input can be achieved using a matching network with a band-pass structure. As seen in Fig. 6, the left portion depicts the load with series resonance characteristics, while the right part represents the matching network with a band-pass structure that must be built and implemented.

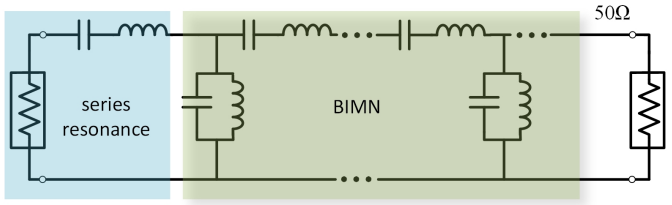

FIGURE 6. Schematic representation of band-pass network structure to achieve broadband matching.

4.2. Synthesizing BIMN Using Band-Pass Prototype

The selected source impedance through the source traction is $Z_S = 15 + j \cdot 9\,\Omega$, and since the bandpass network assumes the matching from real to real impedance, $R = 15\,\Omega$ load is selected for the design. In short, the matching network is to be matched to $50\,\Omega$ at the design frequency.

The prototype low-pass matching network is shown in Fig. 7(a). The normalized conductance elements of the prototype low-pass matching network can be calculated using the equations in [25] and [26]. The factor, $Q = R_0 W_0 C_{\text{out}}$, where $W_0 = \sqrt{W_1 W_2}$, W_1 and W_2 are the lower and upper band edge corner frequencies.

Element g represents a low-pass filter in a 1-Ω system with a corner frequency of 1 rad/s [26]. The low-pass prototype network corner frequency is scaled from the rated 1 rad/s to the design value w_0 by dividing elements g_1, g_2, and g_3 by $(W_2 - W_1)$. Impedance calibration is then applied by multiplying shunt elements g_1 and g_3 by $\frac{1}{R_0}$ and series elements g_0, g_2, and g_4 by R_0. The low-pass network is then converted to a band-pass network by resonating two times of the frequency on each series or shunt element. Fig. 7(b) shows the final values of the bandpass network elements after frequency and impedance scaling. To scale the termination resistor upwards to $50\,\Omega$, the Norton transformation is used as it enables the insertion of an ideal transformer into the network without affecting the bandwidth. The impedance of the inductor L_3 and termination resistor is scaled upward by factor n^2. Using Norton transform, the two capacitors are transformed into a Π-capacitor arrangement, and the transformed circuit is shown in Fig. 7(c).

4.3. Distributed Band-Pass Structure Matching Network

The grounded resonant shunt L-C can be represented by a grounded quarter-wavelength transmission line stub. The characteristic impedance of the transmission line truncation is equal to the reactance of the inductor or capacitor multiplied by $\pi/4$. Due to the problem of the maximum transformation rate of the Norton transformation mentioned at the end of Subsection 4.2, the C_4 transformation in Fig. 7(c) is calculated to be negative. It is discovered that the S-parameter structure of the filtering network continues to follow the design after it is discarded, and finally, the band-pass network is optimized to the topology shown in Fig. 7(d).

The complete input-matching network is obtained by the above transformations. Since the transformations are all based on approximate formulas, we need further fine-tuning and optimization on the simulation software, and the dimensions are

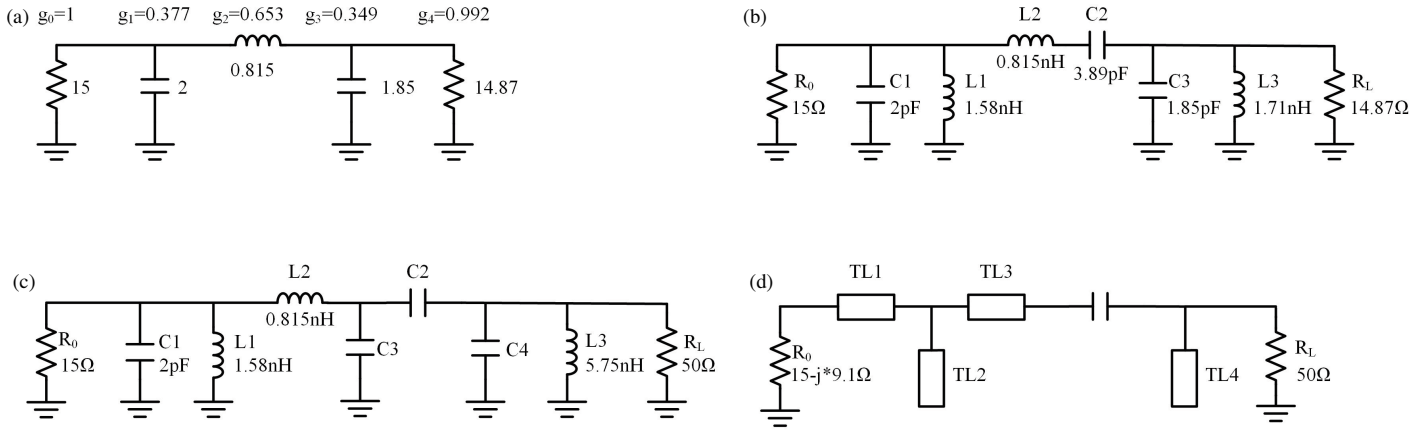

FIGURE 7. Stepwise aggregate matching network design and its equivalent distribution network: (a) Low-pass network; (b) Band-pass network; (c) RL upward impedance transformation to 50 Ω and Norton transformation; (d) Distribution network.

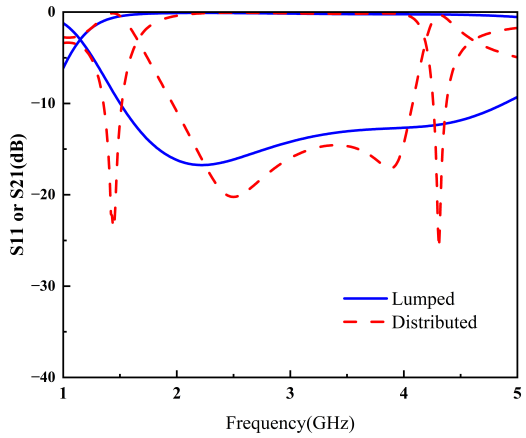

FIGURE 8. Insertion loss and return loss for the lumped output matching network and its corresponding distributed network.

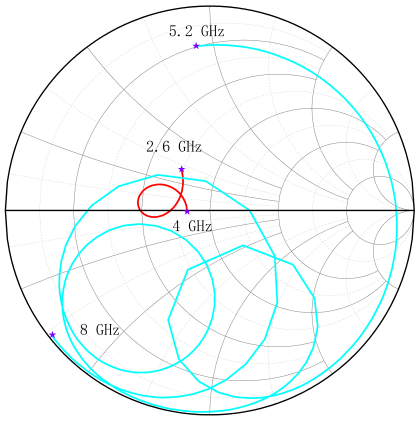

FIGURE 9. Simulated impedance at I-gen plane of the designed output matching network.

slightly modified. Fig. 8 compares the insertion loss and reflection loss of the simulation case set total element matching network and distributed network. The real transmission line has a higher network loss than the ideal transmission line due to substrate and material loss. At this point, the outputs have all been designed.

Figure 9 displays impedance traces for microstrip-based and lumped element output matching networks. It is clear that the OMN's simulated impedance at the I-gen plane is in or close to the goal design space, consistent with the extended continuous inverted class-F mode described in Section 2.

5. POWER AMPLIFIER DESIGN AND REALIZATION

The inputs are matched by a band-pass matching network, and the outputs follow the structure shown in Fig. 5. The equivalent optimization parameters of the transmission line may be derived using the preceding theoretical analysis, and the complete circuit is depicted in Fig. 10. To verify the theory, a 2.6–4.0 GHz power amplifier using a CGH40010F transistor ($\varepsilon_r = 3.66$, $H = 0.762$ mm) on a Roger 4350B substrate was designed and fabricated. The drain and gate bias values were 28 and −2.7 volts, respectively. Fig. 11 shows an actual image of the designed PA.

The small signal experimental configuration-1, which includes a vector network analyzer, DC current, and attenuator, is critical for measuring S-parameters, as illustrated in Fig. 12. Fig. 13 illustrates a measurement arrangement for analyzing large-signal performance. The device consists of an RF signal generator, amplifier driver, DC power supply, attenuator, power meter, and spectrum analyzer. The RF signal generator generates an input signal containing both continuous wave (CW) tones and modulated signals. The spectrum analyzer evaluate parameters of the PA.

6. SIMULATION AND MEASUREMENT RESULTS

The proposed power amplifier was simulated using Agilent Advanced Design System (ADS) software. The small signal S-parameter tests were performed using an R&S vector network analyzer 3674. The large-signal response was measured with a CeYear signal generator 1441B and spectrum analyzer 4037MD.

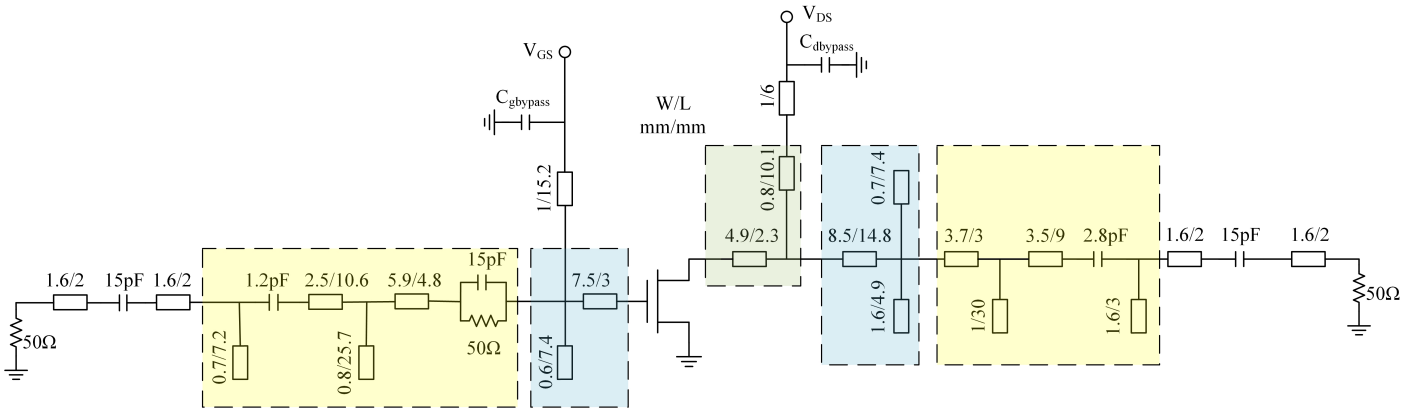

FIGURE 10. Simulated impedance at I-gen plane of the designed output matching network.

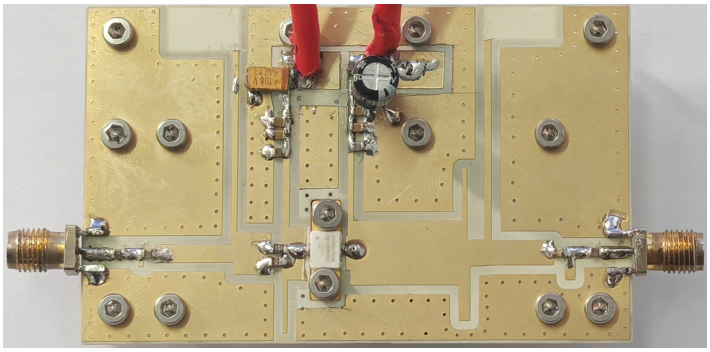

FIGURE 11. Proposed broadband, highly efficient FPA.

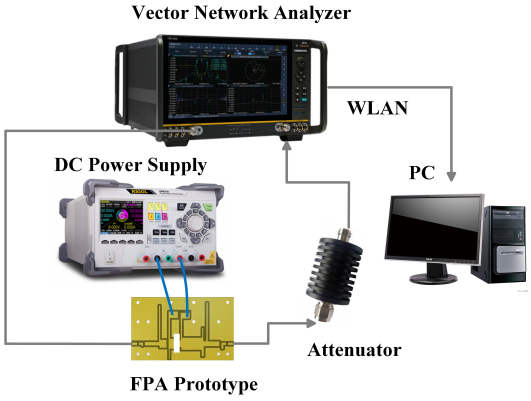

FIGURE 12. Photograph of the implemented PA and testing environment.

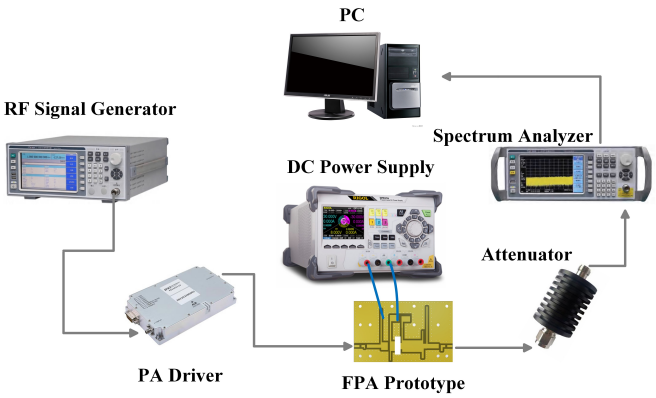

FIGURE 13. Photograph of the implemented PA and testing environment.

Figure 15 shows the simulated and measured drain voltage and current waveforms of the designed power amplifier at two frequencies: 2.8 GHz and 3.6 GHz. From the results, it can be seen that there is almost no overlap between the two waveforms, and they are similar to the theoretical waveforms. The small-signal S-parameters of the designed amplifier are shown in Fig. 15.

The S-parameter tests are carried out based on bias voltage $V_{gs} = -2.7V$, $V_{ds} = 28V$. By measuring the proposed power amplifier using continuous signals, the simulation and measurement results are shown in Fig. 16. The simulation results show that the output power is 40.3–42.7 dBm; the drain efficiency is 61.4%–82.1%; and the gain is 9.4–10.5 dB at the required 2.6–4 GHz, respectively. In addition, the variation of drain efficiency and gain with output power is shown in Fig. 17. It can be seen that the measured output power in the range of 2.6–4 GHz is between 40 and 42.8 dBm, and the measured gain ranges from 10.5 to 11.5 dBm. Additionally, the drain efficiency varies be-

TABLE 1. Research status and comparison of broadband power amplifiers.

Reference	Matching[a] Algorithm	Operation[b] Mode	Freq/FB[c] (GHz)/(%)	GF[d] (dB)	Gain (dB)	Eff[e] (%)
[4]	LP/LP	CE	2.5–3.6/36	±1.5	10–13	55-83P
[5]	LP/LP	CCF	1.4–3.6/88	±2.5	13–18	56-79P
[6]	LP/LP	HT	2.0–3.5/54	±2	12–16	64-76D
[7]	RFT LP	n/a	0.3–1/107	±2	12.3–15.3	62-81D
[8]	RFT LP	CCF	21.1–48.2/78	±3	15.3–18.3	24-32P
[9]	RFT LP	n/a	25–35/33	±1.5	7–10	46-51P
This work	BP/BP	ECCF-1	2.6–4/42	±0.5	10.5–11.5	60-81D

[a]Matching algorithm: LP and BP denote low-pass and band-pass topology.
[b]Operation mode. CE: Class E; CCF: continuous Class F; HT: harmonic tune; ECCF: Extended continuous inverse class-F^{-1}.
[c]Freq: Operating frequency; FB: fractional bandwidth.
[d]GF: Gain flatness.
[e]Suffix P means PAE; suffix D means drain efficiency.

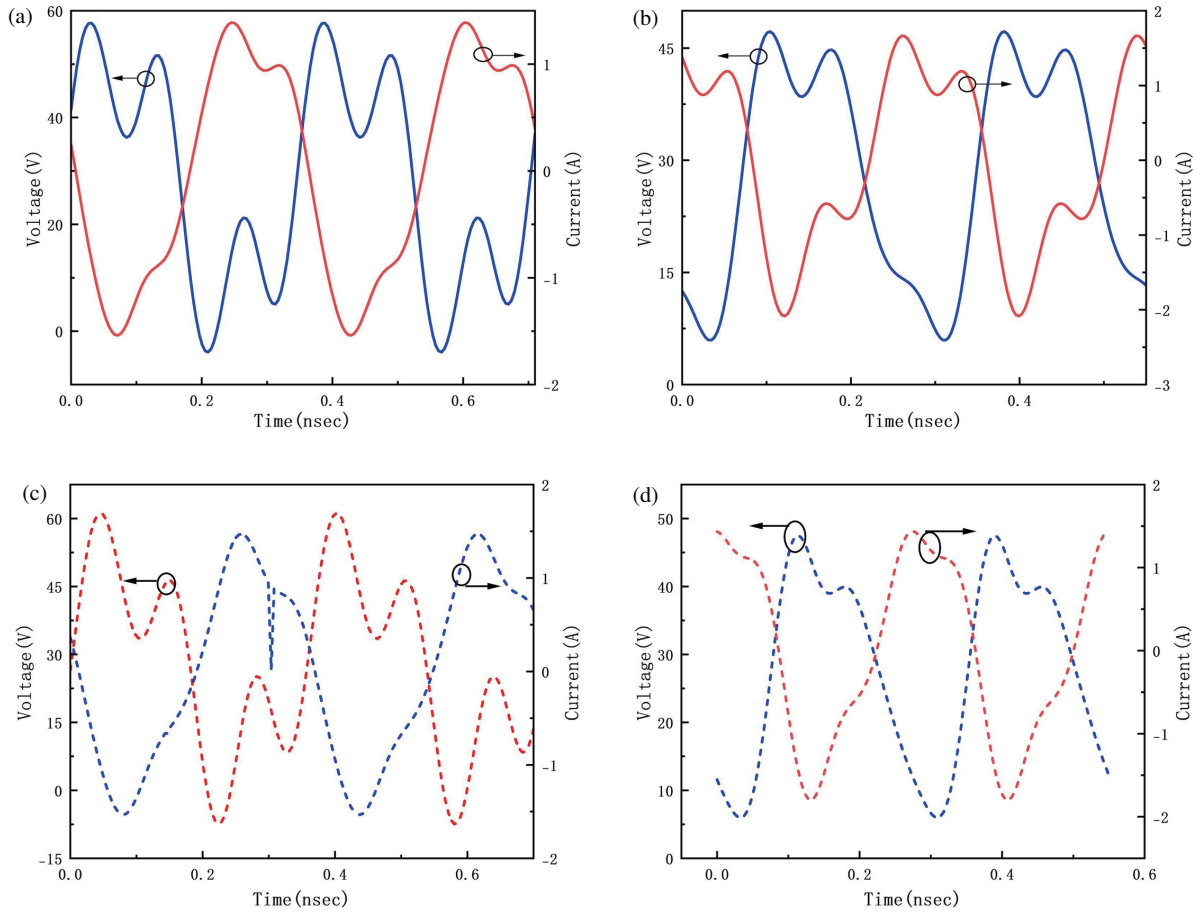

FIGURE 14. Simulated (solid line) and measured (dashed line) waveforms of drain voltage and current of the designed power amplifier at certain operating frequencies: (a) 2.8 GHz; (b) 3.6 GHz. (c) 2.8 GHz; (d) 3.6 GHz.

tween 60% and 81%. It can be visualized that the measured results are very close to the simulated ones, probably due to small differences in manufacturing and soldering processes. To show the linearity of the designed amplifier, the amplifier is driven by a 20 MHz LTE signal with a peak-to-average ratio of 7.5 dB. As can be seen in Fig. 18, the designed amplifier has a better adjacent channel leakage ratio (ACLR) than 30.7 dBc over the entire operating bandwidth. The designed broadband power amplifier is compared with previous publications, as shown in Table 1. This paper produces the smallest gain variation and good input and output load impedance in the passband, which

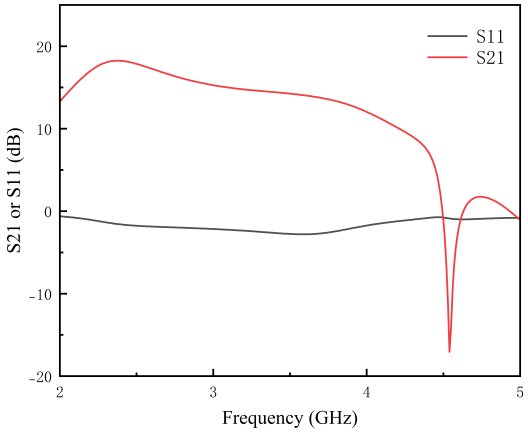

FIGURE 15. Measured small-signal S-parameters of the power amplifier.

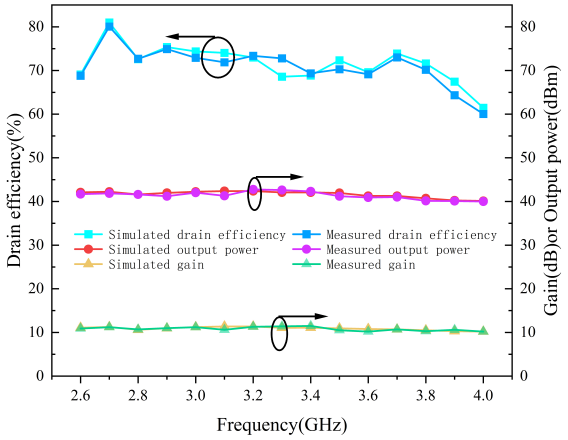

FIGURE 16. Simulated and measured drain efficiencies, output powers, and large-signal gains over the entire frequency band.

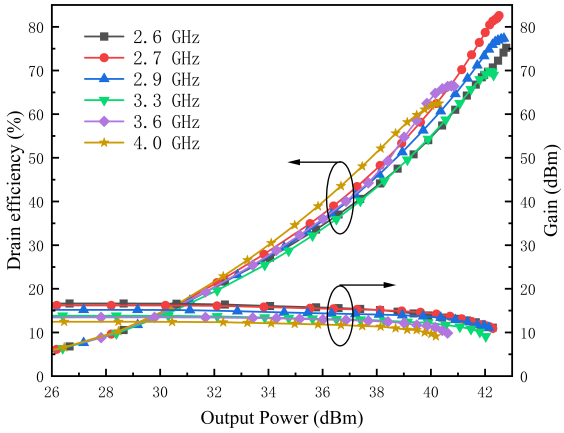

FIGURE 17. Measured gain and drain efficiency relative to output power at different frequencies.

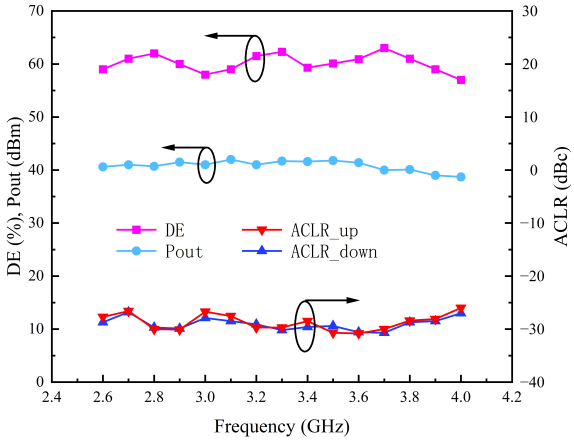

FIGURE 18. ACLR, Pout, and DE.

confirms the effectiveness of the band-pass matching network of the proposed.

7. CONCLUSION

This paper investigates a design methodology for a broadband extended hybrid continuous inverse class-F power amplifier. By combining the broadband design with the extended hybrid-continuous mode, the impedance design space is significantly broadened. In addition, the proposed band-pass matching network not only ensures good impedance transformation at the center frequency but also improves the quality of input matching. This design achieves smaller gain fluctuation and excellent reflection loss performance. The experimental results validate the excellent performance of the designed power amplifier and support the validity of the theory in this paper.

DECLARATION OF COMPETING INTEREST

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