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Design of Mode-Reconfigurable Doherty Power Amplifier

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ABSTRACT: This paper proposes a mode-reconfigurable Doherty power amplifier (DPA). By merely exchanging the transistors' gate bias without altering the corresponding circuits, this power amplifier can achieve two different frequency-band DPA modes, enabling wide bandwidth implementation in DPAs utilizing a single load modulation network. Simultaneously, PIN switches are utilized to improve the amplifier's bandwidth and drain efficiency during mode switching. To validate this approach, a mode-reconfigurable DPA was designed and fabricated using commercial GaN transistors. A reconfigurable Doherty power amplifier with Mode 1 operating in the frequency bands of 2.5–2.9 GHz and 3.3–3.7 GHz, Mode 2 operating in the frequency band of 2.8–3.4 GHz, with a drain efficiency ranging from 60.2% to 70.2%, a 6 dB output power reduction resulting in a drain efficiency of 43.5% to 53.7%, a gain between 9.4 and 11.3 dB, and a saturated output power between 39.4 and 41.3 dBm. This straightforward architecture offers a promising approach for implementing Doherty power amplifiers in 5G frequency bands.

1. INTRODUCTION

The need for communication systems with high average power efficiency is growing as 5G mobile communication systems are developed. To increase system average power efficiency, radio frequency power amplifiers need to be highly efficient at power back-off levels. Many methods have been developed in recent decades to increase the back-off power efficiency of radio frequency amplifiers. Since its initial introduction [1], the Doherty Power Amplifier (DPA) has emerged as one of the most widely used topologies in modern wireless transmitters, particularly in applications involving cellular base stations [2–5]. After years of research and development, most Doherty power amplifiers now cover 3G and 4G frequency bands [6–10]. Next-generation wireless communication systems (5G) also expect Doherty power amplifiers to operate across extensive 5G frequency ranges. To support multi-mode/multi-band operation, bandwidth extension techniques for Doherty power amplifiers have attracted significant attention in recent years. The bandwidth of Doherty power amplifiers can be significantly increased by using technologies like post-matching networks [7–9], integrated compensatory reactance [10], and continuous-mode operation [11, 12]. The development of broadband load modulation networks is the primary objective of these techniques. Architectural-level bandwidth expansion has also been investigated, including bias-adaptive methods [13] and dual-input arrangements [2, 3]. Other average efficiency enhancement methods like Load-Modulated Balanced Amplifiers (LMBAs) [14] and multi-transistor combined DPAs [15] have extended bandwidth beyond 3 GHz to meet 5G requirements. Nevertheless, the bandwidth of Doherty amplifiers remains constrained, making it challenging to design high-efficiency DPAs covering the full 5G spectrum. In this context, reciprocal gate biasing to increase the applicability and bandwidth of DPA Pang was suggested [16–18].

In order to increase operational bandwidth into multi-gigahertz levels, this research proposes a mode-reconfigurable Doherty amplifier architecture. The results show that a single broadband load modulation network can use a pair of reciprocal gate biases to enable mode-reconfigurable functioning over two frequency bands without requiring circuit alterations if it is designed properly. Commercial GaN devices were used to implement a DPA prototype, achieving Mode 1 bandwidth of 2.5–2.9 GHz/3.3–3.7 GHz and Mode 2 bandwidth of 2.834 GHz. PIN switches were employed during mode switching to enhance amplifier bandwidth and drain efficiency. The fabricated power amplifier demonstrates excellent performance in both designed modes, with each mode exceeding one-octave bandwidth. The combined bandwidth of the dual-mode DPA nearly covers all 5G frequency bands allocated to Chinese telecom operators.

2. THEORETICAL ANALYSIS

Doherty amplifiers conventionally link two amplifiers at their output via a load modulation network [19–21]. Traditional designs typically bias one amplifier (the carrier amplifier) in Class AB and the other (the peak amplifier) in Class C. At elevated input power levels, both amplifiers work in tandem to supply power to the load. Under lower input conditions, the only active component is the carrier amplifier. As input power drops, the load modulation network must modify the carrier amplifier's load resistance to maintain efficiency during power back-off. However, intrinsic circuit constraints make it difficult to achieve optimal impedance matching across broad bandwidths in a single operational mode of a Doherty amplifier.

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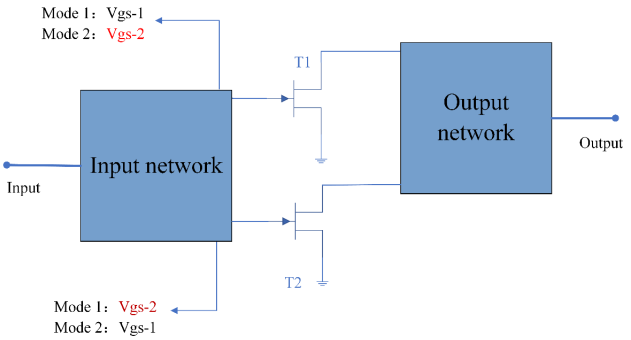

FIGURE 1. Conceptual diagram of mode-reconfigurable power amplifier.

In this paper, we suggest a basic broadband modereconfigurable Doherty power amplifier architecture, as shown in Figure 1 whose central concept lies in enabling Doherty functionality across distinct frequency bands and modes by adjusting the gate bias voltages ($V_{\mathrm{GS}-1}$ and $V_{\mathrm{GS}-2}$) of two identical transistors without altering the circuit, as illustrated in Figure 2. In Mode 1, transistor T1 operates in Class AB as the carrier amplifier with $V_{\mathrm{GS}-1}$ bias, while T2 functions in Class C as the peak amplifier under $V_{\mathrm{GS}-2}$ bias. In Mode 2, the same matching network is retained, but reversing the gate biases swaps the roles of T1 and T2 — T1 becomes the peak amplifier, and T2 acts as the carrier amplifier. The load modulation network exhibits distinct frequency responses in each mode. Through careful design, the amplifier can target mid-band frequencies in Mode 2 and cover the remaining edge bands in Mode 1, enabling an extended composite bandwidth for the Doherty power amplifier, as illustrated in Figure 2.

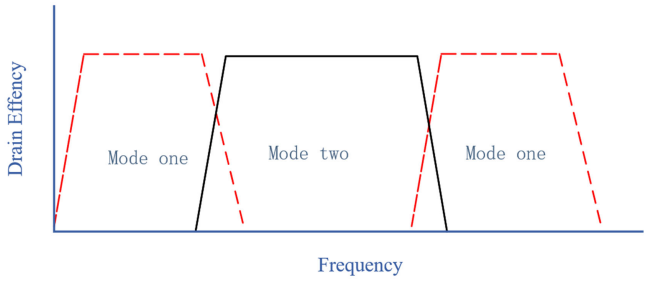

FIGURE 2. Ideal frequency band diagram.

The proposed architecture implements a symmetrical topology with dedicated generalized Output Matching Networks (OMNs) allocated to carrier and peak amplifiers, respectively, as depicted in Figure 3 using current generator (CG) representations for both transistors. Under the analytical premise of fully incorporating transistor parasitic and packaging parameters into OMN equivalency, two distinct operational configurations are established: In Mode 1, CG1 serves as the carrier device biased in Class AB mode while CG2 acts as the peak device biased in Class C mode. Conversely, in Mode 2, CG1 becomes the peak amplifier, and CG2 functions as the carrier amplifier.

Assuming that the OMN can achieve Z_T-to-Z_T matching within the design frequency band, with θ_{M1} and θ_{M2} representing the phase shifts of OMN1 and OMN2, respectively. A

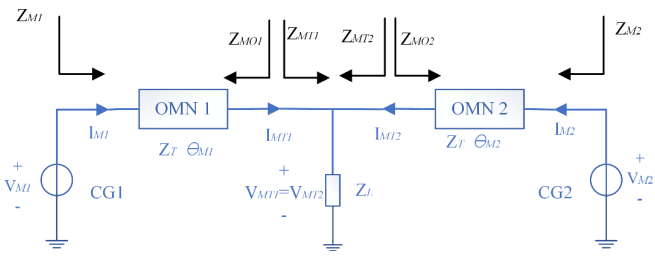

FIGURE 3. Load network of the DPA.

lossless OMN's $ABCD$ matrix can be explained as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_T \sin\theta \\ j\frac{\sin\theta}{Z_T} & \cos\theta \end{bmatrix} \tag{1}$$

where the ideal load impedance for Class-B power amplifier operation, R_{opt}, is set for Z_T. Equation (2) can therefore be used to define the voltage-current relationship between the combining node and current generator (CG) plane.

$$\begin{bmatrix} V_M \\ I_M \end{bmatrix} = \begin{bmatrix} \cos\theta_M & jZ_T \sin\theta_M \\ j\frac{\sin\theta_M}{Z_T} & \cos\theta_M \end{bmatrix} \begin{bmatrix} V_{MT} \\ I_{MT} \end{bmatrix} \tag{2}$$

From Equation (2), the current of the current source can be obtained as:

$$I_M = V_{MT} \cdot (j \sin\theta_M / Z_T) + \cos\theta_M \cdot I_{MT} \tag{3}$$

Meanwhile, the voltage of the combined node is:

$$V_{MT} = (I_{MT1} + I_{MT2}) \cdot Z_L \tag{4}$$

Z_L, which is equivalent to $Z_T/2$ in formula (4), is the combined load of the two branches.

The symmetrical Doherty operation requires equal phase merging at the merged nodes during saturation. The following present relationship needs to be completed:

$$I_{MT2,sat} = I_{MT1,sat} \tag{5}$$

From Formulas (3) to (5), we can obtain:

$$I_{MT,sat} = I_{MT,sat} \cdot (\cos\theta_M + j \sin\theta_M) = I_{MT,sat} \cdot e^{j\theta_M} \tag{6}$$

Therefore, whether it is Mode 1 or Mode 2, the following relationship should be satisfied by the currents produced by CG1 and CG2:

$$I_{M1,sat} = I_{M2,sat} \cdot e^{j(\theta_{M1} - \theta_{M2})} \tag{7}$$

From Equation (7), it can be seen that by adding a phase compensation network with a phase shift of (θ_{M1}-θ_{M2}) at the input end of CG1, the conditions for combining saturation and equalization can be satisfied for both Mode 1 and Mode 2.

The load impedance at the combination node can be computed as follows once Equation (5)'s equal-phase combination requirement is met:

$$Z_{MT1,sat} = Z_{MT2,sat} = Z_T \tag{8}$$

The matching impedance at Z_M can be expressed as:

$$Z_M = \frac{Z_{MT}A + B}{Z_{MT}C + D} \tag{9}$$

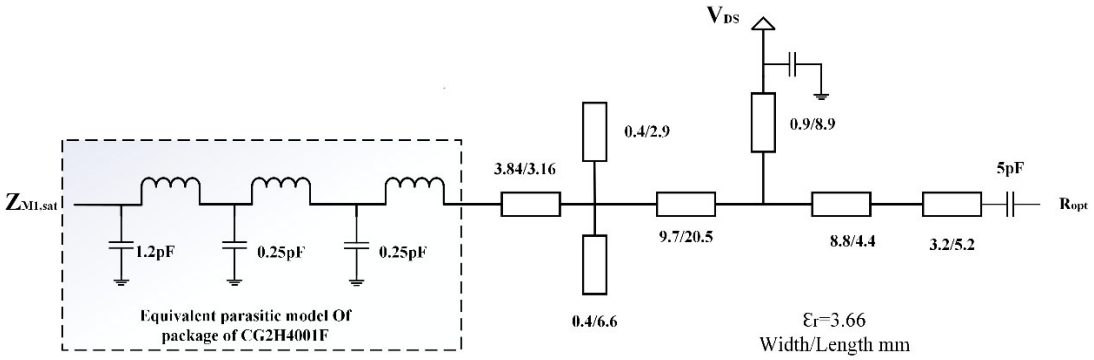

FIGURE 4. EQWN design circuit.

The load impedance of each amplifier branch prior to the combiner is denoted by Z_{MT} in the formula. When (1) is substituted into (9) the result is:

$$Z_{M1} = \frac{Z_{MT1} + jZ_T \tan\theta_{M1}}{Z_T + jZ_{MT1} \tan\theta_{M1}} \tag{10}$$

$$Z_{M2} = \frac{Z_{MT2} + jZ_T \tan\theta_{M2}}{Z_T + jZ_{MT2} \tan\theta_{M2}} \tag{11}$$

Among them, Z_{M1} and Z_{M2} are the matching impedances of OMN.

Substituting Equation (8) into Equations (10) and (11), we can obtain:

$$Z_{M1,sat} = Z_{M2,sat} = Z_T \tag{12}$$

This suggests that the requirements for Doherty saturation are met since the impedances needed for the carrier branch and peak branch are both equal to R_{opt}.

In Mode 1, only CG1 operates during the back-off state of the Doherty power amplifier, while CG2 is not yet activated and remains open-circuited. The impedance of the CG1 branch, $Z_{MO1,bo}$, is given by Z_L in parallel with $Z_{MO2,bo}$, where $Z_{MO2,bo}$ symbolizes the CG2 branch's output impedance. This can be stated as follows:

$$Z_{MO2,bo} = Z_T \frac{1}{j\tan\theta_{M2}} \tag{13}$$

Substituting Formula (13) into Formula (10), we can obtain the backtracking matching impedance $Z_{M1,bo}$ as:

$$Z_{M1,bo} = Z_T \frac{1 - \tan\theta_{M1}\tan\theta_{M2} + j2\tan\theta_{M1}}{2 + j\tan\theta_{M1} + j\tan\theta_{M2}} \tag{14}$$

To satisfy the operating conditions of the Doherty amplifier, $Z_{M1,bo}$ should match 2 R_{opt}. The phase of the OMN (Output Matching Network) is frequency-dependent. Assume that the center frequency corresponds to $\theta_{M1} = -90°$ and $\theta_{M2} = -180°$. By sweeping θ_{M1} and θ_{M2} with normalized frequency, the relationship between the normalized resistance and normalized frequency of $Z_{M1,bo}$ can be observed, demonstrating that the DPA can operate over a wide frequency band.

CG1 serves as the peaking device and CG2 as the carrier device in Mode 2. Equation (12) is satisfied even at saturation because of the proposed DPA's symmetric structure. The CG1 branch is shut off during back-off, and the carrier branch switches to the CG2 branch. Consequently, $Z_{MT2,bo} = Z_L/Z_{MO1,bo}$, where $Z_{MO1,bo}$ can be expressed as:

$$Z_{MO1,bo} = Z_T \frac{1}{j\tan\theta_{M1}} \tag{15}$$

Substituting Formula (15) into Formula (11), the backtracking matching impedance $Z_{M2,bo}$ of Mode 2 can be calculated as follows:

$$Z_{M2,bo} = Z_T \frac{1 - \tan\theta_{M1}\tan\theta_{M2} + j2\tan\theta_{M2}}{2 + j\tan\theta_{M1} + j\tan\theta_{M2}} \tag{16}$$

As mentioned earlier, in the proposed DPA, when switching from Mode 1 to Mode 2, we only switch the bias without altering the circuit. Therefore, θ_{M1} and θ_{M2} remain unchanged. If we perform a normalized frequency sweep on θ_{M1} and θ_{M2} again to observe the relationship between the normalized resistance and normalized frequency of $Z_{M2,bo}$, although the PA cannot function as a Doherty in the central frequency band, the output impedance at each sideband can still approach the optimal values. This allows the Doherty operation to be maintained at the sidebands.

3. DESIGN OF MODE-RECONFIGURABLE DOHERTY AMPLIFIER

The GaN CGH40010F transistor from Cree is used in the suggested DPA based on the aforementioned hypothesis because of its exceptional performance at frequencies higher than 4 GHz. A 0.508 mm Rogers4350 substrate with a dielectric constant of 3.66 is used to build the DPA. 28 V is the set value for the drain supply voltage. Initially, the device's package parasites are eliminated. Figure 4 shows the circuit used to simulate parasitics and packaging. The capacitance and inductance values of the device across the 2.0–5.0 GHz frequency range are estimated to be 1.2 pF, 0.55 nH, 0.25 pF, 0.1 nH, 0.25 pF, and 0.1 nH, respectively, using load-pull simulations and S-parameter analysis of the transistor when the device is off. The estimation techniques are detailed in [22–24]. Additionally, the transistor's knee voltage is estimated to be 4.5 V, and the maximum drain current is 0.75 A. The R_{opt} is calculated as 50 Ω.

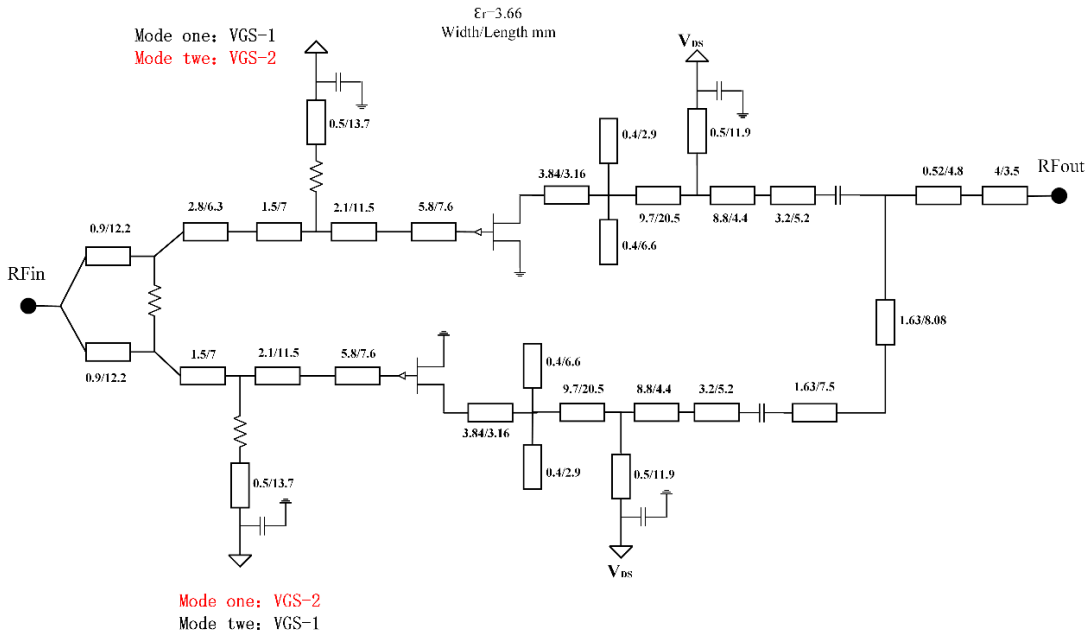

FIGURE 5. The schematic of the power amplifier.

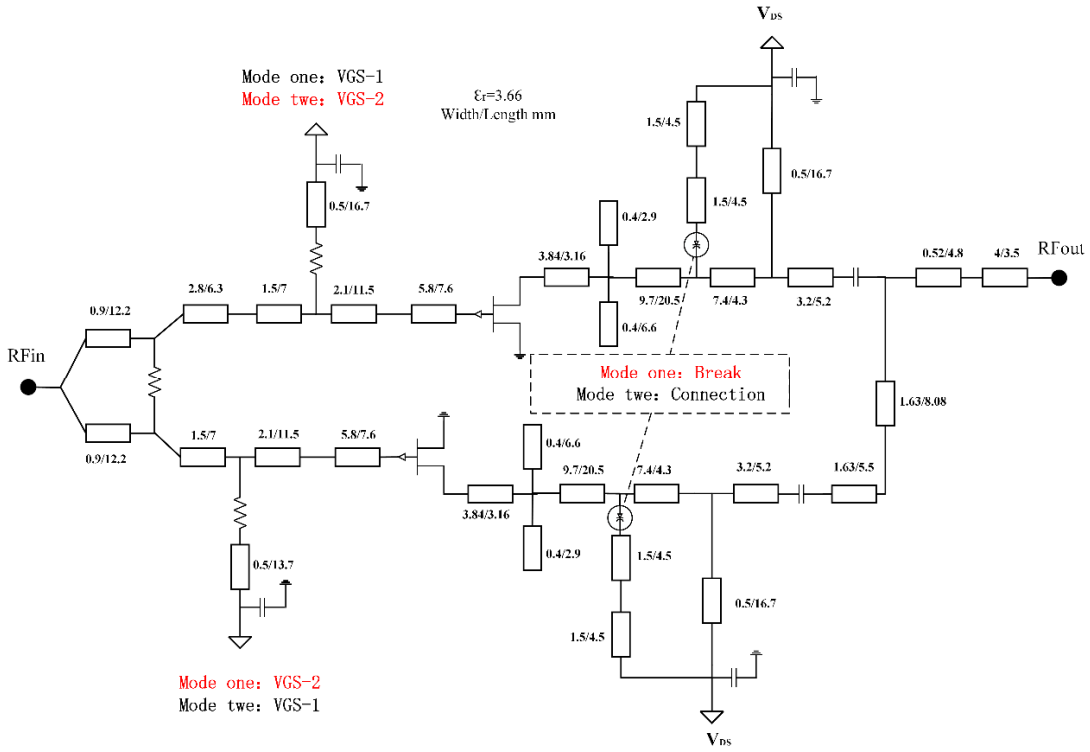

FIGURE 6. The schematic of the improved power amplifier.

Figures 5 and 6 display the schematic schematics of the mode-reconfigurable DPA and the enhanced one, respectively.

First, considering the parasitic parameters of the transistor, the equivalent wideband network (EQWN) is designed as OMN1 using a stepped microstrip line structure, as shown in Figure 5. Since the EQWN's matching target is simple in this design, the precise characteristics of the microstrip lines within the EQWN are immediately adjusted to provide the target matching impedance and intended phase range when the load values at R_{opt} are the same. As shown in Figure 6, the same EQWN circuit is used for OMN2, but a microstrip line with a characteristic impedance of R_{opt} is added to adjust the phase of OMN2. Both OMN1 and OMN2 incorporate the drain bias lines of T1 and T2. Figure 6 lists all of the microstrip

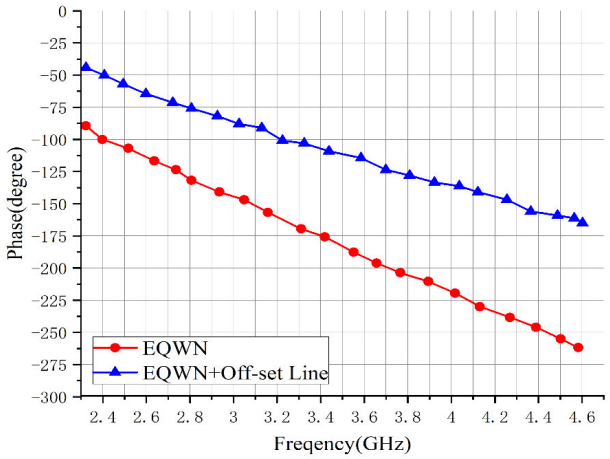

FIGURE 7. Phase shift of OMN1 and OMN2.

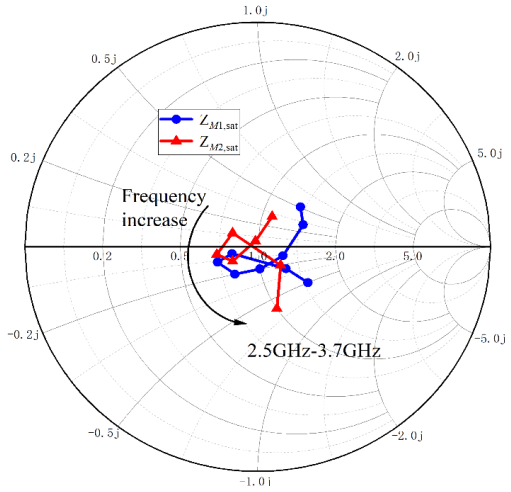

FIGURE 8. EM simulation results of OMNs matching impedance when its load equals R_{opt}.

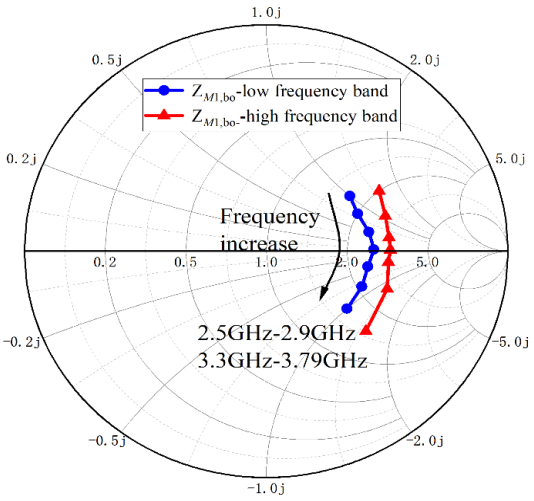

FIGURE 9. Findings from the EM simulation of the Mode 1 back-off impedance of the proposed DPA.

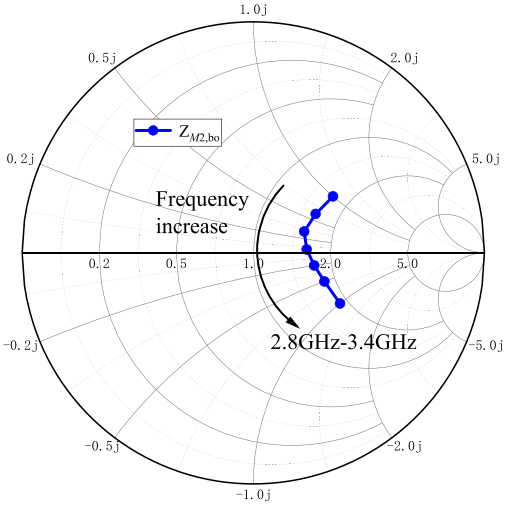

FIGURE 10. Findings from the EM simulation of the Mode 2 back-off impedance of the proposed DPA.

lines' widths and lengths. Figure 7 presents the phase shifts of OMN1 and OMN1 combined with the offset line (OMN2). As observed in Figure 7, OMN1 exhibits a phase range of $-45°$ to $-163°$ across the target frequency band. For OMN2, the phase range spans from $-84°$ to $-263°$. The designed phase ranges of both networks closely align with the required specifications.

The Smith chart in Figure 8 displays the matching impedances of OMN1 and OMN2 when R_{opt} is selected as the simulated load impedance. Furthermore, R_{opt} is used as the reference impedance. Figure 8 illustrates that in the 2.5–3.7 GHz frequency range, OMN's matching impedance is close to R_{opt}.

After designing OMN1 and OMN2, a post-matching network employing a stepped transmission line (TL) structure is designed to achieve a 50 to $R_{opt}/2$ match within the target frequency band. The back-off impedances of the carrier branches for Modes 1 and 2 can be determined when these networks are put into operation. The simulated impedances in the back-off zone are displayed in the Smith chart in Figures 9 and 10. The impedances are clearly situated near the region indicated by the output power contour lines.

Secondly, as the proposed dual-mode DPA relies on reciprocal gate biasing to enable its two operational modes, identical input matching networks (IMNs) are shared between the two amplifier modules to support operation in Mode 1 and Mode 2. To address phase discrepancies between OMN1 and OMN2, a 50-ohm microstrip line is inserted prior to T1's IMN. Figure 6 shows the integrated power divider schematic in detail. The complete DPA was simulated electromagnetically (EM) using Keysight's ADS Momentum, with gate bias voltages set to -3.1 V (VGS-1) and -6.2 V (VGS-2) and a quiescent current of 68 mA. Circuit dimensions were iteratively optimized to improve DPA performance. Simulation results for both modes (Figure 11) reveal that Mode 1 operates across 2.8–3.4 GHz, while Mode 2 spans 2.5–2.9 GHz and 3.3–3.7 GHz. Notably, within Mode 1's frequency range, the Doherty behavior appears weakly defined, and drain efficiency remains suboptimal. This inefficiency may arise from challenges such as insufficient out-

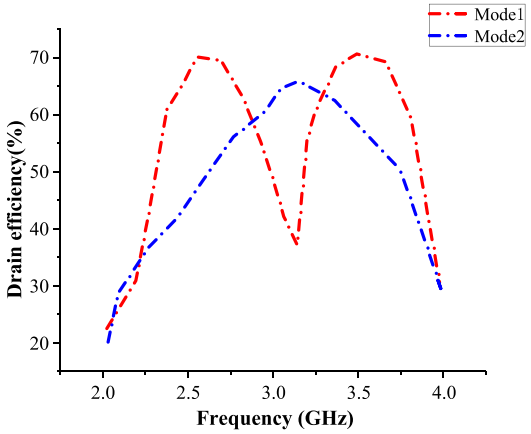

FIGURE 11. Efficiency diagram of dual-mode amplifier.

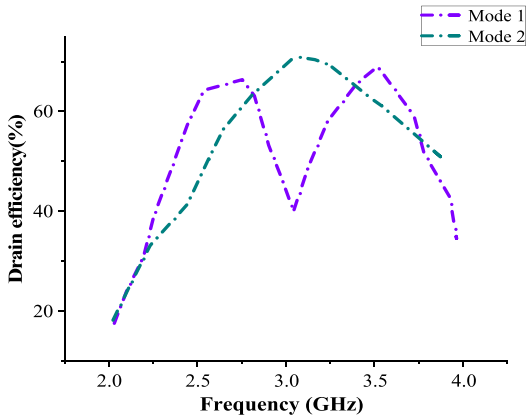

FIGURE 12. Efficiency diagram of dual-mode amplifier with switch.

put matching network alignment in Mode 2's band. Incorporating a PIN switch can enhance impedance matching during mode transitions. The revised dual-mode DPA design (Figure 12) demonstrates significant efficiency improvements in Mode 2, achieving over 65% drain efficiency across the entire band — a marked advancement in amplifier performance.

Figure 13 displays the enhanced mode-reconfigurable amplifier's simulation results for gain and drain efficiency. As shown in Figure 13, the drain efficiency in the 6 dB back-off zone peaks at 52% and stays above 40% across the whole frequency range. Throughout the whole frequency range, the drain efficiency rises above 60% to a maximum of 73%. Over the whole frequency range, the gain stays over 9 dB.

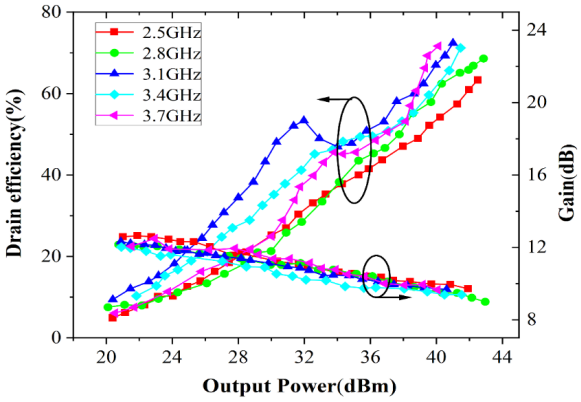

FIGURE 13. Simulated drain efficiencies and gains of the DPA.

4. IMPLEMENTATION AND MEASUREMENT

The design makes use of the CG2H40010F device, which allows enhanced frequency operation, to highlight the ultra-wideband capabilities of the suggested architecture, especially for 5G New Radio (NR) applications. A picture of the manufactured dual-mode power amplifier (DPA) is shown in Figure 14. Both continuous-wave (CW) and modulated signal measurements were used for performance validation. While Mode 2 functioned in the 2.8–3.4 GHz band, Mode 1 was tested in the 2.5–2.9 GHz and 3.3–3.7 GHz bands. T1's quiescent current was kept constant at 68 mA during testing. The gate bias voltages for T1 and T2 were set to −3.2 V and −6.0 V, respectively, in Mode 1. For Mode 2, these bias conditions were reversed, switching the roles of the transistors. A vector signal generator produced the CW and modulated test signals, with output power levels recorded via a spectrum analyzer. To ensure adequate input power for the DPA, a wideband linear driver amplifier was employed to boost the test signals prior to measurement.

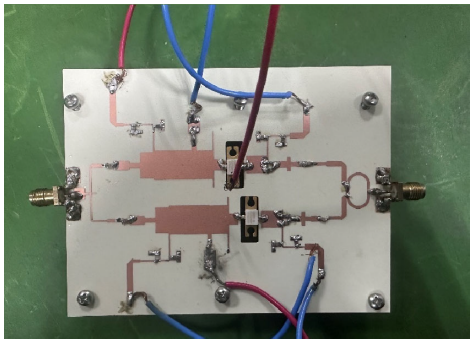

FIGURE 14. Physical photographs of the power waiver produced.

To confirm the Doherty operation of the manufactured DPA, a single-tone CW signal was used for initial testing. Saturated and back-off performance were examined using 0.2 GHz frequency increments over 2.5–3.7 GHz to demonstrate its broadband features. The measured back-off efficiency, drain efficiency, and gain vs frequency for Mode 1 are displayed in Figure 15. Figure 16 displays the comparable frequency-dependent results for Mode 2. The DPA achieves a gain of 9.4–11.3 dB, a maximum output power of 39.4–41.3 dBm, a saturated drain efficiency of 62.2%–71.3%, and a 6-dB output back-off (OBO) drain efficiency of 44.6%–53.7% when operating in Mode 1 over 2.5–2.9 GHz and 3.3–3.7 GHz. With a maximum output power of 40.1–41.4 dBm, a small-signal gain of 10.1–10.4 dB, a saturated drain efficiency of 60.2%–72.0%, and a 6-dB OBO drain efficiency of 45.3%–51.2%, the DPA operates in Mode 2, which spans 2.8–3.4 GHz. Figure 17 shows the power-added efficiency of the Doherty power amplifier across the entire frequency band. When operating at 2.5–3.7 GHz, the DPA achieves a power-added efficiency of 58.3%–69.5%. Figure 18 shows the measured relationship between the phase

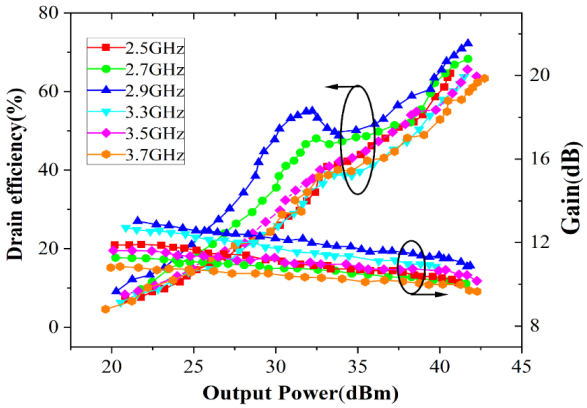

FIGURE 15. Measured drain efficiency and gain of manufactured DPA with output power at different frequencies of Mode 1.

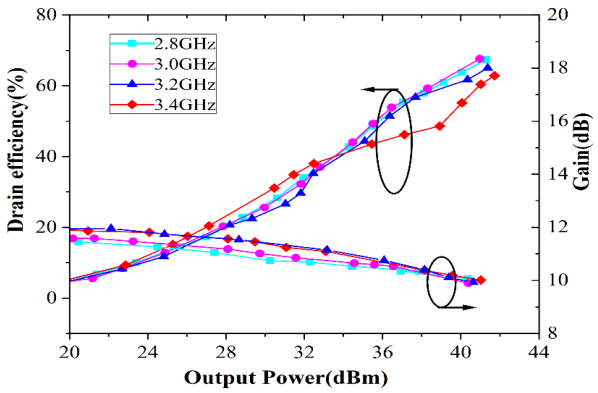

FIGURE 16. Measured drain efficiency and gain of manufactured DPA with output power at different frequencies of Mode 2.

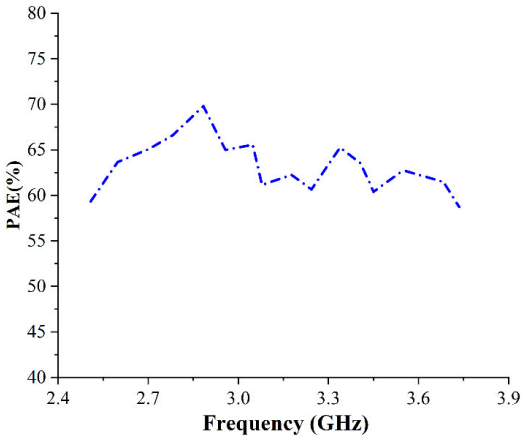

FIGURE 17. Measured power-added efficiency of manufacturing DPA at different frequencies.

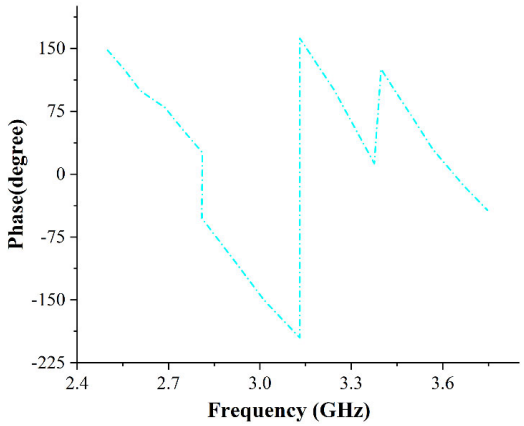

FIGURE 18. Measured relationship between the phase and frequency of the DPA.

and frequency of DPA. It can be seen that the phase undergoes abrupt changes at 2.8 GHz and 3.4 GHz, due to mode switching at these two frequencies.

To assess linearity under modulated signals, third-order intermodulation distortion (IMD3) was evaluated using a two-tone signal with 5 MHz spacing. Figure 19 shows the IMD3 versus output power. Across most of the target band, IMD3 ranges between -20 dBc and -35 dBc, indicating suboptimal linearity. This is attributed to the carrier amplifier operating in saturation at high power levels and the peak amplifier's Class-C bias, which inherently degrades linearity. Consequently, digital predistortion techniques are typically required in practical applications to enhance linearity. Notably, an anomalous IMD3 dip is observed between the back-off point (37.5 dBm) and saturation, explained by the "Sweet Spots" theory [25]. This phenomenon arises from the counteracting phase relationship between the large-signal intermodulation distortion (from the saturated Class-AB carrier amplifier) and the small-signal distortion (from the Class-C peak amplifier), creating a localized region of improved linearity.

Table 1 shows the performance comparison between the designed Doherty power amplifier and some published works. It can be observed that the Doherty power amplifier employing reciprocal gate biasing effectively broadens the amplifier bandwidth while maintaining key performance metrics such as efficiency, back-off efficiency, output power, and gain. Compared with other power amplifiers, the proposed design features mode-switching capability for bandwidth extension, making it more practical for real-world applications.

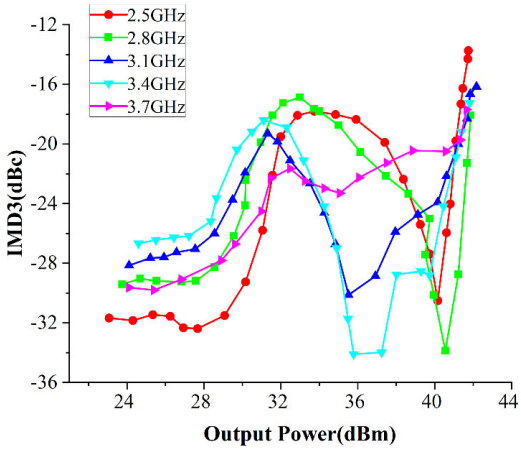

FIGURE 19. Measured IMD3 of DPA manufactured under different output power levels at various frequencies.

TABLE 1. Comparison with other referenced power amplifiers.

Reference	Bandwidth	Efficiency (%)	6 dB Efficiency (%)	Output power (dBm)	Gain (dB)
[7]	1.7–2.6 GHz	57–66	47–57	44.6–46.3	10.2–11.6
[10]	1.7–2.6 GHz	57–71	50–55	44–44.5	13.2–15.7
[24]	3.0–3.6 GHz	55–66	38–56	43–44	8–11
[26]	3.4/4.9 GHz	70.7/70.4	38/42	44/43.2	8/10
This work	2.5–3.7 GHz	60.2–70.2	43.5–53.7	39.4–41.3	9.4–11.3

5. CONCLUSION

This study presents an innovative Doherty power amplifier (DPA) architecture employing reciprocal gate biasing to enable seamless mode-switching across multiple frequency bands, effectively addressing bandwidth limitations in conventional designs. The proposed configuration achieves 43.5%–53.7% 6-dB back-off efficiency over an extended operational bandwidth of 2.5–3.7 GHz while maintaining stable Doherty operational characteristics. This amplifier achieves frequency-agile matching optimization through strategic integration of PIN switches, ensuring impedance adaptability across broadband performance. Simultaneously, it demonstrates multi-standard compatibility encompassing critical 5G NR low-frequency spectrum bands, thereby aligning with the deployment requirements of global telecom operators.

Experimental validation demonstrates the design's potential as a foundational solution for 5G infrastructure, particularly in supporting carrier-aggregated broadband services and dynamic load-modulation scenarios. This work establishes a framework for future high-efficiency PA developments targeting next-generation wireless systems.

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