(Received 3 March 2025, Accepted 11 April 2025, Scheduled 24 April 2025)

Minimum-Current-Stress Strategy for Modular Multilevel Type DC-DC Converter Based on Long Short-Term Memory Optimization

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ABSTRACT: Current stress has a significant impact on the operation of power electronic devices, and the reduction of current stress can improve the safety and reliability of the system. First, this paper proposes a novel asymmetric duty cycle modulation strategy for the primary side of a modular multilevel converter type (MMC) dual active bridge converter (DAB) to increase the control freedom of the primary side. Secondly, a novel optimization strategy based on a long short-term memory network (LSTM) classification is proposed in this paper to optimize the current stress. The output power of the system is classified by LSTM, and minimum current stresses at different powers are optimized by a novel meta-heuristic iterative optimization based on generalized quadratic interpolation (GQI). Finally, the feasibility of the scheme is verified by hardware-in-the-loop experiments.

1. INTRODUCTION

Dual active bridge (DAB) is widely used due to its advantages such as current isolation and high efficiency [1, 2]. The optimization objective is converter inductor current stress. The output voltage of a conventional DAB is usually controlled by single phase shift (SPS) control [3–5]. Refs. [15, 16] proposed that after modeling the SPS control of the converter, the system generates excessive current stresses when the voltages are not matched. In [6, 7], the flexibility of the system can be improved by adding one more degree of freedom, i.e., extended phase shift (EPS) control, which significantly reduces the current stress compared to SPS. Triple phase shift (TPS) control is proposed in [8–10], where two different control degrees of freedom are added to the primary and secondary sides, respectively, which further optimizes the current stress of the system. TPS and combining Lagrange multiplier with proportional-integral (PI) controller for current stress optimization was proposed in [17, 19].

The above shows the optimization of inductor current stress in conventional topology. Refs. [11–13] introduced multilevel topologies in DABs to reduce the voltage stress on the switching devices. Modular multilevel converters (MMCs) have been introduced in DAB topologies due to high modularity and high level of availability [14]. As shown in Figure 1, each phase consists of two bridge arms, with each connected in series with N half-bridge submodules (SMs), while increasing the control degrees of freedom. In [31], a novel partial power DAB converter is proposed that combines the best characteristics of MMC-DAB and autotransformer thereof to minimize the current stress at all operating points. In [32], a multilevel DAB converter with stepped wave modulation is proposed, where the system switching tubes operate in soft-switching mode, and can greatly optimize the system current stress. In [33], a modulation strategy with variable duty cycle is proposed, which can effectively optimize the inductor current stress and counteract the degradation of the soft-switching characteristics. The introduction of artificial intelligence methods has brought many options for optimal control. Refs. [18, 20] proposed a particle swarm optimization (PSO)-based current stress minimization scheme, which reduced system losses and improved power conversion efficiency. Ref. [34] proposed a differential evolutionary algorithm based on data fine-tuning to optimize current stress. In [35], the objective function is minimized by PSO, and the data-driven model is developed by using the optimal dataset, which greatly reduces the converter current stress. As mentioned above, the current stress optimization method for multilevel DAB has become increasingly mature, but the current stress optimization method for MMC-DAB has not yet been studied in depth, and most of the AI optimization algorithms in this area focus on PSO algorithm. In this paper, a current stress optimization method based on generalized quadratic interpolation (GQI) is proposed, which has lower complexity and fewer iterations than PSO and is more suitable for MMC-DAB converters.

Section 1 offers an introduction. Section 2 focuses on the symmetric strategies and novel asymmetric duty cycle modulation strategies for MMC-DAB. Section 3 discusses the classification prediction based on LSTM. Section 4 introduces the inductor current stress optimization strategy about GQI optimization. Section 5 shows the results of hardware-in-the-loop experiments.

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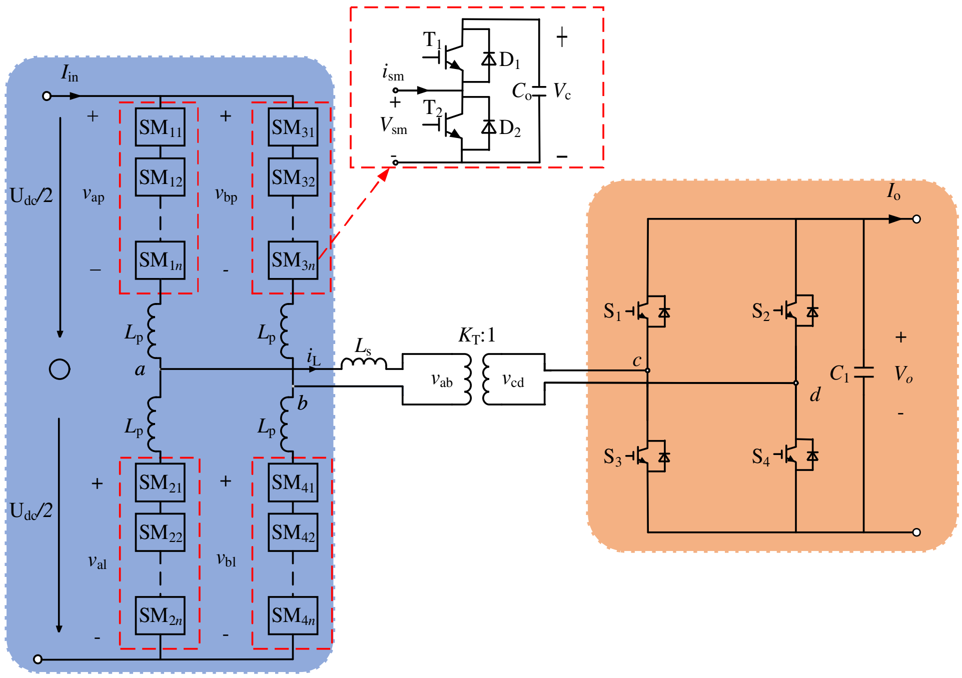

FIGURE 1. MMC-DAB topology.

2. MODULATION STRATEGY FOR MMC-DAB

2.1. Duty Cycle Symmetric Modulation Strategy for MMC-DAB

The constraints can be obtained as follows:

$$\begin{cases} 0 \le D_0, D_1, D_2 \le 0.5 \\ 0 \le d_0, d_1 \le 0.5 \end{cases} \tag{1}$$

where D_0, D_1, and D_2 are the duty cycles of 0, 1/2, and 1 levels of the primary output, respectively, and d_0 and d_1 are the duty cycles of 0 and 1 levels of the secondary output, respectively.

The expression of inductor current and transmitted power can be obtained as follows:

$$\begin{cases} v_{ab} = B_n \sin n\omega t \\ v_{cd} = b_n \sin n\omega \left(t - d_f T_{hs}\right) \end{cases} \tag{2}$$

The inductor current and transmitted power expressions can be deduced as follows:

$$\begin{cases} i\left(t\right) = \sum\limits_{n=1,3,5\cdots}^{\infty} \frac{\sqrt{A^2+B^2}\sin[n\omega t + (\arctan B/A)]}{n\omega L_S} \\ P = \sum\limits_{n=1,3,5\cdots}^{\infty} \frac{K_T b_n B_n}{2n\omega L_S} \sin(n d_f \pi) \end{cases} \tag{3}$$

ω, L_S, d_f, K_T, and T_{hs} represent the angular frequency, transmission inductance, shift ratio between the primary and secondary edges, transformer ratio, and half a switching cycle, respectively.

$$\begin{cases} A = 4b_n \sin n\pi d_f \\ B = 4b_n \cos n\pi d_f - B_n \\ B_n = \frac{2U_{dc}}{n\pi}[\cos n\pi D_0 + \cos n\pi (D_0 + D_1)] \\ b_n = \frac{4V_O}{n\pi} \cos n\pi d_0 \end{cases} \tag{4}$$

2.2. Asymmetric Duty Cycle Modulation Strategy for MMC-DAB

The 0, 1/2, and 1 levels will each appear twice in half of a cycle, which is different from the modulation of symmetrical duty.

$$\begin{cases} D_0 + D_1 + D_2 = 0.5 \\ D_{0r} + D_{1r} + D_{2r} = 0.5 \\ D_0 \ne D_{0r}, D_1 \ne D_{1r}, D_2 \ne D_{2r} \end{cases} \tag{5}$$

Among them, D_0, D_1, and D_2 are the duty ratios of the first 0, 1/2, and 1 levels in the half cycle of the MMC side, respectively. D_{0r}, D_{1r}, and D_{2r} are the duty ratios of the last 0, 1/2, and 1 levels in the half cycle, respectively. High-frequency transformer primary and secondary voltages, inductor current, and transmitted power are the same as those in Eqs. (4) and (5), but the coefficients B and B_n are not the same as those in Eqs. (4) and (5) because they need to be according to the asymmetric modulation strategy. At this time there are:

$$\begin{cases} B = 4b_n \cos n\pi d_f - B_n \\ B_n = \frac{V_{dc}}{n\pi}[\cos n\pi D_0 + \cos n\pi (D_0 + D_1) \\ + \cos n\pi D_{0r} + \cos n\pi (D_{0r} + D_{1r})] \end{cases} \tag{6}$$

3. LSTM-BASED CLASSIFICATION PREDICTION

3.1. Working Principle of LSTM

LSTM is a variant of recurrent neural network (RNN) [21], which reduces overfitting by introducing gating mechanisms, and [24] lists the structure of LSTM and the expressions of each gating mechanism.

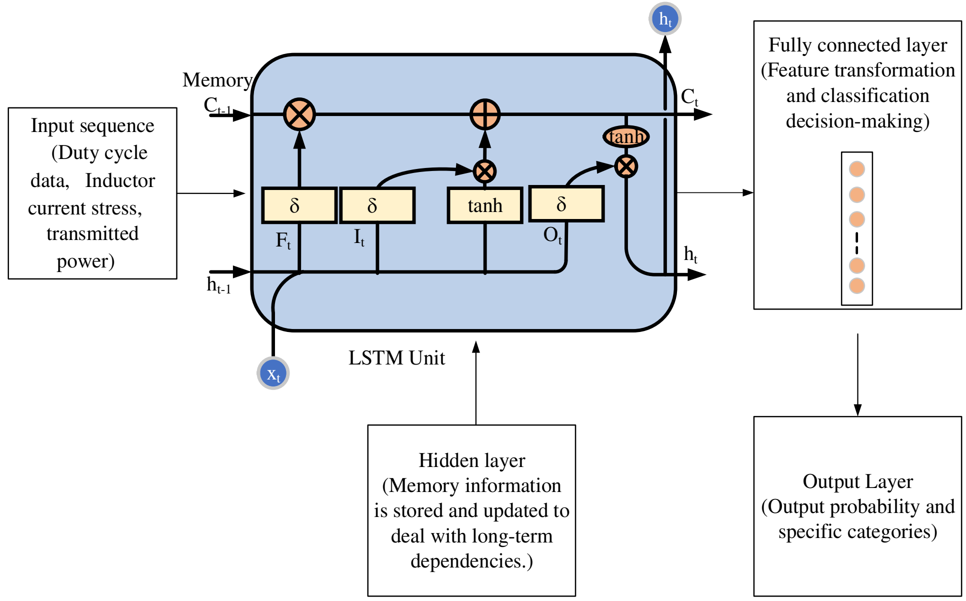

FIGURE 2. LSTM classification prediction steps.

TABLE 1. LSTM classification prediction pesudocode.

Pseudo-code of LSTM Classification forecasts
Setting up the dataset
model = Sequential()
model.add(LSTM(units = lstm_units, input_shape = (seq_length, input_dim)))
Add Dropout layer (to prevent overfitting)
model.add(Dropout(rate = 0.2))
model.add(Dense(units = num_classes, activation = 'softmax'))
history = model.fit(X_train, y_train, epochs = epochs, batch_size = batch_size, validation_split = 0.2)
loss, accuracy = model.evaluate(X_test, y_test)
print(f"Test Accuracy: {accuracy}")
predictions = model.predict(X_test)

3.2. Power Classification Prediction of Current Stress

The training steps of LSTM are shown in Figure 2. The input sequence is preprocessed, such as data normalization and data tile. In the next step of building the LSTM model, the shape of the input layer depends on the feature dimension and sequence length of the input sequence data. The LSTM layer is the core part of the model, which is responsible for extracting the time dependence in the sequence [22]. The hidden layer controls the flow of information, stores and updates information through a series of 'gates' [23]. The long-term dependencies in the sequence are captured by the cell state. The structure of the unit state enables the information to be transmitted more stably. The LSTM classification prediction pseudo-code is shown in Table 1.

δ is the activation function: $\delta = 1/(1 + e^{-x})$.

Figure 3 shows the effect of data classification prediction, and categories 1–4 are four power segments from low to high. The accuracy is as high as 97.1331 %. LSTM has a high accuracy rate for the classification of current stress duty cycle matrix about load power.

4. CURRENT STRESS OPTIMIZATION BASED ON QUADRATIC INTERPOLATION OPTIMIZATION

4.1. Traditional Quadratic Interpolation

Quadratic interpolation is a commonly used curve fitting technique that is commonly used to find the minimum point in a given deterministic initial interval for a unary function [25, 29]. Function $f(x)$ is approximated by a quadratic interpolation polynomial denoted as $L(x)$, $L(x)$, $f(x)$, where α and β are undetermined coefficients [30]. Let $f(x)$ have three points i, j, and k, and the value of $f(x)$ is equal to the value of the interpolation point $L(x)$, which is expressed as:

$$L(x) = \alpha x^2 + \beta x + C = f(x) \tag{7}$$

The α and β values represented by i, j, k and their corresponding $f(i)$, $f(j)$, and $f(k)$ can be obtained according to the above

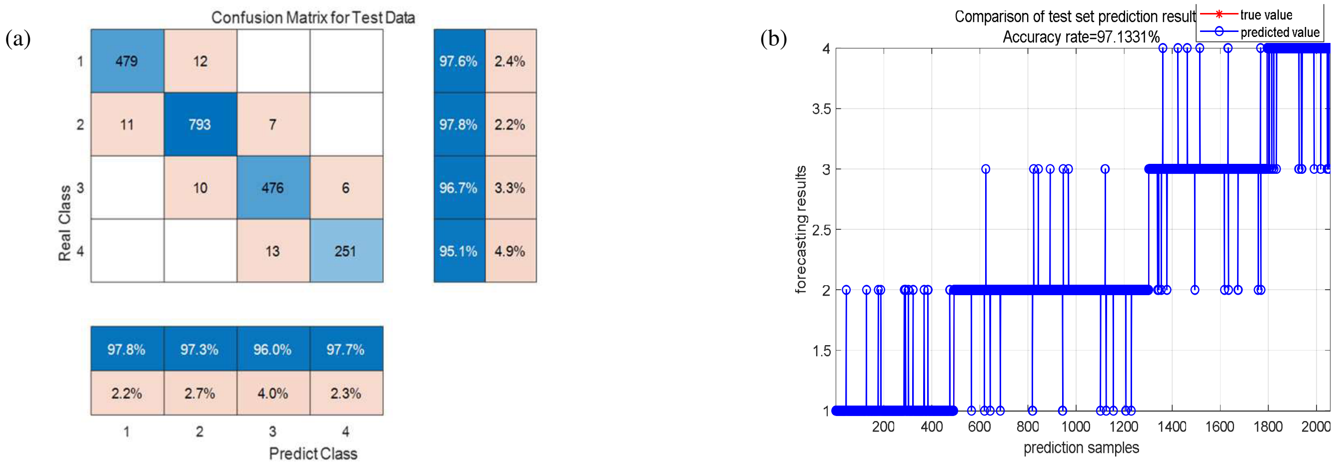

FIGURE 3. LSTM classification prediction results. (a) Test set classification results. (b) Test set classification prediction accuracy.

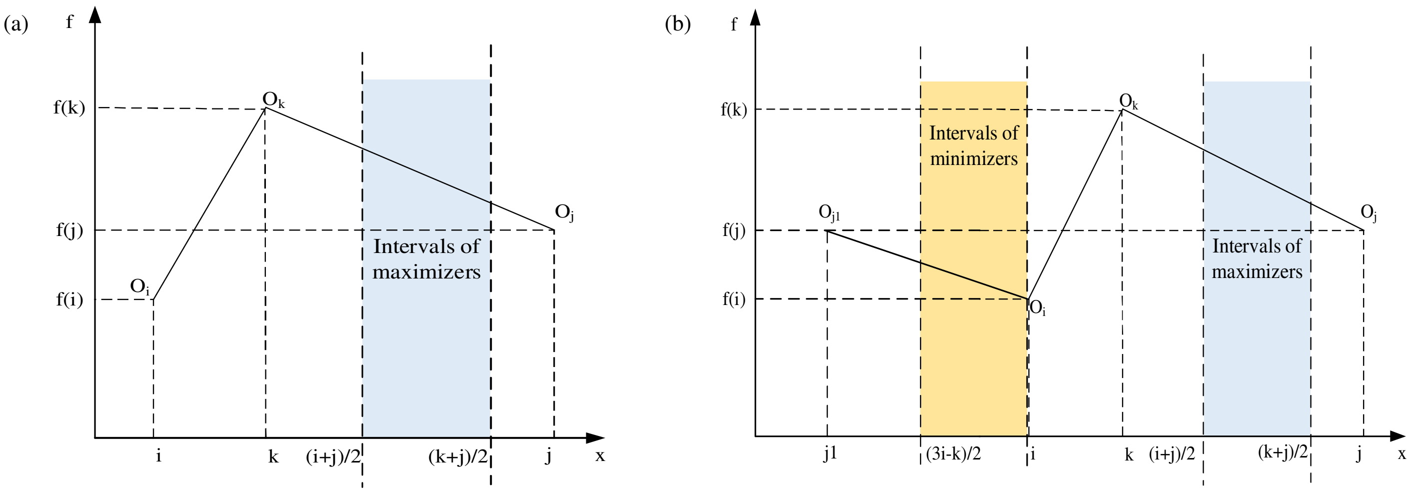

FIGURE 4. Generalized quadratic interpolation strategy. (a) Maximum interval of quadratic interpolation. (b) The minimum intervals of GQI.

formula. Then $L(x)$ can be expressed as:

$$L(x) = \frac{(x-j)(x-k)}{(i-j)(i-k)}f(i) + \frac{(x-i)(x-k)}{(j-i)(j-k)}f(j) + \frac{(x-j)(x-i)}{(k-j)(k-j)}f(k) \tag{8}$$

4.2. A Novel Quadratic Interpolation Optimization

When the minimum value of a one-dimensional dataset is optimized, such as inductor current stress, there will be times when the search area is not selected properly, resulting in only the maximum value in the optimization interval but not the minimum value [27, 28]. For example, for Figure 4(a), where there is only one maximum interval, and the optimal solution of $f(x)$ may be the left of i. When the GQI algorithm [26] is introduced as shown in Figure 4(b), the minimum intervals are supplied by O_{j1}, O_i, and O_k. The maximum and minimum intervals in Figures 4(a) and 4(b) are calculated as shown in Eqs. (15), (16) and Eq. (21) in [26].

After passing the exploration and development phases, the position of the ith instance was updated as follows. x, v, and t denote the position, iteration speed, and number of iteration rounds, respectively.

$$x_i(t+1) = \begin{cases} x_i(t) & fit(x_i(t)) \le fit(v_i(t+1)) \\ v_i(t+1) & fit(x_i(t)) > fit(v_i(t+1)) \end{cases} \tag{9}$$

The specific flowchart of quadratic interpolation optimization is as Figure 5.

5. EXPERIMENTAL RESULT AND ANALYSIS

5.1. Hardware-in-the-Loop Experiment Parameters

This hardware-in-the-loop platform uses the Rapid Control Prototype (RCP) to run the overall control section and the Dspace1202 to run the MMC-DAB hardware topology. The sampled physical quantities are communicated to the RCP control section via I/O ports, and the PWM pulse waves generated by the control section are communicated to the Dspace1202 via Modbus TCP/IP. The overall structure of the platform is shown in Figure 6. The experimental parameters are shown in Table 2.

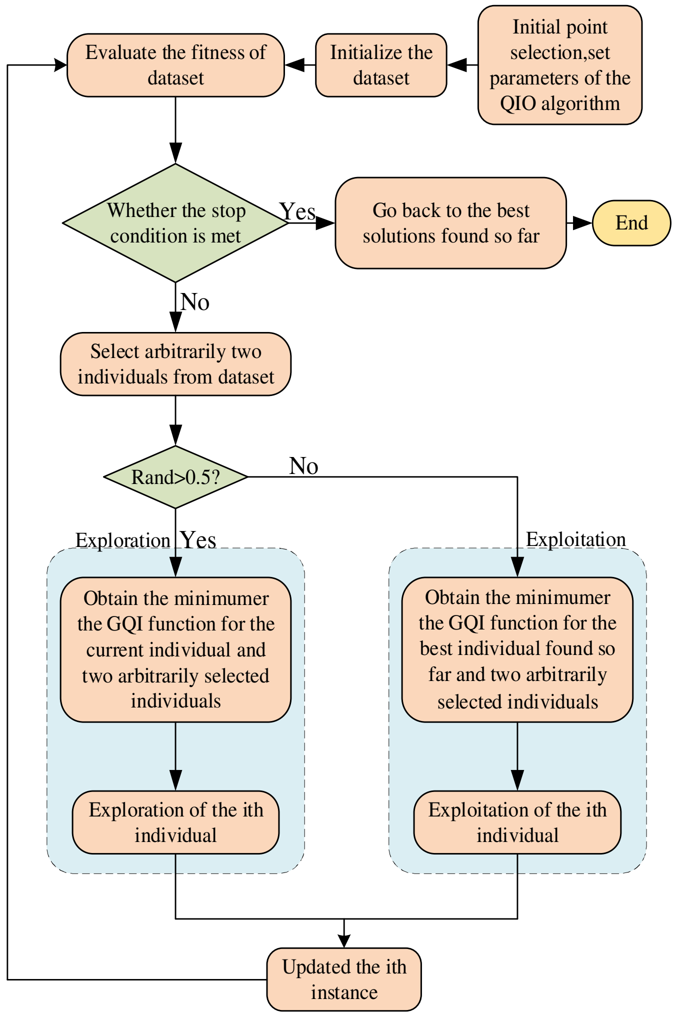

FIGURE 5. QIO specific steps.

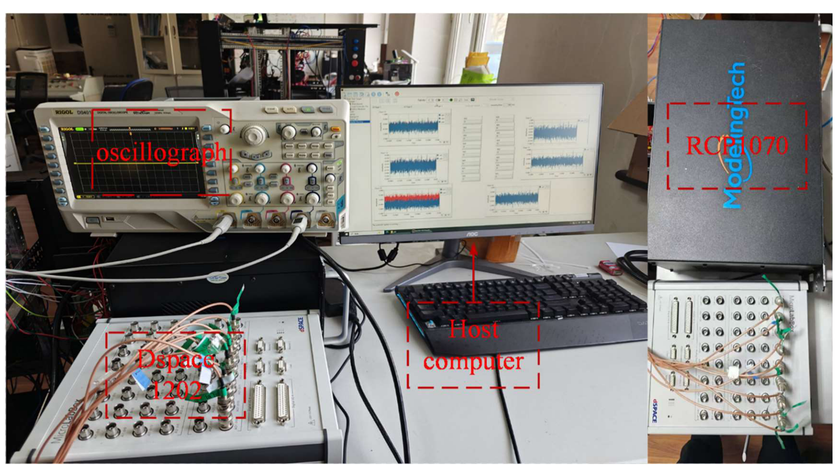

FIGURE 6. Hardware-in-the-loop experimental platform.

5.2. Optimization of Symmetric Modulation

Light load (200 W), medium load (600 W), and heavy load (800 W) are shown in Figures 7–9. (a) The whole process of optimization, (b) the expansion diagram (as below). Online optimizations (taking sudden load reduction as an example) from medium to light load (600 W to 200 W), heavy to medium load (800 W to 600 W) respectively are shown in Figures 10 and 11.

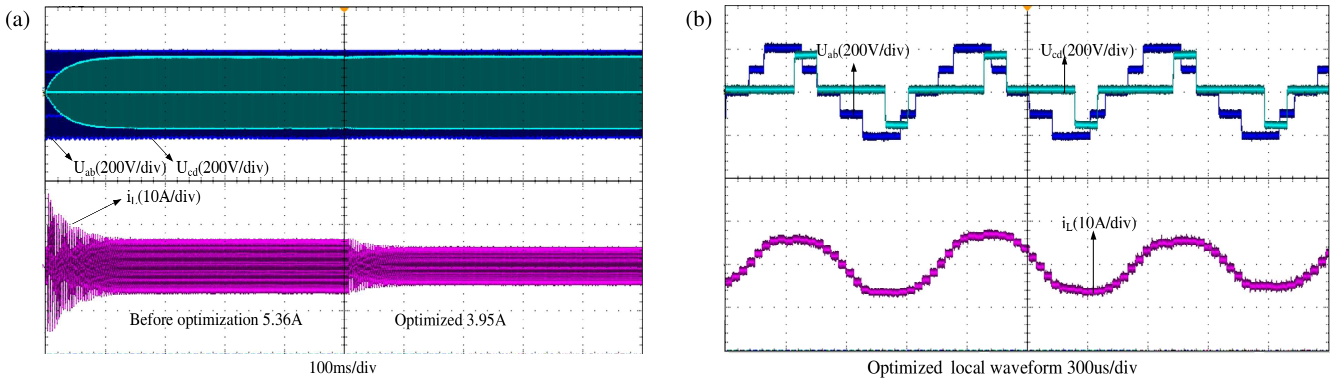

FIGURE 7. Symmetrical light load offline optimization. (a) Optimize the whole process diagram. (b) Optimized local waveform.

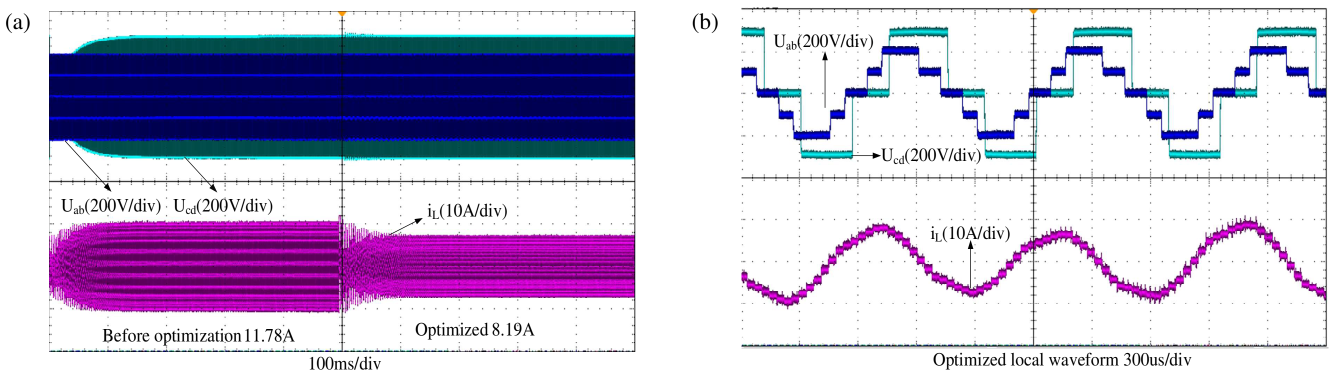

FIGURE 8. Symmetrical medium load offline optimization. (a) Optimize the whole process diagram. (b) Optimized local waveform.

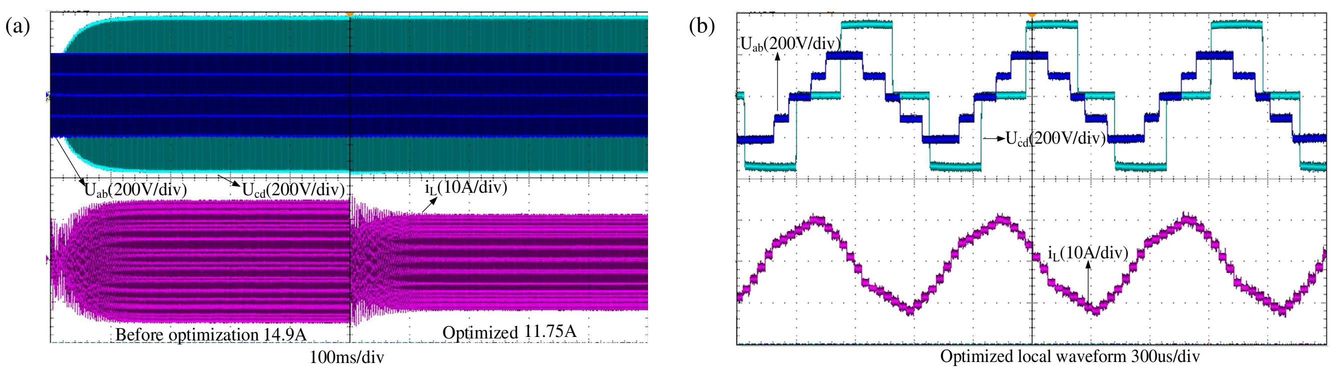

FIGURE 9. Offline optimization of symmetrical heavy load. (a) Optimize the whole process diagram. (b) Optimized local waveform.

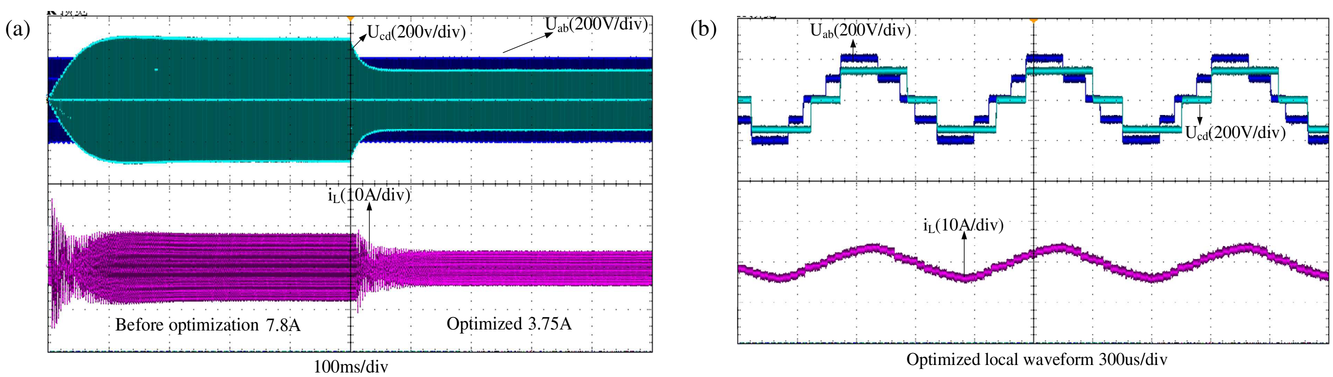

FIGURE 10. Symmetrical online optimization of medium to light load. (a) Optimize the whole process diagram. (b) Optimized local waveform.

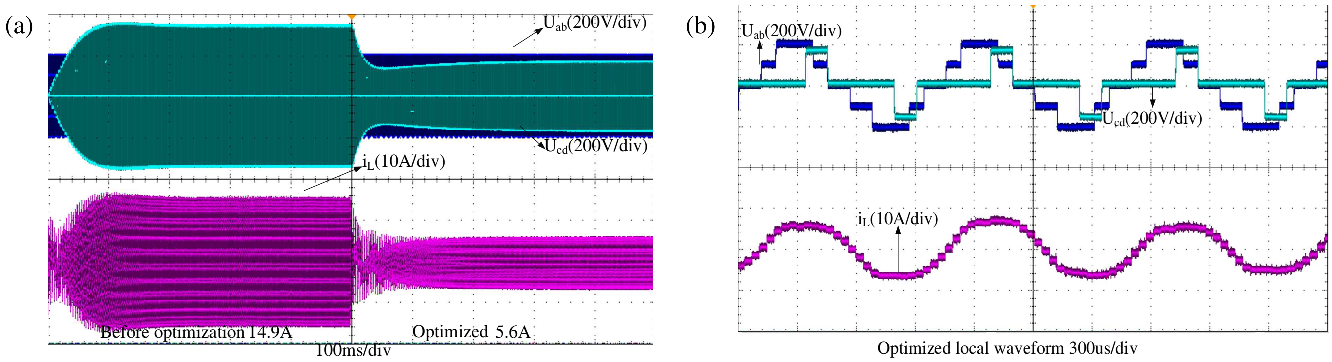

FIGURE 11. Symmetrical online optimization of heavy load to medium load. (a) Optimize the whole process diagram. (b) Optimized local waveform

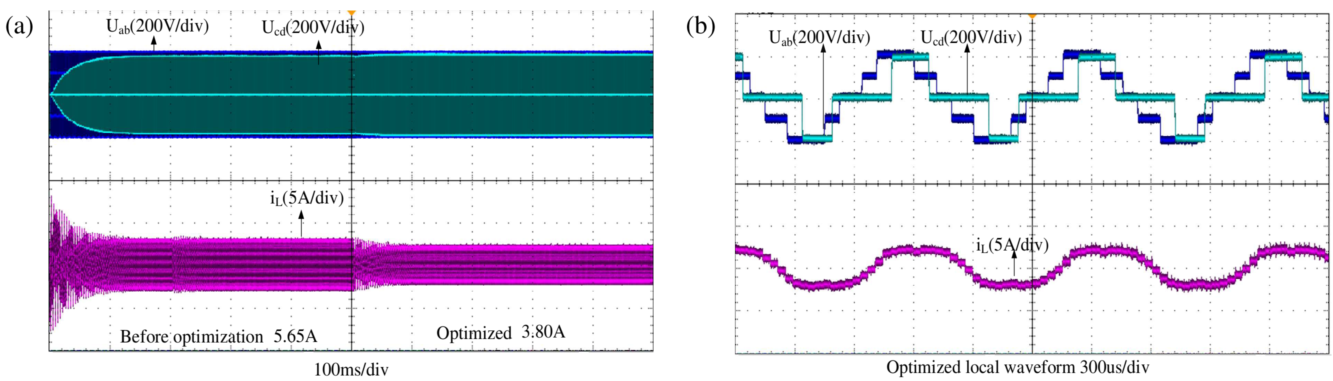

FIGURE 12. Asymmetrical offline optimization of light load. (a) Optimize the whole process diagram. (b) Optimized local waveform.

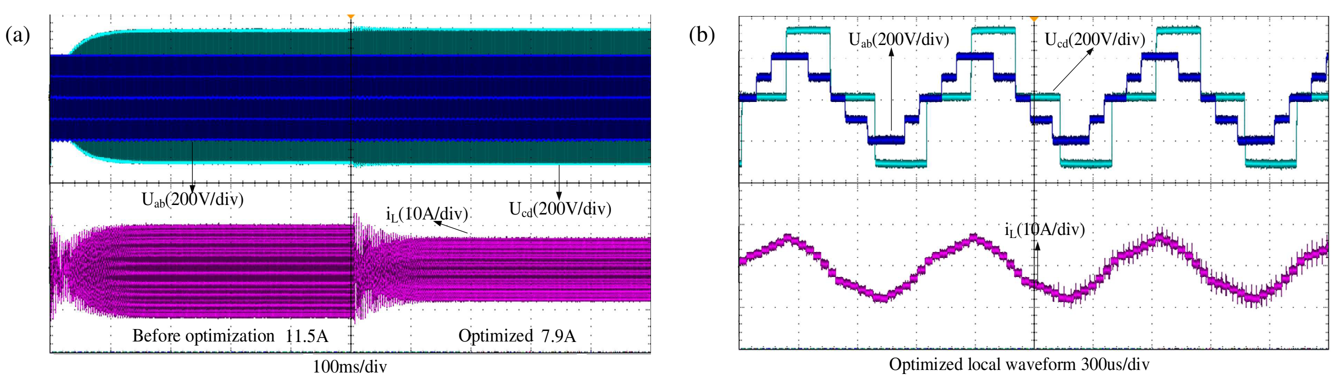

FIGURE 13. Asymmetrical offline optimization of medium load. (a) Optimize the whole process diagram. (b) Optimized local waveform.

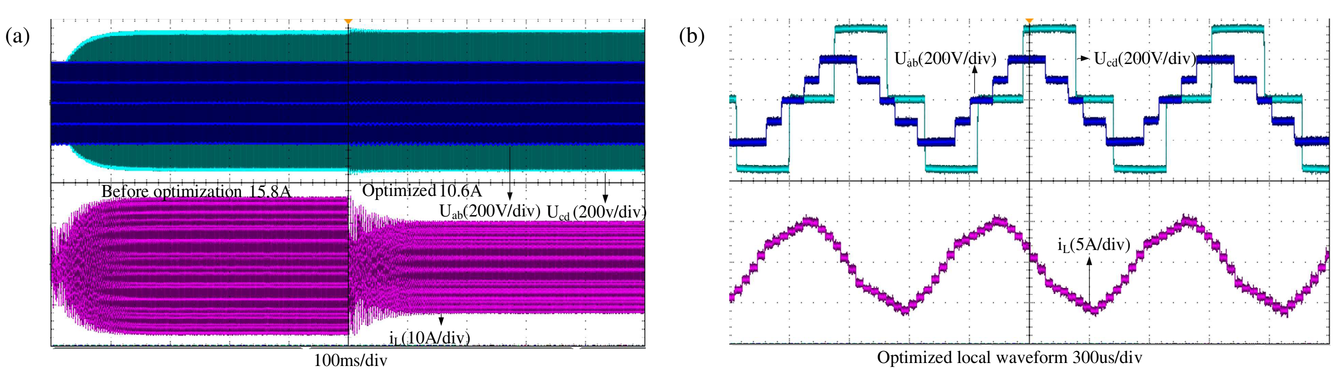

FIGURE 14. Asymmetrical offline optimization of heavy load. (a) Optimize the whole process diagram. (b) Optimized local waveform.

TABLE 2. Five-level MMC-DAB converter parameters.

Parameter	Value	Parameter	Value
Number of HBSMs N	4	Output capacitance C_1/mF	1.8
DC-link U_{dc}/V	200	HBSM capacitance C_O/mF	1
Inductance of arm L_p/mH	1	Transmission inductance L_s/mH	3.5
Fundamental frequency f/kHZ	1	Subside filtering capacitor C_F/μF	150
Output resistance R_0/Ω	10	DC-side split capacitor C_{DC}/mF	1

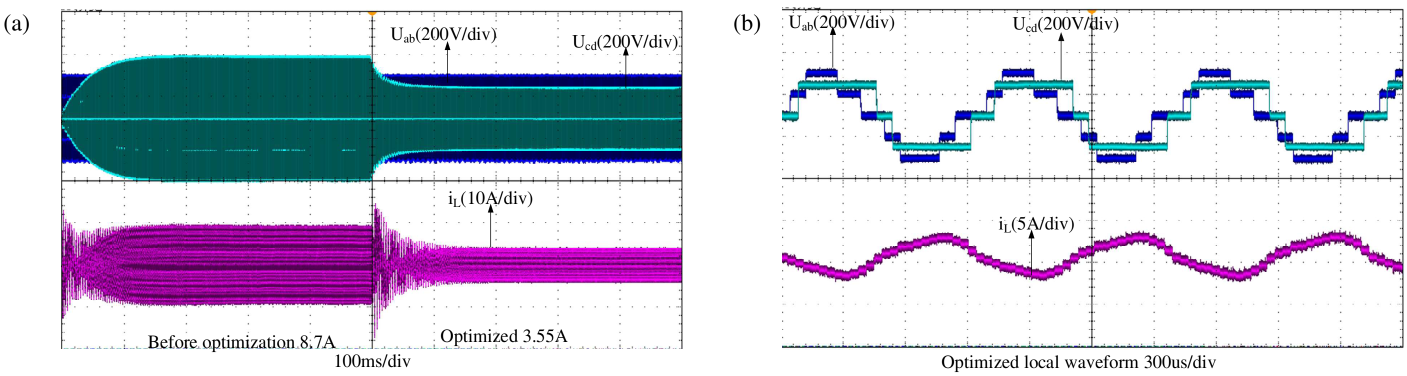

FIGURE 15. Asymmetrical online optimization of medium to light load. (a) Optimize the whole process diagram. (b) Optimized local waveform.

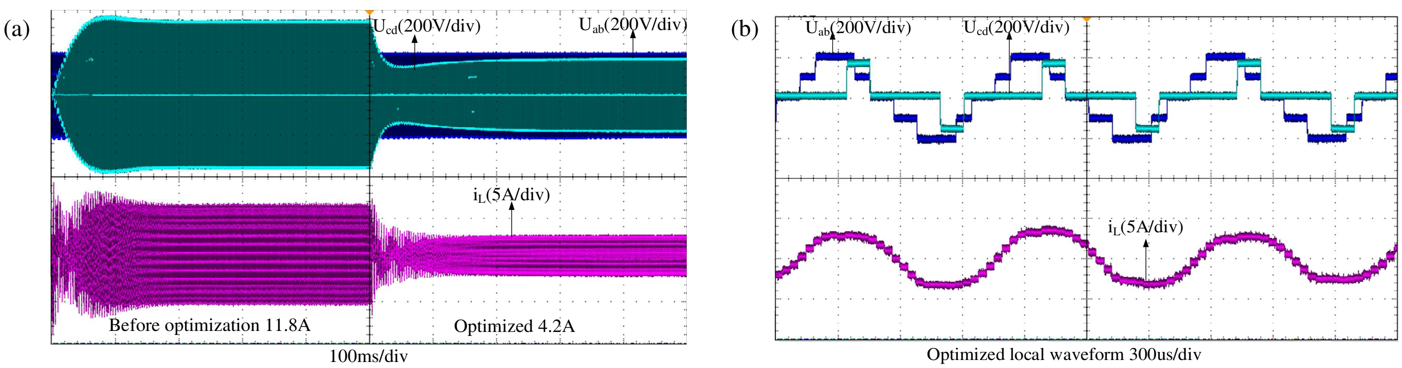

FIGURE 16. Asymmetrical online optimization of heavy to medium load. (a) Optimize the whole process diagram. (b) Optimized local waveform.

TABLE 3. Offline optimization of converter performance (Comparison with TPS.

Modulations	Current Optimized Ratio	Voltage ripple ratio	Transfer power ratio
Symmetric 5-Level	L:15.64% M:9.83% H:6.55%	L:−14.44% M:−13.81%H:−9.97%	L:+1.31%M:+1.36%H:+1.25%
Asymmetric 5-Level	L:17.35%M:11.23%H:6.98%	L:−16.53% M:−14.79%H:−11.68%	L:+1.54% M:+2.13%H:1.64%

TABLE 4. Online optimization of converter performance (Comparison with TPS, load shedding).

Modulations	Current Optimized Ratio	Voltage ripple ratio	Transfer power ratio
Symmetric 5-Level	L:35.34% M:18.84%	L:−15.24% M:−13.81%	L: +2.61% M:+2.82%
Asymmetric 5-Level	L:38.79% M:39.13%	L:−19.33% M:−14.94%	L:+2.34% M:+2.93%

5.3. Optimization of Asymmetric Modulation

The offline optimization results of the asymmetric modulation under light load (200 W), medium load (600 W), and heavy load (800 W) respectively are shown in Figures 12–14.

The online optimizations (taking sudden load reduction as an example) from medium to light load (600 W to 200 W) and heavy to medium load (800 W to 600 W) respectively are shown in Figures 15 and 16.

6. CONCLUSION

In this paper, we propose a load power classification prediction based on LSTM and an inductor current stress optimization algorithm based on secondary interpolation optimization. Experimental results show that asymmetric optimization is better than symmetric optimization, and online optimization results are better than offline optimization. As shown in Tables 3 and 4. L is for light load, M for medium load, and H for heavy load.

As shown in the tables above, in terms of current stress and voltage ripple optimization, asymmetric optimization is better than symmetric optimization, but from the perspective of the transmission power ratio, the two effects are comparable.

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