

Low-Pass and Bandpass Dual-Band Filter Based on Surface Mounted Technology Using Lumped Parameter Components

Jie Xu^{1,*}, Yongle Wu², Qinghua Yang¹, and Weimin Wang²

¹*School of Electronic Engineering, Beijing University of Posts and Telecommunications, Beijing, China*

²*School of Integrated Circuits, Beijing University of Posts and Telecommunications, Beijing, China*

ABSTRACT: This paper proposes a lumped parameter microwave dual frequency filter implemented using surface mount technology (SMT), which has low-pass and band-pass characteristics. We implement a dual-band response by integrating a matching network and harnessing the inherent parasitic inductance of SMT capacitors. This strategy generates transmission zeros (TZs) in the high-frequency band, significantly enhancing frequency selectivity. The performance of the filter was verified through odd-even mode analysis and validated through experimental measurement. The experiment measured that the low pass cut-off frequency of the filter is 360 MHz, and the second channel exhibits good band-pass characteristics at 800 MHz, with an insertion loss of -2.191 dB.

1. INTRODUCTION

With the rapid development of mobile communication technology, there are higher demands for the service quality of various types of data, as well as higher requirements for the volume and weight of various electronic products [1–3]. Multi-band filters can separate or merge signals from multiple frequency bands within a single device, reducing the number of independent filters in the system and simplifying the radio frequency (RF) front-end architecture [4–8]. In the past few decades, multi-band filters have attracted increasing attention from researchers [9–11]. In [12], a dual-band bandpass filter (DBBPF) based on a Y-shaped structure was proposed, which has seven transmission zeros and two passbands. Ref. [13] proposed a low temperature cofired ceramic (LTCC) on-chip dual bandpass filter based on lumped elements, which includes four transmission poles (TPs) and three transmission zeros. Ref. [14] proposed a dual/triple band filter based on GaAs IPD (Gallium Arsenide Integrated Passive Device) technology, which achieved a single channel dual/triple band filter by introducing a single band impedance matching network.

Compared with distributed circuits, lumped-element microwave filters offer irreplaceable advantages in low-frequency applications (< 2 GHz) with stringent size and integration requirements, particularly ultra-compact footprint, design flexibility, and manufacturability. Surface mount technology (SMT), as a mature electronic assembly process, has demonstrated unique advantages in the implementation of microwave filters [15]. Compared to traditional waveguide or microstrip line filters, SMT technology has the following significant characteristics: (1) Using standardized components with good consistency, suitable for mass production; (2) Flexible design, easy to implement complex circuit topologies; (3) Low cost and significant economic benefits [16]. These advantages have

enabled SMT to be widely used in civilian communication equipment, military electronic systems, and aerospace fields [17].

This paper is based on SMT technology and designs a lumped parameter microwave dual-band filter. Building on a low-pass filter (LPF) core, we introduce a matching network to create a second passband. Crucially, we repurpose the inherent parasitic inductance of SMT components to generate a high-frequency TZ, thereby sharpening frequency selectivity. Then, the relationship among component parameters, reflection coefficients, and TPs is analyzed, and the design steps of the filter were summarized. Finally, the correctness of the design is verified through experiments.

2. PROPOSED DUAL-BANDPASS FILTER (DBPF) AND WORKING MECHANISM

2.1. Theory of the Proposed Dual-Band Filter

Figure 1(a) shows the circuit structure of the proposed dual-band filter. The dual-band filter architecture comprises two functional sections: a central low-pass filter component flanked by bilateral matching networks. The frequency responses of the low-pass filter and dual-band filter are shown in Fig. 1(b). Fig. 1(b) compares the simulated frequency response of the proposed DBF with that of a reference LPF. The reference LPF is designed independently with component values ($C_2 = 19.4$ pF, $L_2 = 17.8$ nH) chosen to exhibit a relatively poor cutoff characteristic. This characteristic is intentionally leveraged as a starting point to demonstrate the concept: by introducing the matching network, a second passband can be effectively generated. It is important to note that the component values within the low-pass section of the final DBF ($C_2 = 3.7$ pF, $L_2 = 17.2$ nH) differ from those of the stand-alone reference LPF. This circuit adjustment is required to attain the target low-pass cutoff

* Corresponding author: Jie Xu (xujie2599@163.com).

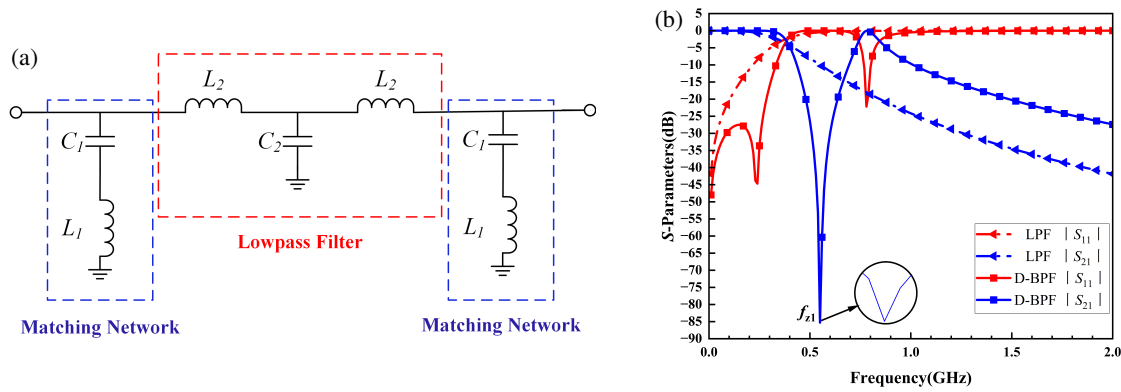


FIGURE 1. (a) The schematic of the proposed dual-band filter and (b) the frequency response of DBF ($C_1 = 6.3$ pF, $C_2 = 3.7$ pF, $L_1 = 13.2$ nH, $L_2 = 17.2$ nH,) and LPF ($C_2 = 19.4$ pF, $L_2 = 17.8$ nH).

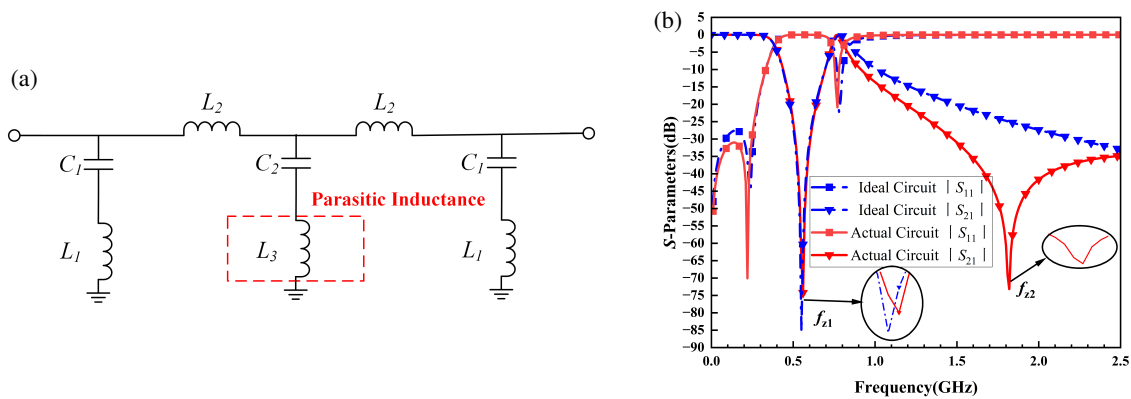


FIGURE 2. (a) The schematic of the actual circuit and (b) the frequency response of actual circuit ($L_3 = 2.4$ nH) and ideal circuit.

frequency and ensure functional integration with the bandpass channel in the DBF architecture, accounting for the matching network's impedance transformation characteristics.

It should be noted that generating the second passband compromises high-frequency stopband suppression to a measurable degree. Surface-mount capacitors exhibit non-ideal characteristics; their practical equivalent circuit comprises an ideal capacitor in series with equivalent series resistance and equivalent series inductance. Furthermore, parasitic coupling effects occur between the capacitor and ground plane during assembly due to soldering imperfections. At high frequencies, the inductance effect gradually increases. Therefore, in the actual circuit shown in Fig. 2(a), it can be seen that parasitic inductance L_3 is generated between capacitor C_2 and ground, forming a series resonator and introducing TZ to enhancement stopband suppression at high frequencies.

From Fig. 2(b), it can be seen that there are two TZs in the actual circuit. Compared to ideal circuits, actual circuits have stronger bandpass selectivity. The deliberate utilization of parasitic inductance enables the generation of TZ at high frequencies, thereby enhancing cutoff characteristics. This demonstrates how inherent process non-idealities can be strategically harnessed to achieve performance advantages.

2.2. Analysis of Frequency Response

Surface mount capacitors are not ideal components; their practical equivalent circuit comprises an ideal capacitor in series with equivalent series resistance and equivalent series inductance. The equivalent circuit stems from the physical structure of the capacitor package and solder pads [18]. The odd even-mode equivalent circuit model of the lumped structure is shown in Fig. 3, where Fig. 3(a) is the even mode equivalent circuit and Fig. 3(b) the odd mode equivalent circuit [19].

The equivalent impedance Z_{ine} of the even-mode circuit in Fig. 3(a) can be calculated as follows:

$$Z_{ine} = \frac{\left(j\omega L_1 + \frac{1}{j\omega C_1}\right) \left(j\omega L_2 + \frac{1}{j\omega(C_2/2)} + j\omega 2L_3\right)}{\left(j\omega L_1 + \frac{1}{j\omega C_1}\right) + \left(j\omega L_2 + \frac{1}{j\omega(C_2/2)} + j\omega 2L_3\right)} \quad (1)$$

The equivalent impedance Z_{ino} of the odd-mode circuit in Fig. 3(b) can be calculated as follows:

$$Z_{ino} = \frac{(j\omega L_1 + 1/j\omega C_1)j\omega L_2}{(j\omega L_1 + 1/j\omega C_1) + j\omega L_2} \quad (2)$$

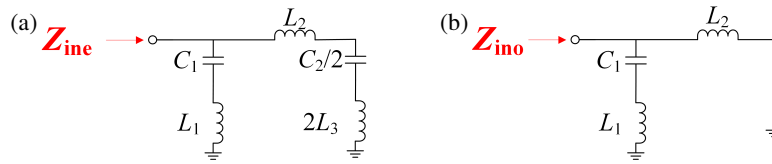


FIGURE 3. Odd-even mode equivalent circuits. (a) The even-mode equivalent circuit. (b) The odd-mode equivalent circuit.

TABLE 1. Final optimized component values of the fabricated dual-band filter.

Component	C_1	C_2	L_1	L_2	L_3 (Parasitic)
Design Value	6.3 pF	3.7 pF	13.2 nH	17.2 nH	2.4 nH
Component Specification/Tolerance	6.3 pF ± 0.1 pF (0603)	3.7 pF ± 0.1 pF (0603)	13 nH $\pm 5\%$ (0603)	17 nH $\pm 5\%$ (0603)	N/A
f_{z1} offset range caused by tolerance	± 9 MHz	N/A	± 26 MHz	N/A	N/A
f_{z2} offset range caused by tolerance	N/A	± 73 MHz	N/A	N/A	N/A
IL at 800 MHz caused by tolerance	± 0.07 dB	± 0.52 dB	± 0.17 dB	± 0.33 dB	N/A

The transmission coefficient S_{21} can be calculated as follows [20]:

$$S_{21} = \frac{(Z_{inc}Z_0 - Z_{ino}Z_0)}{(Z_0 + Z_{inc})(Z_0 + Z_{ino})} \quad (3)$$

The reflection coefficient S_{11} can be calculated as follows:

$$S_{11} = \frac{1}{2} \left(\frac{Z_0 - Z_{inc}}{Z_0 + Z_{inc}} + \frac{Z_0 - Z_{ino}}{Z_0 + Z_{ino}} \right) \quad (4)$$

where Z_0 is the terminal impedance and is set to 50Ω .

2.3. Design of the Proposed DBPF

By setting $S_{21} = 0$ and $S_{11} = 0$ respectively, the TZs and the TPs can be obtained [21]. The useful solutions for TZs can be expressed as follows:

$$f_{z1} = \frac{1}{2\pi\sqrt{L_1C_1}} \quad (5)$$

$$f_{z2} = \frac{1}{2\pi\sqrt{L_3C_2}} \quad (6)$$

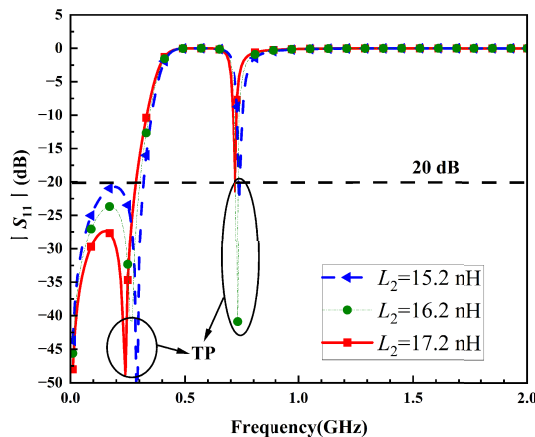


FIGURE 4. The variation of the TPs and return loss with L_2 .

According to (5) and (6), f_{z1} is inversely proportional to the values of L_1 and C_1 , and f_{z2} is inversely proportional to the values of L_3 and C_2 . These two TZs are mutually orthogonal and exhibit negligible interdependence. In contrast, TPs lack deterministic solutions but remain governed by circuit parameter values. Consequently, the independent TZs can be prioritized during synthesis, followed by the tuning of return loss and TPs via L_2 — a parameter decoupled from TZ positioning. Fig. 4 quantifies the parametric relationship between L_2 variation and corresponding TPs/return loss characteristics. Based on the analysis above, the filter design process is as follows:

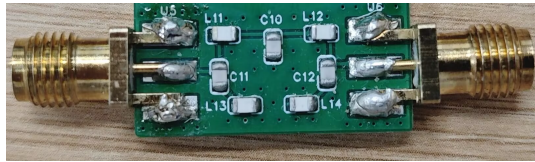
- Specify the desired parameters including the bandpass center frequency and low-pass cut-off frequency.
- Determine the circuit structure of the dual-band filter and set TZs by L_1 , C_1 , and C_2 .
- Adjust TPs and return loss by L_2 .
- Produce boards and optimize them repeatedly through multiple measurements until they satisfy performance demands.

3. SIMULATED AND MEASURED RESULTS

The final optimized component values are listed in Table 1. At the same time, due to systemic tolerances inherent in SMT components, TZs and passband insertion loss are subject to manufacturing variations. Table 1 presents sensitivity analysis of filter performance metrics against typical manufacturing tolerances of these SMT components as well. It is evident that capacitor C_2 exhibits heightened sensitivity to system performance due to parasitic coupling with the ground plane and intrinsic component characteristics. Based on the above design content, verify through SMT technology and use EDA software for circuit design. The involved circuit structure is transformed into a physical layout as shown in Fig. 5, and the used inductors and capacitors are packaged in 0603. In this paper, FR-4 is used as the dielectric substrate for the filter. Its relative dielectric constant is 4.5, the loss tangent 0.004, and substrate

TABLE 2. Comparison with published filters.

Technology/Ref	f_{c1}/f_{c2} (GHz)	FBW (%)	IL ₁ /IL ₂ (dB)	RL ₁ /RL ₂ (dB)	Size (λ_g^2)	Cost Factor	Parasitic Utilization
SIW [3]	5.57/7.84	6.8/4.1	1.8/2	32.4/27.6	0.19	6.1	None
Microstrip [7]	2.5/5.53	3.0/9.5	1.1/0.7	18.6/22.9	0.046	3.5	None
LTCC Lumped [13]	3.32/5.17	25.45/14.2	1.38/1.53	28/23	0.012	4.2	Passive
GaAs IPD [14]	2.26/4.75	24.8/12.4	1.88/2.21	24/23	0.005	8.7	Passive
This Work (SMT Lumped)	0.36/0.8	N/A/12.2	2.47 (LP)/2.19 (BP)	25 (LP)/20 (BP)	0.008	1.0	Active

**FIGURE 5.** Practical photograph.

thickness 1.6 mm. The experimental results were obtained by a vector network analyzer.

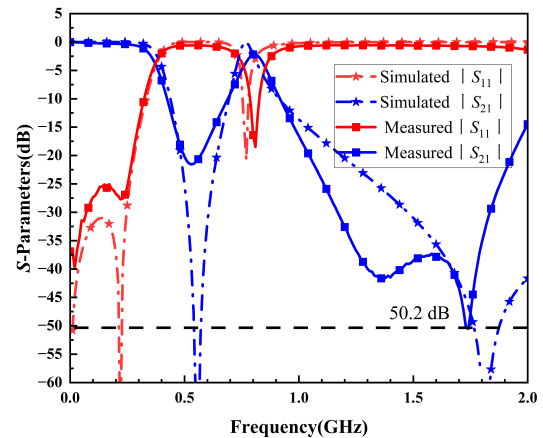
In Fig. 6, the comparison between the measured and simulated results can be seen. The results show that the low-pass cut-off frequency of the dual-band filter is 360 MHz, and the insertion loss of the bandpass center frequency of 800 MHz is -2.191 dB, which verifies the correctness of the design. The first suppression peak was measured at 43.8 dB (1.38 GHz), while the second reached 50.2 dB (1.75 GHz). Across the 1.38–1.75 GHz band, suppression consistently approximated 43 dB, validating the design methodology. However, compared to the simulated insertion loss of -0.373 dB at 800 MHz, measured performance degraded to 2.191 dB due to signal integrity impairment from parasitic effects in solder joints and weld beads.

This loss level represents a deliberate compromise between low-cost SMT implementation and strategic utilization of parasitics for selectivity enhancement. Consequently, transmission loss degradation is an inherent characteristic of this approach.

Mitigation strategies include adopting high-frequency substrates (e.g., Rogers RO4000 series) and layout optimization. When being modeled using microstrip transmission theory, the RO4350B substrate ($\epsilon_r = 3.48$, $\tan \delta = 0.0037$) exhibits significantly lower loss at 800 MHz than FR-4. Substituting FR-4 with RO4350B reduces dielectric loss by approximately 20%. Further reduction in conductor and radiation losses can be achieved through:

- Critical path shortening.
- Pad size minimization.
- Grounding optimization.
- Enhanced transmission line structures.

Conservative electromagnetic simulations estimate that these layout refinements could yield an additional 0.1–0.2 dB insertion loss improvement at 800 MHz. These projections represent best-case scenarios; actual performance gains depend critically on manufacturing process control.

**FIGURE 6.** S-parameters of the simulated and measured results.

Finally, performance comparisons with the reported filters are listed in Table 2 to highlight the benefits of the DBF presented in this brief.

4. CONCLUSIONS

This paper successfully designs and verifies a lumped parameter microwave dual frequency filter based on surface mount technology (SMT). By introducing a matching network and utilizing the parasitic inductance characteristics of surface mount capacitors, it achieves the coordinated operation of low-pass and band-pass. Experiments have shown that parasitic inductance significantly improves the frequency selectivity and stop-band suppression ability of filters by generating transmission zeros in the high frequency range, providing an effective solution for simplifying the front-end architecture of multi-band communication systems.

The innovation of this design lies in combining the low cost and high consistency advantages of SMT technology with the beneficial utilization of parasitic parameters, providing new ideas for the development of high-performance and miniaturized filters.

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