(Received 28 July 2025, Accepted 17 August 2025, Scheduled 27 August 2025)

Bandpass Type Negative Group Delay Design of CMOS RC-Network Integrated Circuit

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ABSTRACT: Nowadays, microelectronic integrated circuit (IC) design constitutes the biggest challenge of negative group delay (NGD) electronic engineering research. Bandpass (BP) type NGD circuits are generally designed with resonant and not-integrable inductive large size network-based topology. However, BP-NGD circuit integrability is delimited by the inductor design. A design solution for fully resistive-capacitive (RC) network-based BP-type IC in 130-nm CMOS technology is the purpose of the present research work. The theory expressing the design equations of RC-network based BP-NGD circuit is developed. The design feasibility is verified with a proof-of-concept (POC) represented by a 130-nm CMOS RC-network passive IC with 0.68 mm$\times$ 0.72 mm physical size simulated by Cadence®. The obtained results of S-parameters confirm the BP-NGD behavior of the CMOS IC POC with 21.9-MHz NGD center frequency and -0.99-ns NGD value over 68-MHz NGD bandwidth. The BP-NGD characterization results are in excellent agreement with the theoretical model. The robustness of 130-nm CMOS BP-NGD RC passive IC is explored by 2000 trials Monte Carlo statistical analysis with respect to the uncertainty of component parameters.

1. INTRODUCTION

In recent years, Negative Group Delay (NGD) circuits have attracted increasing attention from researchers [1–3]. Realizing non-Foster elements, which can be exploited to design phased-array antennas [4, 5], as well as realizing equalization techniques [6], feedforward amplifiers [7], and constant phase shifters [8], represents some of the most promising applications of NGD circuits. A thermal wave variation prediction system with a minute-level time advance based on a low-pass NGD digital circuit was proposed [9]. An all-passband NGD (AP-NGD) circuit has been applied to finite impulse response (FIR) filters [10]. NGD technology has also been used to reduce parasitic RLC dispersion in cables, aiming to improve signal integrity (SI) and electromagnetic compatibility (EMC) [11]. An experimental method using an RC network topology for NGD-based sensor delay elimination was proposed, achieving millisecond-level delay removal [12]. A novel phase shifter with two-step phase transitions for potential 5G and 6G communication systems was implemented using a stopband NGD passive microwave circuit [13, 14]. NGD circuits have also been applied to design non-Foster inductors and capacitors for antenna applications. It is worth noting that the NGD phenomenon does not violate the principle of causality [15, 16]. Moreover, NGD circuits based on various microwave structures and lumped components have been synthesized into different topologies. Due to this diversity, non-specialist electronic circuit designers often struggle to understand the function and meaning of NGD. Similar to the classification theory of filters, a simpler and more fundamental theory of NGD circuits has been proposed. Studies have shown that all NGD circuits can be categorized based on the function of the NGD frequency band. Basic types of low-pass (LP) [17–19], high-pass (HP), and band-pass (BP) NGD functions have been classified.

With the rapid development of integrated circuit technology, the continuous scaling down of transistor feature sizes and advances in process nodes have laid a solid foundation for realizing high-performance and highly integrated chips. In this context, signal integrity and timing control have become critical challenges in fields such as high-speed communication, radar systems, and real-time signal processing [20, 21].

The application of NGD circuits in the integrated circuit domain has also continued to expand. An active LP-NGD circuit based on 180 nm CMOS technology has been proposed [22], confirming time-advance characteristics associated with both passive and active CMOS IC LP-NGD behaviors. An RL network-based HP-NGD circuit using 130 nm CMOS technology has verified the time-advance characteristics of HP NGD ICs [23]. A constant phase shifter (PS) based on 130 nm BiC-

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MOS and utilizing an RLC network BP-NGD structure demonstrated improvements in IC PS performance [24]. A 24 GHz source-degenerated tunable delay shifter with negative group delay compensation, based on a 65 nm CMOS process, further validated NGD as a highly promising choice for broadband time-array systems [25].

However, most researchers believe that BP NGD function is generated by resonant networks, and BP-NGD circuit design methods tend to use resonant RLC networks or transmission-line-based topologies. Transmission-line-based topologies are generally complex in design and difficult to integrate. BP-NGD circuits based on RLC resonant networks typically rely on inductive components, which pose two major challenges in practical chip implementation: first, planar spiral inductors occupy significant chip area in CMOS 180 nm technology and more advanced processes, greatly increasing manufacturing costs; second, many standard CMOS process design kits (PDKs) do not provide available inductor models, making inductor-based NGD designs difficult to implement in mainstream integrated circuits.

Therefore, eliminating reliance on inductive components and exploring novel inductorless band-pass NGD circuit architectures has become the key to pushing this technology toward practical chip applications. Existing inductorless BP-NGD circuit designs are limited to proof-of-concept (POC) implementations based on lumped components, and no research on integrated inductorless BP-NGD circuits has yet been reported in the literature [26–29]. Inductorless NGD units offer the potential for integration, miniaturization, and wide-band operation.

This paper, based on the 130 nm CMOS process, investigates design methodologies for inductorless BP-NGD circuits, aiming to realize highly integrated, low-cost on-chip NGD solutions, and to provide feasible paths for applications in high-speed communication and real-time signal processing.

The paper is organized in five sections as follows:

- Section 2 explores the S-matrix modelling of the fundamental L-topology of lumper passive cell representing the BP-NGD circuit under study.
- Section 3 develops the circuit theory of BP-NGD type inductorless RC-network topology. Furthermore, the different steps to be fulfilled are described for the BP-NGD IC design methodology in CMOS technology.
- Section 4 describes the schematic and layout design of the proof of concept (POC). The BP-NGD inductorless IC is designed in 130-nm CMOS technology.
- Section 5 focuses on the BP-NGD feasibility study with the 130-nm BP-NGD RC-network based IC. The comparison of calculated models and simulations in both frequency and time domain validation results with uncertainty Monte Carlo (MC) analysis is discussed.
- Section 6 is the final conclusion.

2. MODELLING THEORY OF THE CONSIDERED RC-NETWORK BP-NGD TOPOLOGY

After the topological description, the modelling of S-matrix is described in the present section. Then, the fundamental specifications of the BP-NGD function are defined.

2.1. Analytical Modelling

The L-shape topology shown in Fig. 1, composed by impedances Z_1 and Z_2, represents the general circuit under study.

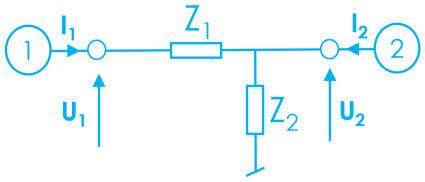

FIGURE 1. L-shape passive topology.

By denoting the Laplace and angular frequency variable, $p = j\omega$ and the angular frequency, ω, one can demonstrate from the voltage $[U_1(p)\ U_2(p)]$ and current $[I_1(p)\ I_2(p)]$ vectors, and the corresponding Z-matrix is given by:

$$[Z(p)] = \begin{bmatrix} Z_1(p) + Z_2(p) & Z_2(p) \\ Z_2(p) & Z_2(p) \end{bmatrix}. \tag{1}$$

One recalls that according to the circuit theory, the Z-to-S-matrix transform is written as:

$$[S(p)] = \left([Z(p)] - R_0 \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\right) \times \left([Z(p)] + R_0 \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\right)^{-1} \tag{2}$$

with reference impedance equal to $R_0 = 50\,\Omega$. Substituting impedance expressed in (1) into the previous relationship, we have the S-matrix model given by:

$$[S(p)] = \frac{\begin{bmatrix} Z_1(R_0 + Z_2) - R_0^2 & 2R_0Z_2 \\ 2R_0Z_2 & Z_1Z_2 - R_0(R_0 + Z_1) \end{bmatrix}}{R_0^2 + R_0(Z_1 + Z_2) + Z_1Z_2}. \tag{3}$$

Knowing the S-matrix model, the BP-NGD analysis is performed by means of frequency domain characterization. The BP-NGD analysis is based on the consideration of S-parameter magnitudes, $S_{11}(\omega) = |S_{11}(j\omega)|$, $S_{21}(\omega) = |S_{12}(\omega) = |S_{21}(j\omega)|$ and $S_{22}(\omega) = |S_{22}(j\omega)|$, and also the GD:

$$GD(\omega) = \frac{-\partial \arg\left[S_{21}(j\omega)\right]}{\partial\omega}. \tag{4}$$

For the further understanding about the analysis of BP-type NGD function, a brief recall on its basic parameters and specifications will be defined in the following subsection.

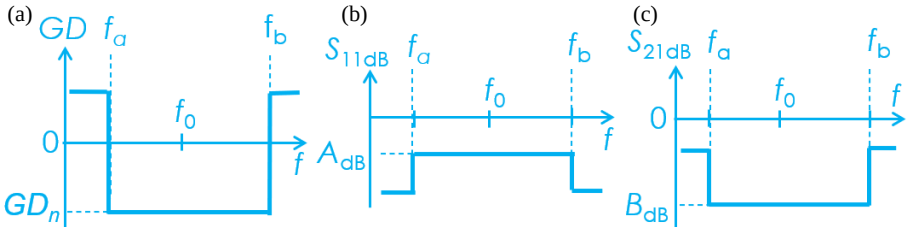

FIGURE 2. (a) GD, (b) S_{11}, and (c) S_{21} specific diagrams of ideal BP-NGD frequency responses.

TABLE 1. Notable differences between NGD and filter specifications.

Specification	BP-NGD function	BP-filter
Key parameter	GD	Transmission coefficient magnitude S_{21}
Cut-off frequency	Roots of $GD(f)$ =0	Root of $S_{21}(f) = S_{21\,\max}/\sqrt{2}$
Frequency band of f_0	$GD(f) \leq 0$	$S_{21}(f) \geq S_{21\,\max}/\sqrt{2}$
Out of band	$GD(f) > 0$	$S_{21}(f) < S_{21\,\max}/\sqrt{2}$

2.2. BP-NGD Technical Basic Definition

Similar to filter theory, BP-type NGD response is defined in function of the existence of frequency band where GD becomes negative $GD(\omega) < 0$. The GD response of BP-type NGD characteristics can be represented as shown in top of Fig. 2(a). The reflection and transmission coefficient responses which are assumed to be plotted in dB are illustrated by Fig. 2(b) and Fig. 2(c).

According to this ideal diagram, the BP-type NGD analysis is fundamentally the determination of the specifications of the circuit. For example, the NGD cut-off frequencies $f_1 < f_2$ are the roots of the GD $GD(f_1) = 0$ and $GD(f_2) = 0$. Consequently, the NGD bandwidth is expressed as $\Delta f = f_2 - f_1$. Furthermore, the NGD center frequency corresponds to the NGD value:

$$GD(f_0) = GD_n < 0. \tag{5}$$

In addition to the GD specifications, in the NGD frequency band or at the NGD center frequency, we suppose the reflection coefficient associated by the given limit of real positive constant, $A < 1$ as $S_{11}(f_0) = A$. Moreover, the transmission coefficient is similarly characterized in function of the given limit of real positive constant, $B < 1$ as $S_{21}(f_0) = B$.

2.3. Differences between BP-NGD and BP-Filter Specifications

Despite the initiated fundamental circuit theory [25, 26] which identifies the basic specifications of BP-NGD function, one may confuse the uncommon function with the filter. However, there are notable differences in terms of specifications. The electronic circuit characteristics should not be only limited to the transfer function magnitudes. Further circuit theory on non-familiar parameter as GD should also be considered in the future in order to extend the research fields in electronic engineering. As simple way to be familiar to NGD function, Table 1 addresses the main differences between the definition of BP-NGD and BP-filter key parameters as cut-off frequency, working frequency band, and out of band.

The definition of $GD(f) < 0$ bandwidth is applicable in time-domain waveform/signal analysis, provided that the S_{21} magnitude deviation within this bandwidth is less than 3 dB (approximately a $\sqrt{2}$ factor). However, for NGD designs with large out-of-band gain (or center-frequency attenuation) — typically exceeding about 6 dB — the in-band magnitude variation (shown to be approximately equal to one-half of the out-of-band gain in decibels [30]) will exceed 3 dB, which may introduce correspondingly significant distortion to the input waveform. In such cases, the 3-dB bandwidth (BW_3 dB), which will be smaller than BW_$\{GD < 0\}$, should also be reported as a performance metric. More detailed circuit theory enabling to determine the BP-NGD IC in CMOS technology and to carry out the design method is the main focus of the following section.

3. ANALYTICAL EXPRESSION, SYNTHESIS EQUATION AND DESIGN METHOD OF CONSIDERED BP-NGD IC IN CMOS TECHNOLOGY

The theoretical approach established from RC-parameter based model and the design method of IC in CMOS technology operating as BP-NGD function are described in this subsection.

3.1. *S*-Parameter Modelling Versus RC-Parameters

Figures 3 presents the L-shape topologies constituting the passive circuit under study. The BP-NGD topology shown in Fig. 3(c) acts as a passive RC-network based circuit constituted by lumped resistor R_1, capacitor C_1, resistor R_2, and capacitor C_2 components. Let us denote the analytical impedances constituting the BP-NGD cell expressed as:

$$\begin{cases} Z_1(p) = \dfrac{R_1}{1 + R_1 C_1 p} \\ Z_2(p) = R_1 + \dfrac{1}{C_2 p} \end{cases}. \tag{6}$$

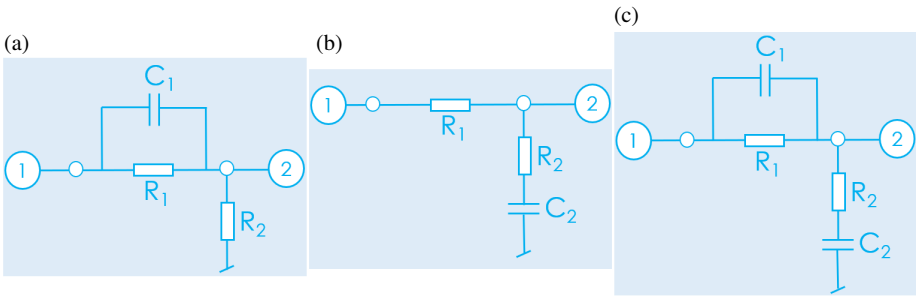

FIGURE 3. RC-passive (a) LP-, (b) HP-, and (c) BP-topology under study.

A distinctive study [16] showed the similarity between the functions of RLC filters and NGD functions. Extensive work [31] has even established LP- (Fig. 3(a)), HP- (Fig. 3(b)), and BP- (Fig. 3(c)) NGD function equivalence for some referent RLC filter topologies. From the given NGD specifications, it is possible to find RLC-component parameters of the corresponding circuit, and vice versa. Substituting Z_1 and Z_2 into the S-parameters given in Equation (2), the models of reflection and transmission coefficients are formulated in function of R_1, C_1, R_2, and C_2.

The associated expressions are given by:

$$S_{11}(p) = \frac{c_2^{11}p^2 + c_1^{11}p + c_0^{11}}{c_2p^2 + c_1p + c_0} \tag{7}$$

$$S_{21}(p) = \frac{c_2^{21}p^2 + c_1^{21}p + c_0^{21}}{c_2p^2 + c_1p + c_0} \tag{8}$$

$$S_{22}(p) = \frac{c_2^{22}p^2 + c_1^{22}p + c_0^{22}}{c_2p^2 + c_1p + c_0} \tag{9}$$

with:

$$\begin{cases} c_2^{11} = -R_0^2R_1C_1C_2 \\ c_1^{11} = C_2[R_1(R_0+R_2) - R_0^2] \\ c_0^{11} = R_1 \\ c_2^{21} = R_0^2R_1C_1C_2 \\ c_1^{21} = C_2[R_0(R_0+R_1) - R_1R_2] \\ c_0^{21} = -R_1 \\ c_2^{22} = R_1C_1C_2^2(R_0^2 - R_0R_2 + R_2^2) \\ c_1^{22} = C_2^2(R_0^2 - R_0R_2 + R_2^2) \\ \quad +R_1C_1C_2(2R_2 - R_0) \\ c_0^{22} = R_1C_1 + C_2(2R_2 - R_0) \\ c_3 = R_0R_1C_1C_2(R_0 + 2R_2) \\ c_2 = 2R_0R_1C_1 + C_2[R_0(R_0 + R_1 \\ \quad +2R_2) + R_1R_2] \\ c_1 = 2R_0 + R_1 \end{cases}. \tag{10}$$

Due to the mathematical complexity of the BP-NGD circuit GD, we propose a simpler approach to establish the design equations by means of LP- and HP-NGD cells in the following subsection.

3.2. LP- and HP-NGD Cut-off Frequencies

By taking $Z_1(p)$ defined in Equation (6) and $Z_2(p) = R_2$, the S-parameter model of LP-NGD circuit presented in Fig. 3(a) derived from Equation (3) becomes:

$$[S_{LP}(p)] = \frac{\begin{bmatrix} R_1(R_0+R_2) & 2R_0R_2\zeta(p) \\ -R_0^2\zeta(p) & \\ 2R_0R_2\zeta(p) & R_1(R_2-R_0) - R_0^2\zeta(p) \end{bmatrix}}{\begin{matrix} R_0R_1C_1(R_0+2R_2)p + R_0^2 \\ +R_0(R_1+2R_2) + R_1R_2 \end{matrix}} \tag{11}$$

with $\zeta(p) = 1 + R_1C_1p$. Under the same way, the S-matrix model of HP-NGD shown in Fig. 3(b) determined by taking $Z_1(p) = R_1$ and $Z_2(p)$ defined in Equation (6) becomes:

$$[S_{HP}(p)] = \frac{\begin{bmatrix} R_0C_2(R_1-R_0)p & 2R_0\chi(p) \\ +R_1\chi(p) & \\ 2R_0(1+R_2C_2p)\chi(p) & R_1\chi(p) \\ & -R_0C_2(R_0+R_1)p \end{bmatrix}}{C_2[R_0^2+R_0(R_1+2R_2)+R_1R_2]p + 2R_0 + R_1} \tag{12}$$

with $\chi(p) = 1+R_2C_2p$. Based on the NGD circuit theory [25], we can demonstrate that the associated LP- and HP-NGD cut-off frequencies from their GDs are expressed as, respectively:

$$f_{LP} = \frac{R_0^2 + R_0(R_1+2R_2) + R_1R_2}{2\pi R_0R_1^2C_1^2(R_0+2R_2)} \tag{13}$$

$$f_{HP} = \frac{2R_0 + R_1}{2\pi R_2C_2^2[R_0(R_0+R_1+2R_2) + R_1R_2}. \tag{14}$$

It is worth to note that the maximum reflection and minimum transmission coefficients of LP-NGD cell which are calculated at very low frequencies are given by, respectively:

$$S_{11LP\,\max} = \frac{R_1(R_0+R_2) - R_0^2}{R_0^2 + R_0(R_1+R_2) + R_1R_2} \tag{15}$$

$$S_{21LP\,\min} = \frac{2R_0R_2}{R_0^2 + R_0(R_1+R_2) + R_1R_2}. \tag{16}$$

By means of the GD diagram for the LP- and HP-NGD graphical analysis, the NGD parameters are established based on the circuit parameters in the next subsection.

3.3. Synthesis Design Equations Versus NGD and *S*-Parameter Specification Goals

This synthesis approach consists in establishing the design equations of constituting components R_1, R_2, C_1, and C_2 in function of BP-NGD specification goals. By choosing A and B, the resistors are extracted by solving the equations $S_{11\,\max} = A$ and $S_{21\,\min} = B$. Substantially, we have the design formulas:

$$R_1 = \frac{(1 + A - B)R_0}{1 - A} \tag{17}$$

$$R_2 = \frac{B\,R_0}{1 - A - B}. \tag{18}$$

The relations were exploited to determine the BP-NGD circuit design equations by choosing $f_{HP} < f_0 < f_{LP}$ which yields the condition:

$$C_2 > C_{2\,\min} = \lambda\, C_1 = \frac{R_1\sqrt{R_0(R_0 + 2R_2)(2R_0 + R_1)}}{\sqrt{R_2}[R_0(R_0 + R_1 + 2R_2) + R_1R_2]}. \tag{19}$$

Substituting resistor design Equations (17) and (18) into the last expression, we have:

$$\lambda = \frac{[(1 - B)^2 - A^2]\sqrt{(1 - A + B)(3 - A - B)}}{2(1 - A)\sqrt{B(1 - A)}}. \tag{20}$$

The C_1 design equation is established by taking f_b as the cut-off frequency of LP-NGD circuit proposed in Fig. 3(a). After simplification, we have the design equation:

$$C_1 = \frac{(1 - A)\sqrt{2}}{2\pi(1 - A + B)f_bR_0\sqrt{1 + B - A}}. \tag{21}$$

Then, the C_2 one is similarly established by taking f_a as the HP-NGD cut-off frequency. It implies the following formula:

$$C_2 = \frac{(1 - A - B)\sqrt{3 - A - B}}{2\sqrt{2}\pi(1 - A)f_aR_0}. \tag{22}$$

By using the established analytical equations, the design methodology of the inductorless BP-NGD IC in CMOS technology is described in the following subsection.

3.4. Design Methodology of BP-NGD CMOS IC

The synthesis and design methodology of the investigated BP-NGD RC network as an IC implemented in CMOS technology is described in the present subsection. The developed methodology refers to Cadence® IC simulator commercial tool. The main successive actions of the BP-NGD IC POC can be organized in eight steps as illustrated by the design flow of Fig. 4.

Despite the counterintuitive aspect, similar to the case of classical electronic functions, its main actions of the BP-NGD CMOS IC design are:

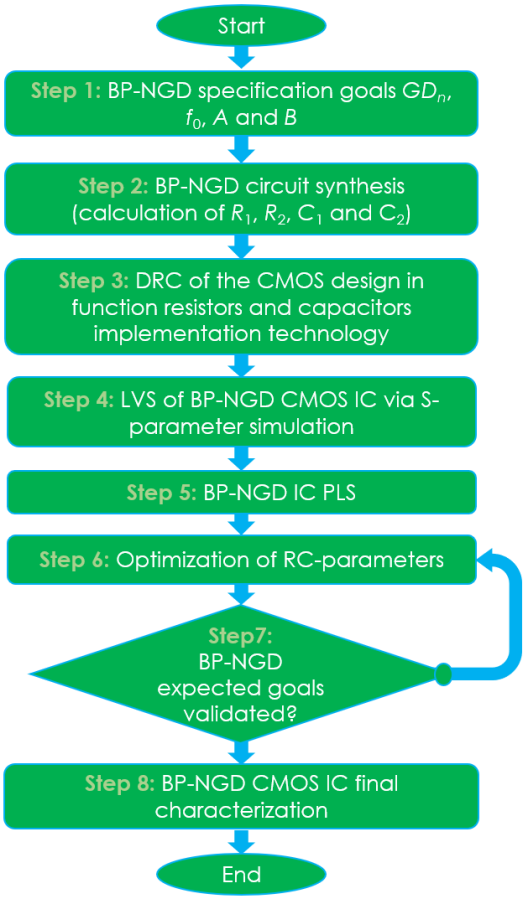

FIGURE 4. Workflow indicating CMOS BP-NGD IC design.

- Step 1: The starting task of the electronic circuit engineering methodology is to set the design goals definition of the inductorless BP-NGD POC expected specifications as (GD_n, f_0, $\Delta f = f_b - f_a$) and also the reflection and transmission coefficients, ($S_{11\,\max}$, $S_{21\,\min}$, $S_{22\,\max}$).

- Step 2: The preliminary resistor and capacitor values of RC elements constituting the BP-NGD IC POC are calculated from the design Equations (17) and (18), and Equations (21) and (22). The LP- and HP-NGD ideal cell S-parameter models formulated by Equations (11) and (12) should be computed, for example, by means of MATLAB® program. Then, the schematic of BP-NGD circuit can be optimized by considering the calculated initial values.

- Step 3: According to the considered CMOS technology, the design rule checking (DRC) phase must be elaborated. The resistor and capacitor values should belong to the realistic range of implementable ones, for example, in high ohmic unsalicided N+poly resistor and metal-insulator-metal (MIM) multi-layer technology, respectively.

- Step 4: As first step of the POC feasibility study, the S-parameter simulation of the BP-NGD lumped can be performed in the schematic environment. The layout design can be elaborated in order to check the influence of the

TABLE 2. Expected specifications to design an ideal BP-NGD POC.

Description	Specification	Name	Value
NGD specifications	BP-NGD center frequency	f_0	25 MHz
	BP-NGD bandwidth	Δf	60 MHz
	LP-NGD cut-off frequency	f_{LP}	15 MHz
	HP-NGD cut-off frequency	f_{HP}	70 MHz
S-parameters	Reflection coefficient	$S_{11\,\max}$	-12 dB
	Transmission coefficient	$S_{21\,\min}$	-5 dB
Synthesized components	Resistor	R_1	56 Ω
		R_2	150.8 Ω
	Capacitor	C_1	71.2 pF
		C_2	63.8 pF

CMOS technology. The layout versus schematic (LVS) is the step enabling the confirmation of the design feasibility.

- Step 5: Because of the technology design imperfections, it is important to pay attention to the designed realistic environment layout BP-NGD performance. To do this, the post-layout simulation (PLS) can be assessed with the final verification of parameters (GD_n, f_0, $\Delta f = f_b - f_a$) and ($S_{11\,\max}$, $S_{21\,\min}$, $S_{22\,\max}$).
- Step 6: The optimization of the RC-components is generally necessary in order to meet better performances of the POC with respect to the BP-NGD specification goals initially defined in Step 1.
- Step 7: The process of RC-component value optimization ends when the BP-NGD specifications goals are achieved.
- Step 8: The final BP-NGD characterization can be performed once the BP-NGD CMOS IC POC is well designed.

To verify the design feasibility, the following section will reveal the validation results. To verify the design feasibility, the following section will reveal the validation results.

4. DESIGN DESCRIPTION OF RC-NETWORK CMOS IC POC WITH BP-NGD FUNCTION

By using the synthesis equations from the constituting LP- and HP-cell previously established, the POC of BP-NGD CMOS IC is designed in this section with respect to the BP-NGD specifications.

4.1. Description of BP-NGD CMOS IC Schematic Design

The main object of this feasibility study is to design and validate a BP-NGD IC POC of the previously theorized topology in a 130-nm CMOS technology. The different steps of the circuit study were elaborated following the flowchart introduced in Fig. 4. First, the targeted specifications of the BP-NGD function as NGD value GD_n in the considered working frequency band with center frequency f_0 and NGD bandwidth Δf were fixed. The convenient LP- and HP-NGD cut-off frequencies f_{LP} and f_{HP} were adequately chosen. In addition to the NGD requirements, the reflection and transmission coefficient limits were also fixed $S_{11} < S_{11\,\max}$, $S_{21} < S_{21\,\min}$, and $S_{22} < S_{22\,\max}$. The assumed values of the NGD and S-parameter required specifications are recapitulated in Table 2. The ideal component parameters R_1, R_2, C_1, and C_2 are calculated from the given specifications. Fig. 5(a) and Fig. 5(b) display the calculated GD and S-parameters of the LP- and HP-NGD circuits synthesized from design Equations (17), (18), (21), and (22).

The expected LP- and HP-behaviors are confirmed by the black solid and red dashed lines plotted in Fig. 5(a). The associated reflection and transmission coefficients are shown in Fig. 5(b). Moreover, the synthesized NGD circuits present insertion loss which does not exceed 5 dB and matching better level than 10 dB.

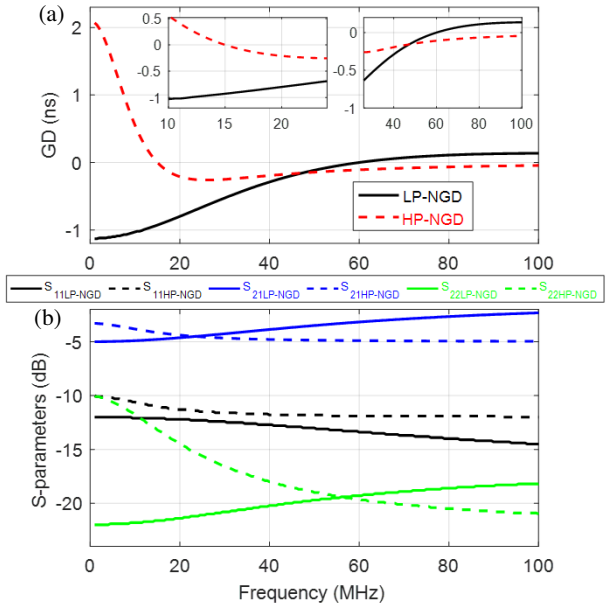

FIGURE 5. Calculated (a) GD and (b) S-parameter responses of synthesized LP- and HP-cells constituting components of the BP-NGD IC POC.

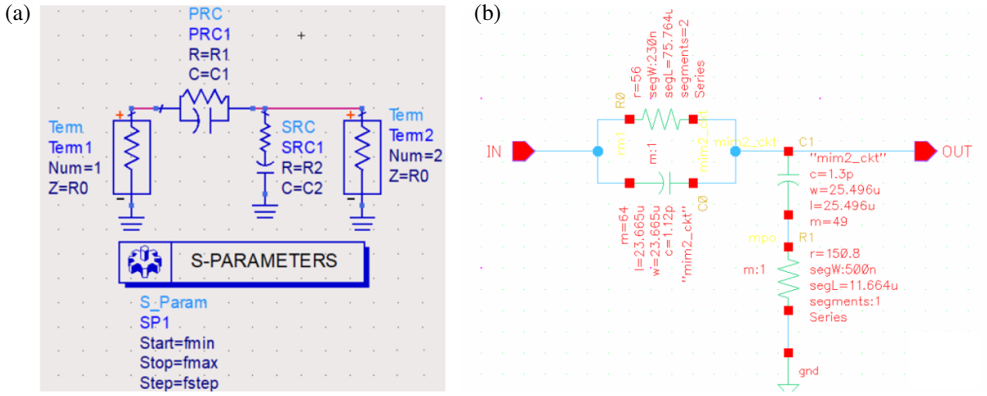

FIGURE 6. (a) ADS® and (b) Cadence® schematic design of BP-NGD CMOS IC POC.

4.2. Description of BP-NGD CMOS IC Schematic Design

Before more realistic design of POC, the BP-NGD passive RC-network lumped classical circuit was schematized in the commercial tool simulators. Furthermore, the IC POC is designed in 130-nm CMOS technology. The feasibility study is carried out by simulations with POC modeled in the environment of commercial tools ADS® from Keysight Technologies® platform Cadence® Virtuoso from Orcad®. After the consideration of ideal LP- and HP-NGD components addressed previously in Table 2, the POC circuit is optimized in order to meet the expected specifications. Accordingly, Fig. 6(a) and Fig. 6(b) present the passive BP-NGD IC designed in the ADS® and Cadence® Virtuoso schematic environment, respectively. The excitation ports are represented by the standard ports with reference load R_0. After the first optimization, the schematics of optimized values R_1, R_2, C_1, and C_2 are listed in the third column of Table 3.

TABLE 3. Optimized schematic and layout component values.

Nature	Parameters	Optimized schematic value	Optimized layout value
Resistor	R_1	33 Ω	37 Ω
	R_2	68 Ω	72 Ω
Capacitor	C_1	100 pF	4 × 26 pF
	C_2	100 pF	4 × 26 pF

The schematic design of the BP-NGD CMOSIC is described in the next subsection.

After the DRC of the POC schematic, four parallel identical capacitors were considered to design C_1 and C_2 values fixed to 26 pF constituting the CMOS IC Cadence® layout. As per previous comment, $GD(f) < 0$ cut-off, 60 MHz (Fig. 5(a), solid black line), in this case is corroborated to correspond to S_{21} magnitude in-band deviation of approximately insertion_loss_dB/2 = 5 dB/2 = 2.5 dB (solid blue line in Fig. 5(b) at 60 MHz), as per [30] discussion. In this case, this is lower than 3 dB variation. Therefore, distortion is not a concern, and it is ok to keep $GD(f) < 0$ bandwidth and no need to specify 3 dB bandwidth in this application.

The design of the POC 130-nm CMOS layout is described in the next subsection.

4.3. Description of BP-NGD CMOS IC Layout Design

Because of the potential integration of RC-components in the range of desired specification values, STMicroelectronics® 130-nm CMOS manufacturing process was chosen as the main reference to design the BP-NGD IC layout corresponding to the schematic shown in Fig. 6. Accordingly, Fig. 7 represents the Cadence® layout of the BP-NGD IC POC in 130-nm CMOS technology having compact physical size with 0.44 mm × 0.3 mm. Due to the relatively large size of the components, expensive manufacturing processes such as 28 nm-FDSOI are not needed.

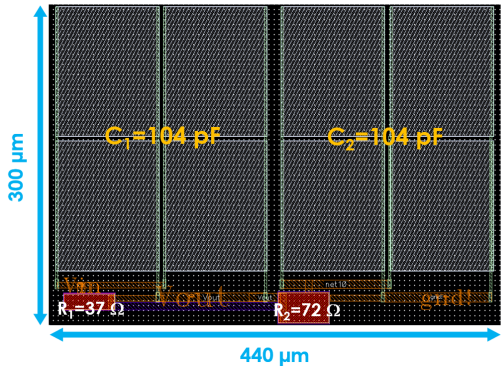

FIGURE 7. Cadence® layout design of BP-NGD CMOS IC POC.

This work employs MIM capacitors, which have a parallel-plate structure. MIM capacitors exhibit relatively low capacitance per unit area, resulting in high capacitance precision, with a minimum capacitance value as low as 28 fF. For resistors, Silicide Polygate (rpo) polysilicon resistors are used. These resistors offer high matching accuracy and low parasitic effects, making them key components in analog circuits. However, due to their small sheet resistance, the minimum achievable resistance value is only 4 Ω, making them suitable for medium to low resistance applications. For higher resistance requirements, alternative processes or off-chip solutions are necessary. The range of the geometrical parameters (width w, length d, Sili-

TABLE 4. Ranges of geometrical parameters of the used designed 130-nm CMOS resistors.

Description	Design technology	Width, w (µm)		Length, d (µm)		RC-values	
Parameter	rpo1b resistor	w_{min}	w_{max}	d_{min}	d_{max}	R_{min}	R_{max}
Value		1	100	3	100	4 Ω	13 kΩ
Parameter	Cmim_2p capacitor	w_{min}	w_{max}	d_{min}	d_{max}	C_{min}	C_{max}
Value		3.5	140	3.5	140	28 fF	40 nF

cium area) of the considered resistor and capacitor layouts in function of the constituting materials are addressed in Table 4.

In chip layout design, achieving a compact layout is essential to reducing manufacturing costs. Additionally, to minimize parasitic effects within the chip, the layout should adhere to the principle of central symmetry. The MIM capacitors designed in this work specifically address this by employing a symmetrical distribution, which helps enhance the stability and consistency of circuit performance. Process metal density has a significant impact on the parasitic effects of MIM capacitors. In CMOS processes, to meet the metal density requirements of design rule checks (DRCs), dummy metals are often filled in empty areas. These dummy metals, being adjacent to the MIM capacitor metal layers, can form additional parasitic capacitances and inductances, resulting in capacitance deviations and signal distortion. Furthermore, parasitic coupling can affect the circuit frequency response and phase characteristics, reducing the stability and performance of negative group delay circuits. Therefore, during layout design, it is essential to carefully plan the placement and method of metal density fills, maintaining sufficient spacing between MIM capacitors and dummy metals to minimize the impact of parasitic effects on circuit performance.

The minimal and maximal limits of the constituting R and C components are denoted by (R_{min}, C_{min}) and (R_{max}, C_{max}) for the BP-NGD IC layout configuration, respectively. For the capacitors, the limits come from the total surface area of the component. Meanwhile, the limit values indicated in Table 4 depend on the square components. We can see that the bulkiest elements of the BP-NGD IC layout cover more than 90% of the total surface. These cumbersome components are MIM capacitors. LVS was carried out in the Cadence® environment from the designed POC. The obtained results from the investigation in the BP-NGD frequency and time domain behaviors are discussed in the following subsection.

5. FEASIBILITY STUDY ILLUSTRATING THE BP-NGD BEHAVIOR OF RC-NETWORK CMOS IC POC

This section reveals the BP-NGD feasibility study of RC-network topology described in the previous section. The POC of CMOS IC is investigated both in frequency and time domain.

5.1. Frequency Domain Analysis of the BP-NGD CMOS IC Outcome

The frequency domain analysis validating the BP-NGD behavior of the IC design in 130-nm technology is explored in the present subsection.

5.1.1. BP-NGD Behavioral Validation Results

To validate the BP-NGD specification, the GD and S-parameter responses of the CMOS IC POC are calculated from the theory and simulated by using ADS® and Cadence® commercial tools. The performed calculations are computed via MATLAB® programming of analytical S-parameter models expressed in Equations (6), (8), and (9) of Subsection 3.1.

The POC modelling results associated with the GDs and S-parameters plotted in Fig. 8 and in Fig. 9 were obtained in the frequency band defined from $f_{min} = 1$ MHz to $f_{max} = 0.1$ GHz, respectively. Fig. 8(a) plots the comparison of the theoretical and simulated responses corresponding to the calculated (solid red curve), ADS® schematic (dashed green curve), Cadence® schematic (dotted blue curve), and Cadence® layout (solid black curve) simulated GD diagrams plotted in the frequency band [1 MHz, 0.1 GHz]. A good agreement between the theory and simulations from schematic and layout environment is observed in Fig. 8 and Fig. 9. To better highlight the BP-NGD behavioral responses of the CMOS IC POC, the zoom-in plots in narrower bands [5 MHz, 25 MHz] and [60 MHz, 0.1 GHz] showing the lower and upper cut-off frequencies are displayed in Fig. 8(b) and Fig. 8(c), respectively. The differences between the BP-NGD specifications based on the theoretical and simulated results are shown in Table 5.

The obtained results confirm the BP-NGD behavior of the CMOS IC POC. As expected in Fig. 8(a), the optimized BP-NGD IC POC generates NGD value about $GD_n = -0.99$ ns

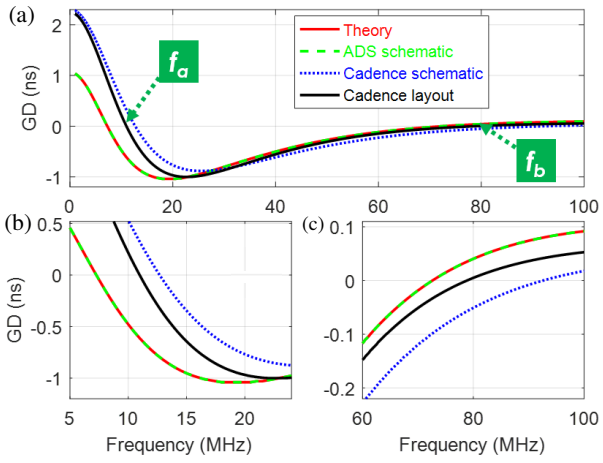

FIGURE 8. Comparison of BP-NGD GD diagrams in the frequency bands (a) [1 MHz, 100 MHz], (b) [5 MHz, 25 MHz] and (c) [60 MHz, 100 MHz] from theoretical calculation, schematic and layout simulations.

TABLE 5. Comparison of theoretical and simulated BP-NGD characteristics.

Characteristics	Parameter	Theory	Schematic	Layout
GD diagram	GD_n	-1.04 ns	-0.88 ns	-0.99 ns
	f_0	18 MHz	25.12 MHz	21.98 MHz
	f_a	7.5 MHz	12.7 MHz	10.96 MHz
	f_b	73 MHz	92.9 MHz	79.07 MHz
S-parameter diagrams	$S_{11\,\max}$	-10.9 dB	-13.26 dB	-12.46 dB
	$S_{21\,\min}$	-4.07 dB	-4.26 dB	-4.32 dB
	$S_{22\,\max}$	-13.2 dB	-12.74 dB	-11.4 dB

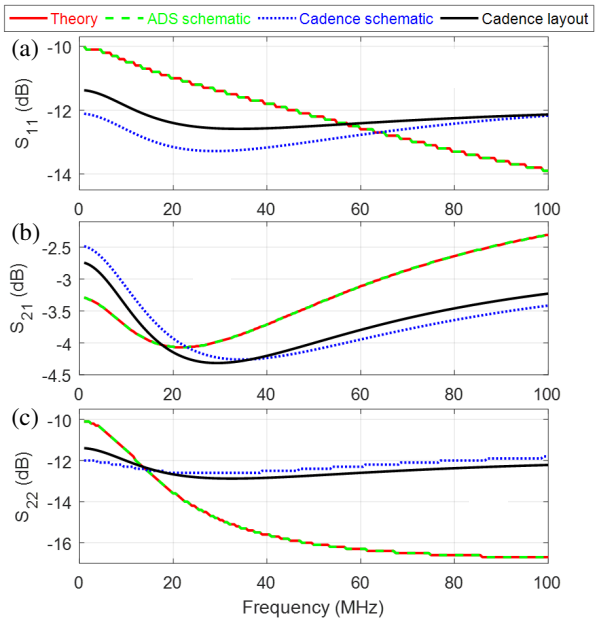

FIGURE 9. Comparisons of (a) S_{11}, (b) S_{21}, and (c) S_{22} theoretical, schematic and layout simulation BP-NGD CMOS IC POC.

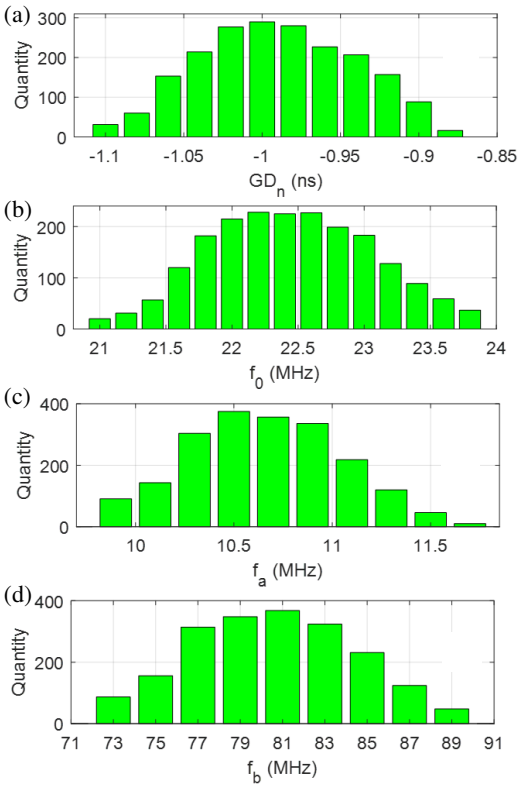

FIGURE 10. (a) GD_n, (b) f_0, (c) f_a, and (d) f_b histograms from MC analyses of CMOS BP-NGD IC layout with $+/-5\%$ standard deviation.

at the center frequency around $f_0 = 21.98$ MHz. In addition to the GD diagram analysis, the comparisons of calculated and simulated S-parameter magnitudes, S_{11}, S_{21}, and S_{22} calculated from Equation (6), Equation (8), and Equation (9), and the optimized circuit simulation are displayed in Fig. 9(a), Fig. 9(b), and Fig. 9(c), respectively. As expected, the optimized BP-NGD CMOS IC POC operates with targeted insertion loss and access matching with respect to the specifications previously targeted in Table 2. As the LVS highlights non-negligible influence of geometrical parameters on the BP-NGD specifications, the BP-NGD CMOS IC PLS including constituting RC component uncertainty is necessary. To study the parametric influences quantitatively, the MC uncertainty statistical analysis is discussed in the following subsection.

5.1.2. Uncertainty MC Analyses

The BP-NGD IC LVS was accomplished with the inaccuracy analyses with respect to the simultaneous variation of physical parameters of components constituting the POC layout. After computation, the S-parameter MC analyses were run in Cadence®. The statistical computation was performed with 2000 samples by considering random variations of resistor and capacitor component parameters with $+/-5\%$ standard deviations. The used component parameters were simultaneously varied according to Gaussian law during the S-parameter simulations. As results, we get the histograms of simulated BP-NGD parameters GD_n, f_0, f_a, and f_b displayed by Fig. 10(a), Fig. 10(b), Fig. 10(c), and Fig. 10(d), respectively.

A rather Gaussian behavior of BP-NGD specifications quantified by the variations of GD_n, f_0, f_a, and f_b is observed in Fig. 10. Furthermore, Table 6 summarizes the GD_n, f_0, f_a, and f_b minimal, maximal, mean values and standard deviations of each BP-NGD parameter. Based on the obtained histograms, the statistical range of GD_n, f_0, f_a, and f_b confirms the robustness of the 130-nm CMOS IC to operate as a BP-NGD function despite the component physical parameter variations.

TABLE 6. Minimal, maximal, mean values and standard deviations of the BP-NGD characteristics of the 130-nm CMOS layout.

Function	Characteristics	Minimum	Maximum	Mean values	Standard deviations	Variation percentage
NGD function	GD_n	-1.16 ns	-0.84 ns	-1.01 ns	0.035 ns	3.46%
	f_0	20.2 MHz	24.8 MHz	22.6 MHz	0.762 MHz	29.3%
	f_a	9.7 MHz	11.9 MHz	10.9 MHz	0.404 MHz	3.7%
	f_b	71 MHz	91 MHz	78.4 MHz	2.96 MHz	3.77%
S-parameter	$S_{11\,\max}$	-11.75 dB	-11.15 dB	-11.39 dB	0.137 dB	0.32%
	$S_{21\,\min}$	-4.345 dB	-4.275 dB	-4.31 dB	0.0123 dB	0.028%

TABLE 7. Comparison of theoretical and simulated BP-NGD characteristics.

Ref.	f	GD (ns)	BW (MHz)	S_{11} (dB)	S_{21} (dB)	size	Integrated circuitry?
31	0.55 MHz	-18.12	1.35	-9.83	-2.95	centimeter level	NO
32	3.72 MHz	-8.5	18.7	-6.79	-6.9	centimeter level	NO
33	2.14 GHz	-1.11	140	-22.3	-9.75	112 mm $\times$ 62 mm	NO
34	1.57 GHz	-8.7	60	-32	-20	37.3 $\times$ 18.2 mm	NO
35	16.4 MHz	-1.96	75	-9.8	-7.1	29 mm $\times$ 18 mm	NO
This work	**21.9 MHz**	**-0.99**	**68**	**-11.39**	**-4.31**	**0.68 mm $\times$ 0.72 mm**	**YES**

In addition to the BP-NGD characteristics, the maximal and minimal reflection and transmission coefficients, $\max(S_{11\,\mathrm{dB}})$ and $\min(S_{21\,\mathrm{dB}})$, were also analyzed by MC statistical computations. The $\max(S_{11\,\mathrm{dB}})$ and $\min(S_{21\,\mathrm{dB}})$ of 130-nm CMOS IC POC histograms are displayed by Fig. 11(a) and Fig. 11(b), respectively. The last row of Table 6 addresses the corresponding minimal, maximal, mean values and standard deviations.

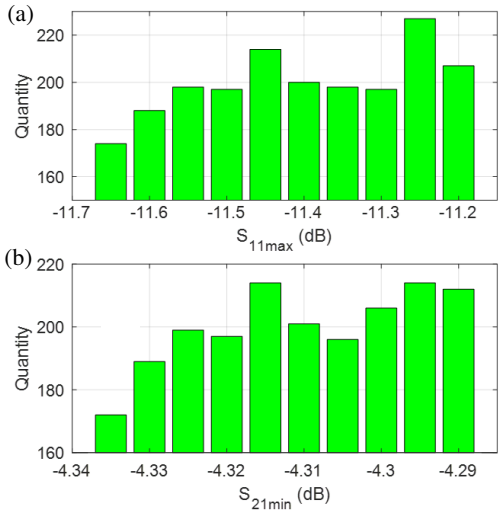

FIGURE 11. (a) $\max(S_{11\,\mathrm{dB}})$ and (b) $\min(S_{21\,\mathrm{dB}})$ (b) histograms from MC analyses of CMOS BP-NGD IC layout with $+/-5\%$ standard deviation.

The $\max(S_{11\,\mathrm{dB}})$ and $\min(S_{21\,\mathrm{dB}})$ MC analysis results confirm the robustness of the designed BP-NGD IC in 130-nm CMOS technology. We can emphasize from the MC analyses that the BP-NGD behavior of the 130-nm CMOS IC POC is preserved despite the layout parameter variations.

As shown in Table 7, the proposed inductorless BP-NGD IC circuit demonstrates an excellent insertion loss (-4.31 dB) and return Loss (-11.39 dB) compared to existing works [31–35]. Additionally, it offers a delay of -1.01 ns and a group delay bandwidth of 78.4 MHz. The physical size is only 0.68 mm $\times$ 0.72 mm, enabling direct on-chip integration.

5.2. BP-NGD Transient Analysis

The time-domain behavioral validation which enables the rigorous illustration of BP-NGD interpretation remains a challenging work for NGD engineers. To do this, arbitrary waveform transient signals were assumed as the input of the 130-nm CMOS RC-network based IC POC. In order to highlight the difference between the LP- and BP-NGD behaviors and time-domain responses, transient analyses are simulated by the consideration of:

- Baseband input-output signals denoted by pair $(input, output) = (v_{ip}, v_{op})$ with spectra plotted in blue solid and pink dashed curves of Fig. 12 whose power density is concentrated in lower frequencies $f \leq f_a$.

- Modulated input-output signals with carrier frequency f_0 denoted by pair $(input, output) = (v_{in}, v_{on})$ whose power density is concentrated in the frequency band $f_a \leq f \leq f_b$ corresponding to spectra plotted in black solid and red dashed curves of Fig. 12.

Three different cases of time-domain analyses were performed in this study with results depicted by Fig. 13. Accordingly, the input and output responses of the BP-NGD IC are plotted in Fig. 13(a), Fig. 13(b), and Fig. 13(c) with time durations $t_{\max}$ fixed to 80 ns, 150 ns, and 85 ns, respectively.

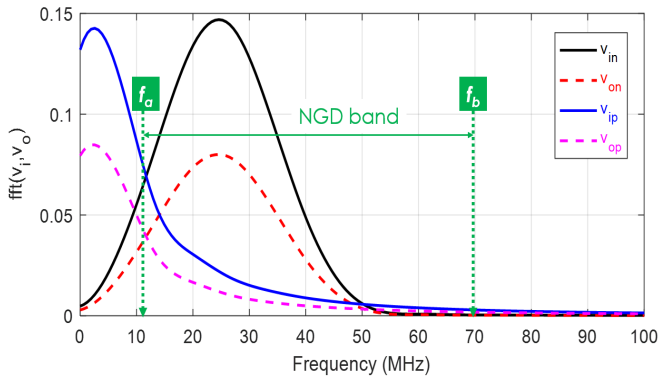

FIGURE 12. Spectra of baseband (v_{ip}, v_{op}) and modulated (v_{in}, v_{on}) signals considered for the BP-NGD IC analyses in the time-domain.

Fig. 13(a) represents (v_{in}, v_{on}) the cases of f_0-modulated signal response. We can see in Fig. 13(a) and Fig. 13(c) that the outputs plotted in dashed red curve are in time-advance of about -1 ns compared to the inputs plotted in black solid curves, respectively. However, we can understand with pair (v_{ip}, v_{op}) from the dashed pink curves of Fig. 13(b) and Fig. 13(c) that the outputs are delayed after the inputs plotted in solid blue curves.

The interaction between the input signals and 130-nm CMOS IC can be understood with the spectral representations shown in Fig. 12. We can see clearly that the time advance effect appears when the fast Fourier transforms (FFTs) (displayed by the spectra of Fig. 12) of the input transient signals generating the results plotted in Fig. 13 belong to the NGD in- and out-frequency bands. Substantially, the time-advance apparition for modulated signals explains the effectiveness of the BP-NGD function as the input signal spectrum power belongs to the NGD frequency band $(f_a \leq f \leq f_b)$ as illustrated by Fig. 12. We can see that the outputs in positive delay regions are associated with the spectra corresponding to baseband signals, with the power mainly located in the frequency band $f \leq f_a$.

6. CONCLUSION

An innovative design of miniature BP-NGD type IC using inductorless passive topology is investigated. The BP-NGD function is defined by its specifications based on the S-parameter model. The lumped topology of the RC-passive cell is described. The design methodology of miniature IC, taking into account DRC, LVS, and PLS with respect to design rules in CMOS technology, is established. The feasibility of the design method is verified with a POC designed with Cadence® Virtuoso®. The S-parameter simulations confirm the BP-NGD behavior with center frequency around 21.9 MHz with low-attenuation loss and good matching. The robustness of the BP-NGD CMOS IC is analyzed by the MC simulations with $+/-5\%$ standard deviation by considering 1000 samples.

In the future, due to the potential integration and miniaturization, the developed study opens huge possibility of NGD function potential applications by means of radio frequency integrated circuit (RFIC) and monolithic microwave integrated circuit (MMIC) engineering to improve the performance of transceiver electronic and communication system.

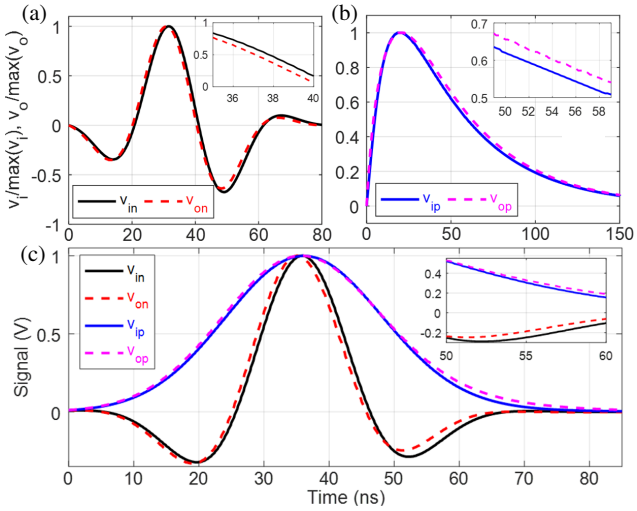

FIGURE 13. Input and output transient signals of the BP-NGD CMOS IC POC with (a) case 1 plotting modulated signals (v_{in}, v_{on}), (b) case 2 plotting baseband signals (v_{ip}, v_{op}) and (c) case 3 plotting another both (v_{in}, v_{on}) and (v_{ip}, v_{op}).

ACKNOWLEDGEMENT

This work was supported in part by the NSFC under Grant 62371241 and Grant 62350610268, and in part by Beijing Natural Science Foundation under Grant L233002 and Grant SC#202009030007.

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