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High-Efficiency Dual-Band Rectifier Using Coupled-Line Matching for RF Energy Harvesting Applications

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ABSTRACT: This paper presents a compact dual-band RF energy harvesting rectifier designed for operation at 2.45 GHz and 5.2 GHz Industrial, Scientific, and Medical (ISM) bands. The rectifier employs a voltage-doubler topology integrated with a dual-band impedance matching network (MN) composed of a coupled-line section and a microstrip transmission line. The analytical design of the MN is established using the $ABCD$-matrix formulation to determine the initial modal impedances and electrical lengths, which are subsequently refined through full-wave electromagnetic optimization in ADS. The proposed approach achieves accurate dual-frequency impedance transformation using only two matching segments, significantly simplifying the structure compared with conventional multi-section designs. The prototype, fabricated on a low-cost FR-4 substrate, occupies a compact area of $34 \times 25\,\text{mm}^2$. Measurements show high power conversion efficiencies of 75% and 55% at 2.45 GHz and 5.2 GHz, respectively, under a 0 dBm input power and a 1 kΩ load, in close agreement with simulations. The results confirm that the proposed design provides an effective and low-cost solution for ambient RF energy harvesting and low-power IoT applications.

1. INTRODUCTION

The rapid growth of wireless communication technologies and the increasing demand for energy-efficient devices have driven significant research into energy harvesting (EH) and wireless power transfer (WPT) systems. These technologies provide sustainable solutions for powering low-power electronics such as wireless sensors, medical implants, and Internet of Things (IoT) nodes [1]. Among the various available energy sources, ambient radio frequency (RF) signals are particularly attractive due to their ubiquity and stability. In such systems, antennas capture the ambient RF energy, while rectifier circuits convert it into usable DC power [2–8].

Dual-band rectifiers have attracted considerable attention because they can simultaneously harvest energy from multiple frequency bands, thereby increasing the total harvested power. However, their design remains challenging, especially in achieving efficient impedance matching at more than one frequency. Proper matching is essential to minimizinh reflection losses (S_{11}) and maximizing power conversion efficiency (PCE).

Lumped-element matching networks are often employed in rectifier circuits owing to their compactness and potential for efficiency enhancement [9–11]. Nevertheless, their performance is highly sensitive to component tolerances and significantly affected by parasitic effects at microwave frequencies [12, 13]. To overcome these issues, distributed matching networks implemented using microstrip transmission lines have been proposed. Such networks exhibit lower parasitic effects, can be integrated directly onto printed circuit boards (PCBs), and are more suitable for high-frequency applications. Consequently, several multi-band rectifiers have adopted distributed structures [14–17]. For instance, Zhang et al. [16] achieved efficiencies of 44% and 35% at 2.49 and 5.14 GHz using a six-section network, while Niotaki et al. [17] reported 40% and 37% efficiencies at 0.915 and 2.45 GHz using four microstrip lines. Other reported designs employ even more complex matching networks of six to ten sections [18, 19], which increase circuit size and fabrication complexity while limiting achievable efficiency. Industrial, Scientific, and Medical (ISM) bands at 2.45 GHz and 5.2 GHz are widely used in IoT and Wi-Fi systems, making them highly suitable for RF energy harvesting applications [20]. This paper presents a compact dual-band rectifier targeting these two ISM bands. The proposed design employs a voltage-doubler topology integrated with a dual-band impedance matching network composed of a coupled line and a single microstrip transmission line. Unlike most previous designs that rely on multi-section networks and expensive substrates, the proposed rectifier achieves high measured efficiencies of 68.5% at 2.45 GHz and 52.5% at 5.2 GHz under a 0 dBm input power and a 1 kΩ load, while being implemented on low-cost FR-4. The main contributions of this work are summarized as follows:

1. A simplified dual-band impedance matching network consisting of only one coupled-line and one transmission-line section.

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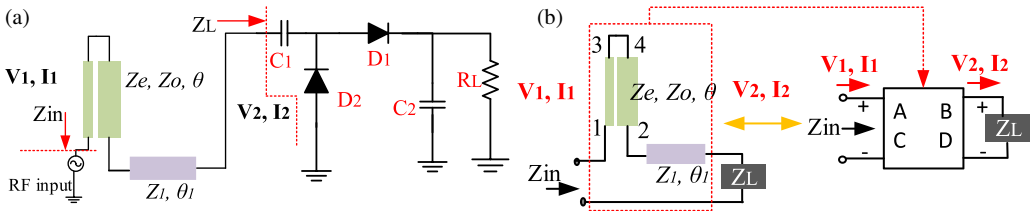

FIGURE 1. (a) Proposed dual-band rectifier. (b) Schematic diagram of the MN and its equivalent two-port model.

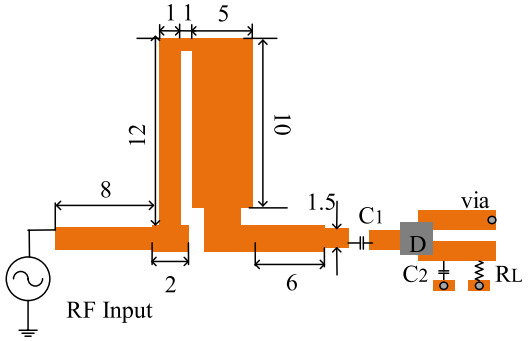

FIGURE 2. Layout of the proposed dual-band rectifier (all dimensions in mm).

2. High PCE performance on a low-cost FR-4 substrate, demonstrating efficiency comparable to designs on premium materials.
3. Experimental validation confirming a compact footprint (34×25 mm^2) and robust dual-band operation at ISM frequencies.

The remainder of this paper is organized as follows. Section 2 describes the configuration and matching principle of the proposed rectifier. Section 3 presents the analytical design and theoretical modeling of the dual-band matching network based on the $ABCD$-matrix formulation. Section 4 outlines the complete design-to-fabrication process, including the measurement setup, experimental validation, and a comparative analysis with previously reported designs to emphasize the advantages of the proposed approach. Finally, Section 5 concludes the paper by summarizing the key findings.

2. CONFIGURATION AND MATCHING PRINCIPLE

The objective of this study is to design a compact dual-band rectifier based on a voltage-doubling circuit (VDC). The rectifying core consists of two Schottky diodes, two capacitors (C_1 and C_2), and a load resistor (R_L). In this configuration, C_1 functions as a coupling and storage capacitor rather than a simple input blocking element, while C_2 acts as a smoothing capacitor to stabilize the rectified output. Diodes provide RF-to-DC conversion, and the load resistor represents the connected application, whose value strongly influences the overall efficiency of the rectifier.

The input impedance of the VDC (Z_L) was simulated at the two target frequencies of 2.45 GHz and 5.2 GHz. The circuit exhibits highly capacitive input impedances of $25.5 - \text{j}231\ \Omega$ at 2.45 GHz and $13 - \text{j}108\ \Omega$ at 5.2 GHz.

To enable efficient dual-band operation, a compact matching network (MN) was designed by cascading a coupled-line section with an additional microstrip transmission line, as illustrated in Fig. 1(a). The coupled-line section primarily compensates for the large reactive (imaginary) component of the rectifier impedance, while the microstrip line performs the real impedance transformation to $50\ \Omega$. So, the proposed MN acts as an effective impedance transformer, ensuring proper matching at both 2.45 GHz and 5.2 GHz. The matching condition for dual-frequency operation can be expressed as

$$Z_{in}(f_1) = Z_{in}(f_2) = Z_0. \tag{1}$$

3. ANALYTICAL DESIGN OF THE MATCHING NETWORK

The proposed dual-band matching network (MN) is designed based on the analytical model presented in [21], in which a coupled-line section is cascaded with a single microstrip transmission line to realize dual-frequency impedance transformation. In [21], the two coupled lines have identical widths and electrical lengths, forming a symmetric configuration whose even- and odd-mode impedances (Z_e, Z_o) can be derived analytically using the $ABCD$-matrix representation.

In contrast, the present work introduces an asymmetric coupled-line structure, composed of two connected microstrip lines with different widths but equal electrical lengths. This modification alters the even- and odd-mode impedances, providing an additional degree of freedom for impedance control at both target frequencies (2.45 and 5.2 GHz) while maintaining a compact and continuous layout. The equivalent schematic of the proposed MN is shown in Fig. 1(b), and its $ABCD$-matrix representation can be expressed as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = M_{CL} M_{TL} \tag{2}$$

where M_{CL} and M_{TL} denote the $ABCD$ matrices of the coupled-line and transmission-line sections, respectively. The voltage and current at the two ports are related as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{3}$$

The elements of M_{CL} and M_{TL} are given by:

$$A_{CL} = D_{CL} = \frac{Z_e - Z_o \tan^2\theta}{Z_e + Z_o \tan^2\theta} \tag{4}$$

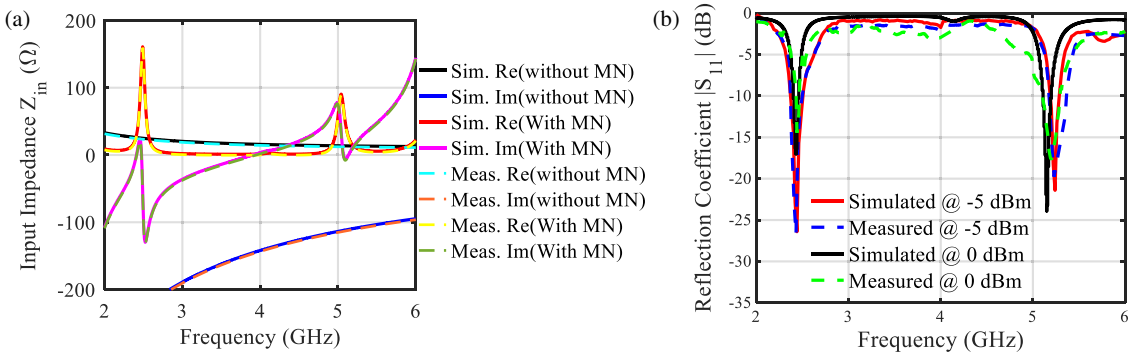

FIGURE 3. Simulated and measured (a) input impedance at 0 dBm, (b) S_{11} of the rectifier at $R_L = 1\,\text{k}\Omega$.

$$B_{CL} = \frac{2Z_e Z_o j \tan\theta}{Z_e + Z_o \tan^2\theta} \tag{5}$$

$$C_{CL} = \frac{2j \tan\theta}{Z_e + Z_o \tan^2} \tag{6}$$

$$M_{TL} = \begin{bmatrix} \cos\theta_1 & jZ_1 \sin\theta_1 \\ j \sin\theta_1 / Z_1 & \cos\theta_1 \end{bmatrix} \tag{7}$$

where Z_e and Z_o are the even- and odd-mode impedances of the coupled-line section; θ is its electrical lengths; Z_1 is the characteristic impedance of the additional microstrip line; and θ_1 is its electrical length.

The input impedance seen from the source side can then be written as

$$Z_{in} = \frac{AZ_L + B}{CZ_L + D} \tag{8}$$

where Z_L represents the input impedance of the voltage-doubler rectifier (VDC) when it is disconnected from the matching network, as defined in Fig. 1(a).

The design process begins with the analytical calculation of Z_e, Z_o, and Z_1 based on the $ABCD$-matrix model following the approach in [21] by Wu et al. The initial modal impedances were approximately estimated as $Z_e = 78\,\Omega$ and $Z_o = 34\,\Omega$ at 2.45 GHz, and $Z_e = 74\,\Omega$ and $Z_o = 31\,\Omega$ at 5.20 GHz. The connecting transmission line exhibited a characteristic impedance around $Z_1 = 52\,\Omega$ and $50\,\Omega$ at the two frequencies, respectively. These analytically obtained parameters were used as initial values for electromagnetic (EM) optimization in advanced design system (ADS), where the physical dimensions of both the coupled-line and transmission-line sections were fine-tuned to achieve optimal impedance matching and improved PCE across the two frequency bands.

4. IMPLEMENTATION AND EVALUATION

4.1. Fabrication

The proposed dual-band rectifier employs an SMS7630-006LF Schottky diode, which was modeled in ADS using the manufacturer's SPICE parameters [22] to accurately capture its nonlinear characteristics in simulations. The microstrip layout of the rectifier is shown in Fig. 2, where all dimensions are in millimeters. The circuit was fabricated on a cost-effective FR-4 substrate with a relative dielectric constant of $\varepsilon_r = 4.3$, loss tangent $\tan\delta = 0.025$, and thickness of 0.8 mm. Although FR-4 exhibits higher dielectric losses than premium substrates such as Rogers, it was chosen to demonstrate a practical and low-cost design approach suitable for real-world energy harvesting applications. The relatively high loss tangent of FR-4 can degrade efficiency by attenuating RF signals and lowering the quality factor of transmission lines and matching networks. Nevertheless, through careful impedance matching and compact layout optimization that minimizes transmission line lengths and parasitic effects, the proposed rectifier achieves high power conversion efficiency while maintaining a compact footprint of $34 \times 25\,\text{mm}^2$. The impact of the proposed MN was investigated by comparing the rectifier's input impedance with and without the MN. The (without MN) case represents the standalone voltage doubler circuit, whereas the (with MN) case includes the coupled-line-based matching network.

As shown in Fig. 3(a), both simulated and measured input impedances at 0 dBm indicate that the MN effectively transforms the highly capacitive impedance of the bare rectifier toward the 50-Ω source impedance at both target frequencies. Correspondingly, Fig. 3(b) illustrates the simulated and measured reflection coefficients (S_{11}) of the rectifier with $R_L = 1\,\text{k}\Omega$, confirming good dual-band impedance matching. The voltage doubler circuit components were $C_1 = 100\,\text{pF}$, $C_2 = 100\,\text{pF}$, and $R_L = 1\,\text{k}\Omega$.

4.2. Rectification Results

The simulated frequency-dependent power conversion efficiency (PCE) of the proposed rectifier at various load resistances is shown in Fig. 4(a) for a fixed input power of 0 dBm. This analysis was conducted to determine the optimal load value for maximum RF-to-DC conversion. Distinct efficiency peaks are observed near 2.45 GHz and 5.2 GHz, confirming effective dual-band operation. Among the evaluated load values (0.8 Ω, 0.9 Ω, 1 Ω, and 1.5 Ω), the highest PCE was achieved at 0.8–1 Ω, indicating that proper load selection is crucial for maximizing conversion efficiency. Consequently, the rectifier was fabricated with a 1 kΩ load resistor. The fabricated prototype was experimentally characterized using an RF signal generator as the input source. The input power was swept from −10 dBm to 15 dBm at the operating frequencies of 2.45 GHz and 5.2 GHz. The rectifier was connected directly to the gener-

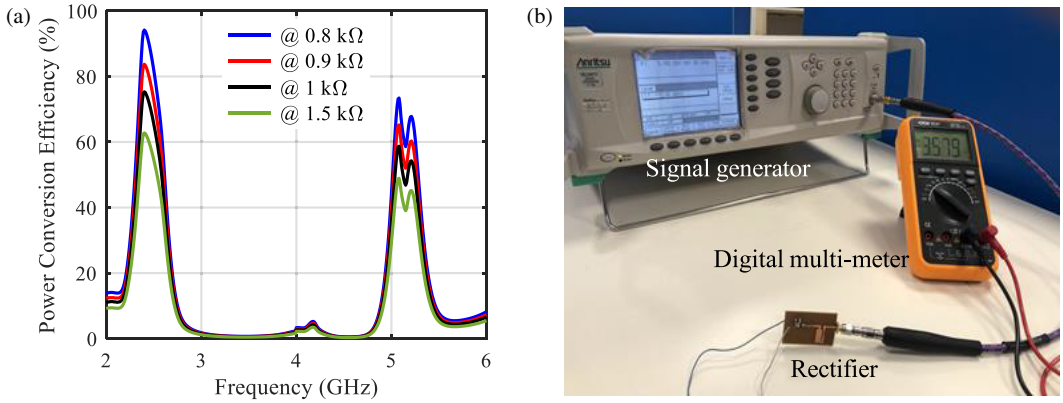

FIGURE 4. (a) PCE versus frequency @ different loads @ dBm. (b) Photograph of the measurement setup.

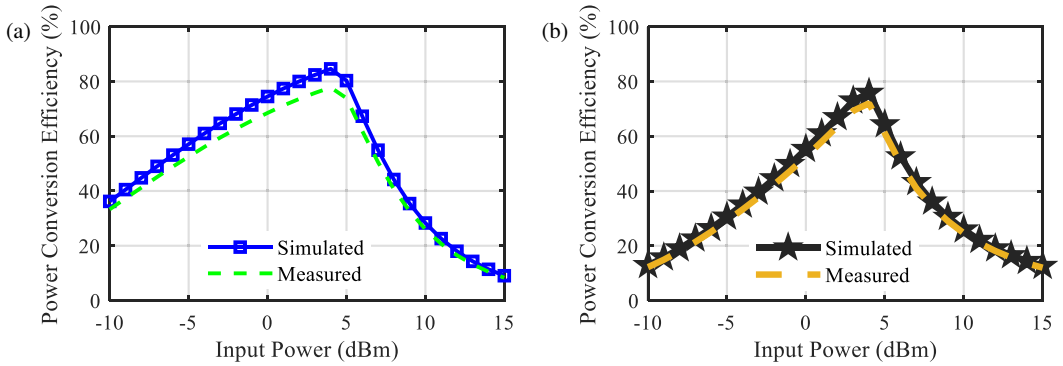

FIGURE 5. Measured and simulated PCEs with $R_L = 1\,\text{k}\Omega$, (a) @2.45 GHz, (b) @5.2 GHz.

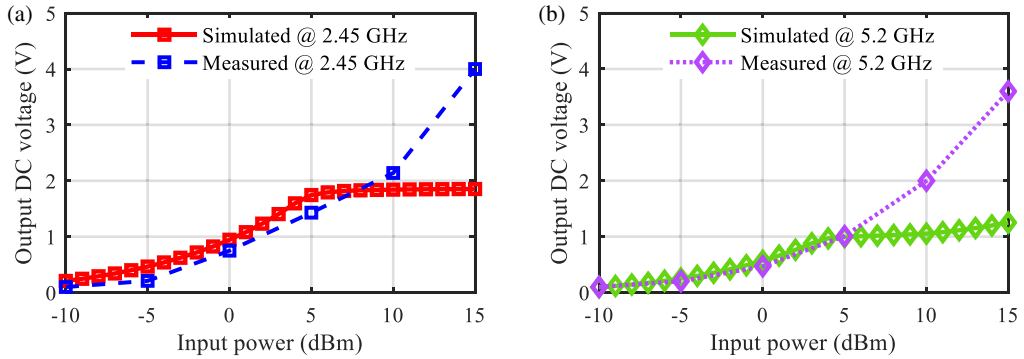

FIGURE 6. Measured and simulated DC voltages of the rectifier, (a) @2.45 GHz, (b) @5.2 GHz with $R_L = 1\,\text{k}\Omega$.

ator through an SMA cable without any external matching network, and the DC output voltage across the load was measured using a digital multimeter. The measurement setup is shown in Fig. 4(b).

The measured PCE as a function of input power is presented in Fig. 5(a) and Fig. 5(b) for 2.45 GHz and 5.2 GHz, respectively, with $R_L = 1\,\text{k}\Omega$. At 2.45 GHz, the rectifier achieves peak efficiencies of 83.7% (simulation) and 75% (measurement) at an input power of 4 dBm. Even at 0 dBm, the measured efficiency remains high at 68.5%. At 5.2 GHz, the rectifier reaches maximum efficiencies of 75.5% (simulated) and 73% (measured) at 4 dBm, while at 0 dBm, the respective efficiencies are 55% and 52.5%. These results confirm the strong agreement between simulation and measurement, and the robustness of the proposed rectifier across both ISM bands.

The measured and simulated output DC voltages versus input power are shown in Fig. 6(a) and Fig. 6(b) for 2.45 and 5.2 GHz, respectively. At 0 dBm, the measured output voltages are 0.5 V and 0.4 V, compared to simulated values of 1.0 V and 0.5 V, respectively. The lower measured voltages, especially at low input powers, are mainly attributed to practical losses not fully captured in simulation. Connector and cable losses introduce additional attenuation before the rectifier, while fabrication tolerances can slightly alter microstrip dimensions and impedance characteristics. Furthermore, the diode model used in simulation idealizes nonlinear and parasitic effects, leading

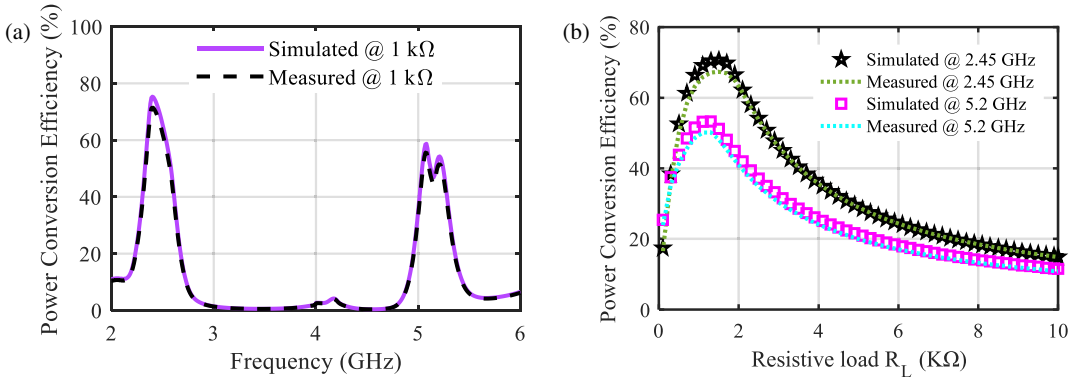

FIGURE 7. PCE of the rectifier (a) versus frequency @0 dBm and 1 kΩ, (b) versus R_L at 0 dBm.

TABLE 1. Comparison of the proposed rectifier with state-of-the-art designs.

Ref.	Diode	Freq. (GHz)	PCE@0 dBm	RL (kΩ)	Size (mm^2)	No. of segments	Substrate	Year
[14]*	BAT1503W	0.9 & 2.36	61% & 56%	0.68	35 × 34	5	Taconic TLY-5	2024
[15]*	BAT1503W	0.91 & 2.45	55% & 53%	0.6	52 × 46	8	Taconic TLY-5	2023
[16]*	BAT1503W	2.49 & 5.14	44% & 35%	1	31 × 25	6	Rogers RO4003C	2024
[17]*	SMS7630	0.915 & 2.45	70% & 58%	1	N/A	4	Arlon 25N	2014
[18]	HSMS-2862	1.8 & 2.4	48.8% & 34.8%	1.5	154 × 65	10	Arlon AD255	2018
[19]*	HSMS-2822	0.915 & 2.45	30% & < 10%	0.68	38.9 × 28.9	6	Taconic TLC32	2025
[23]	HSMS-2860	2.45 & 5.8	58% & 35%	1.05	35 × 26	6	Roger RO4003	2013
[24]*,a	HSMS-2862	0.915& 2.45	58% & 40%	1.5	86 × 72	3	Arlon AD 255	2020
[25]	HSMS2860	2.4 & 5.8	51.2% & 56.7%	1.2	48 × 22	6	ROG4003C	2024
This work	SMS7630	2.45 & 5.2	75% & 55%	1	34 × 25	2	FR4	2025

* PCE values are estimated from the original publications.

[a] Rectifier-I in [24].

to optimistic results. Nevertheless, these discrepancies do not significantly affect the measured PCE in Fig. 7, as efficiency is defined by the ratio of DC output power to RF input power.

The measured output voltage exhibits delayed saturation compared to simulation due to the diode's gradual nonlinear behavior, including junction capacitance, series resistance, and thermal effects, which are not fully captured in the simplified simulation model. This leads the real device to maintain voltage growth over a wider input power range. Such behavior, also observed in recent rectifier studies, is beneficial for ambient RF energy harvesting applications, as it enables stable operation under varying input power conditions.

4.3. Comparison and Discussion

Table 1 presents a detailed comparison between the proposed dual-band rectifier and several recently reported designs from 2013 to 2025. The proposed rectifier demonstrates superior overall performance in terms of efficiency, compactness, and structural simplicity. At an input power of 0 dBm and a load resistance of 1 kΩ, it achieves power conversion efficiencies (PCEs) of 75% at 2.45 GHz and 55% at 5.2 GHz, outperforming most recent designs such as [14–16], which report efficiencies below 61%, and [19], which achieves less than 30% at the lower frequency band. Compared with more recent high-efficiency designs from 2024 to 2025 [14, 16, 19, 25], the proposed rectifier maintains comparable or higher PCE while featuring a significantly simpler configuration consisting of only two matching segments — a coupled-line section and a microstrip line. In contrast, most competing designs rely on five to ten cascaded sections to achieve dual-band operation, increasing complexity and footprint. The proposed rectifier also offers a compact physical size of 34 × 25 mm^2, which is considerably smaller than many counterparts such as [18] and [24], whose dimensions exceed 80 × 60 mm^2. Despite being implemented on a low-cost FR-4 substrate, the proposed design achieves performance levels comparable to or better than those using premium materials (e.g., Rogers or Taconic). The combination of high efficiency, compact size, and fabrication simplicity makes this rectifier particularly attractive for ambient RF energy harvesting and low-power Internet of Things (IoT) applications.

5. CONCLUSION

A compact dual-band rectifier for RF energy harvesting at 2.45 GHz and 5.2 GHz has been designed, fabricated, and experimentally validated. The rectifier integrates a voltage-doubler circuit with a simple two-section impedance matching

network consisting of a coupled-line section and a microstrip transmission line. The analytical design, based on $ABCD$-matrix modeling, enabled accurate estimation of the modal impedances and electrical lengths, which were further optimized using ADS to achieve dual-frequency impedance matching. Implemented on a low-cost FR-4 substrate, the proposed rectifier demonstrates measured PCEs of 75% and 55% at the two frequency bands, respectively, while maintaining a compact footprint of $34 \times 25\,\text{mm}^2$. Compared with state-of-the-art designs, it offers competitive or higher efficiency with a simpler and more economical structure. The proposed approach thus provides a practical, low-cost, and efficient solution for powering low-energy wireless and IoT systems from ambient RF sources. In future work, we will focus on designing a suitable antenna to integrate with the rectifier and realize a complete RF energy harvesting system.

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