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A 50 pA-Input-Bias-Current 134 dB-Open-Loop-Gain Operational Amplifier with a New CMFB and Base Current Compensation Circuit

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ABSTRACT: In the design of a precision operational amplifier (OPA), cancellation of the input bias current is a challenging issue, which is primarily limited by the current mirror mismatch and the low β value of the PNP transistors. This article proposes a new base current compensation design, which enables zero input-bias-current theoretically. The input stage of the circuit is an active load differential pair with a new common-mode feedback (CMFB) circuit based on the current reuse technique, which can provide a stable common-mode voltage for the amplifier without additional power consumption and area occupation. The proposed OPA is designed in a bipolar process with a core area of 2.85 mm $\times$ 1.5 mm. Simulation results show that this OPA achieves a 134_dB open-loop-gain, 50 pA input-bias-current @25°C, and a low supply current of 0.9 mA, which suggests a concise architecture of the OPA for low offset, low noise, low input bias current, and high gain.

1. INTRODUCTION

Precision operational amplifier (OPA) has the characteristics of low input offset voltage, low temperature drift, and low noise, which make it capable of acquiring weak signals and then complete amplification. It is widely used in sensors, instrumentation amplifiers, precision filters, etc. [1]. Its performance has a direct impact on the overall system and can even become a bottleneck that hinders significant advancements [2]. In addition, it is usually fabricated in a bipolar process with the advantages of designing high-performance operational amplifiers, because the bipolar process can achieve greater transconductance and lower noise than the standard CMOS process [3]. In addition, the bipolar process has the advantages of high gain, wide bandwidth, and low offset. However,the bipolar process may reduce the input impedance of the OPA, resulting in an increase of the input bias current [4].

To address these shortcomings, a base current compensation circuit has been proposed to decrease the input bias current. However, the resulting residual current is typically one-fifth to one-twentieth of the original uncompensated base current [5]. Furthermore, a modified base current compensation structure that mainly consists of a resistor-adjustable current mirror and an improved Wilson current mirror has been proposed. However, the accuracy is insensitive to the value of β (the ratio of the collector current to base current) [5, 6]. In particular, cancellation of the input bias current is challenging, primarily limited by the current mirror mismatch and the low β value of the PNP transistors. Thus, this study proposes an innovative input bias current compensation structure, which can theoretically reduce the bias current to zero.

For a higher gain and stable common voltage of the output [7], a common-mode feedback (CMFB) loop was proposed, which can also improve the common-mode rejection ratio (CMRR) [8]. However, another OPA for a CMFB loop circuit requires a large area and consumes more power [9]. Thus, a new (CMFB) circuit based on current reuse technology is proposed, which can provide a stable common-mode voltage for the amplifier without additional power consumption and area occupation.

Based on the above, a high-gain precision operational amplifier was designed for the bipolar process. The remainder of this paper is organized as follows. The system architecture is described in Section 2. Section 3 introduces the circuit design of the three-stage OPA with the proposed CMFB loop and base current compensation structure. Simulation results of the proposed OPA are presented in Section 4. Finally, the conclusions are presented in Section 5.

2. SYSTEM ARCHITECTURE

The system architecture of the proposed amplifier is shown in Fig. 1. It is mainly composed of a differential input stage with a

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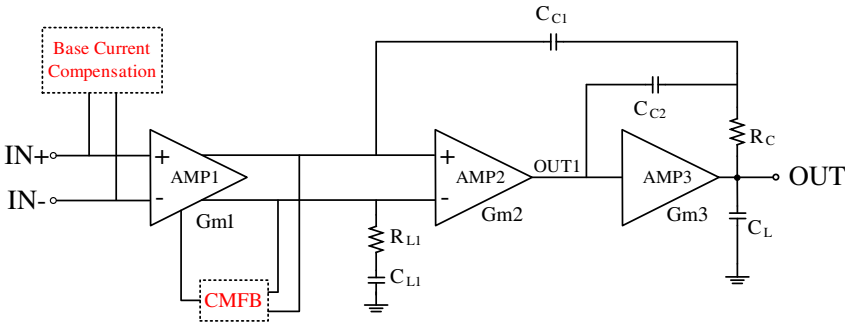

FIGURE 1. System architecture of the OPA.

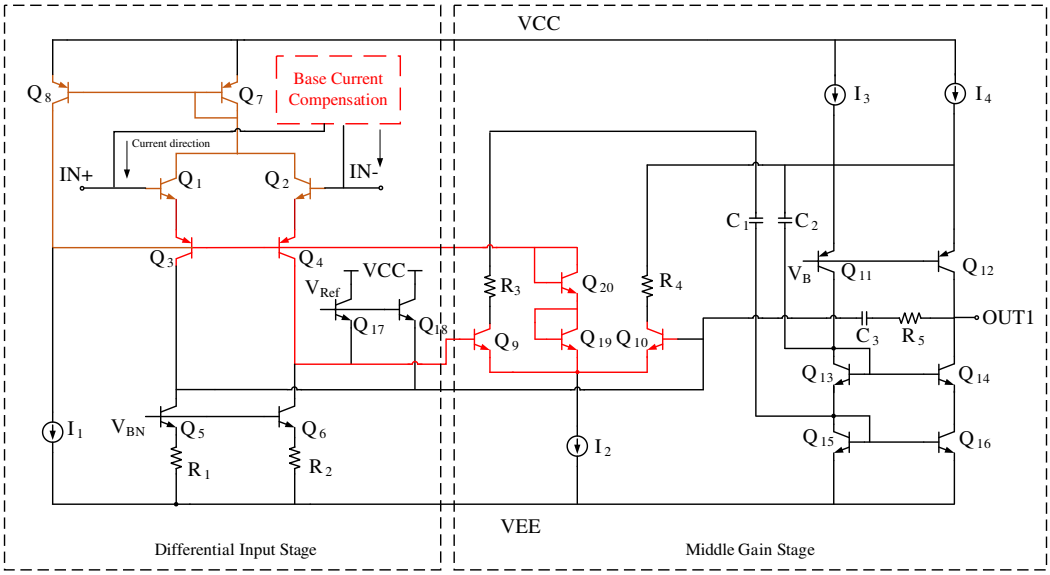

FIGURE 2. Differential input and gain stages.

CMFB loop and base current compensation structure, a middle gain stage, an output stage, and a bias. The working principle is as follows. First, the external input signal is amplified by the differential input stage. The amplified signal is converted into a current signal at the middle-gain stage, and the current signal was amplified. Finally, the current signal was converted into a voltage signal through the output stage, and amplified once again. Through this process, the OPA obtains gain from the analog input signal to the output signal. The role of the CMFB loop is to stabilize the differential output voltage of the input stage, and the base current compensation structure reduces the bias current and increases the input impedance.

The overall gain of the OPA is expressed as follows:

$$A_{v0} \approx G_{m1}G_{m2}G_{m3}R_{O1}R_{O2}R_{OL} \tag{1}$$

where G_{m1}, G_{m2}, and G_{m3} represent the transconductances of AMP1, AMP2, and AMP3, respectively. R_{O1} and R_{O2} represent the equivalent output impedances of AMP1 and AMP2, respectively, and R_{OL} represents the equivalent load impedance of AMP3.

C_{C1} and C_{C2} are Miller capacitors that compensate for the overall frequency response, and their values are designed as follows [10]:

$$C_{C1} = 4\left(\frac{G_{m1}}{G_{m3}}\right)C_L \tag{2}$$

$$C_{C2} = \frac{2}{1-\frac{G_{m2}}{G_{m3}}}\left(\frac{G_{m2}}{G_{m3}}\right)C_L \tag{3}$$

where C_L represents the output load capacitance.

3. CIRCUITS DESIGN AND IMPLEMENTATION

3.1. High Gain Differential Input and Gain Stages

The internal circuit diagrams of the input and middle-gain stages are shown in Fig. 2. The input stage is an N-type differential pair stage composed of Q_1 and Q_2, Q_3, Q_4, Q_5, Q_6, R_1, and R_2. A common loop provides a bias voltage to the base of Q_3, Q_4, Q_7, and Q_8 [5]. The working principle is as follows: when the base voltage of Q_3 increases, the collector voltage of Q_1 increases. Then, Q_7 detects the change and decreases the base voltage of Q_8. Through this negative feedback loop, the base voltage of Q_3 was decreased.

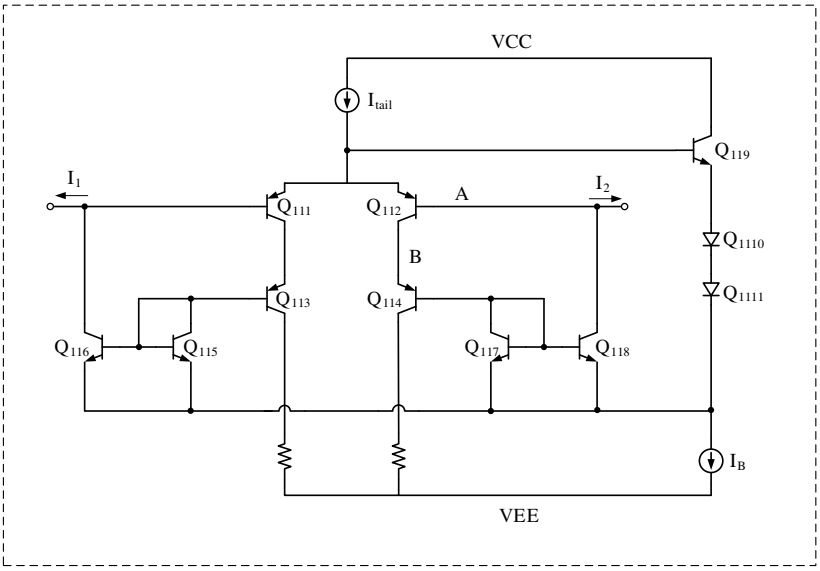

FIGURE 3. Traditional base current compensation scheme.

The middle gain stage is a folded cascode structure that converts the differential input to a single-ended output. Q_9 and Q_{10} are N-type differential input transistors of the second-stage amplifier, doubling as common-mode sampling transistors. The CM voltage is sensed by the emitter of Q_{19} and then flows through Q_{19}, Q_{20}, and Q_4. The common-mode feedback circuit proposed in this paper eliminates the need for extra amplifiers and power consumption. Subsequently, the collector voltage of the Q_4/Q_3 is biased at $V_{\text{Ref}} - 0.7$.

$r_{B9} + r_{\pi 9}$ represents the equivalent base input impedance of Q_9, while $C_{\pi 9}$ and $C_{\mu 4}$ denote the base-emitter junction capacitance of Q_9 and the base-collector junction capacitance of Q_4, respectively. $C_{\pi 9}$ and $C_{\pi 14}$ denote the base-emitter junction capacitance of Q_9 and Q_{14}. The dominant and non-dominant poles of the common-mode feedback loop are given by Eq. (9).

$$\begin{aligned} P_1 &= \frac{1}{2\pi * ((r_{B9} + r_{\pi 9})//(\frac{V_E}{I_{c4}})) * (C_{\pi 9} + C_{\mu 4})} \\ P_2 &= \frac{1}{2\pi * \frac{2}{g_{m19}} * (C_{\pi 9} + C_{\pi 19})} \end{aligned} \tag{4}$$

Typically, $\frac{2}{g_{m19}} \ll r_{b9} + r_{\pi 9}$, the common-mode feedback loop of the amplifier achieves stable operation without difficulty.

Q_{11} and Q_{12} are folded common-based transistors. Q_{13}–Q_{16} consist of a cascode current mirror. R_3, C_1, R_4, C_2 constitute the feedback compensation, and R_5 and C_3 are Miller compensations with the zero-setting resistance.

3.2. Base Current Compensation Circuit

The traditional base current compensation scheme is shown in Fig. 3. In the circuit, Q_{119}, Q_{1110}, and Q_{1111} ensure that the emitter voltage of Q_{118} (Q_{116}) is three diode voltages below that of Q_{111} (Q_{112}):

$$V_{E118} = V_{E111} - 3V_{\text{diode}} \tag{5}$$

Because the emitter voltage of V_B is two-diode voltage above that of Q_{118} (Q_{116}), and V_A is one-diode voltage lower than that of Q_{111} (Q_{112}):

$$V_B = V_{E118} + 2V_{\text{diode}} \tag{6}$$

$$V_A = V_{E111} - 1V_{\text{diode}} \tag{7}$$

then, there is:

$$V_A \approx V_B \tag{8}$$

If the β of the transistor is large, the collector current of Q_{113} (Q_{114}) is equal to that of Q_{111} (Q_{112}). Q_{115}, Q_{116}, Q_{117}, Q_{118} act as current mirrors to replicate the base current of Q_{113} (Q_{114}) and provide it to the bases of Q_{111} and Q_{112}, thereby eliminating the input current. The current error I_{mis} is expressed as:

$$I_{\text{mis}} = \frac{I_{CQ113}}{\beta_P} \bullet \frac{\beta_n}{1+\beta_n} - \frac{I_{CQ113}\beta_P}{\beta_P(1+\beta_P)} \approx I_{CQ113}\frac{1}{\beta_P(1+\beta_P)} \tag{9}$$

where I_{CQ113} is the collector current of Q_{113}, and β_p is the Common-Emitter Current Gain of Q_{111}. Thus, the elimination depends on the β value of the transistor. Because of the limited β value, the replication accuracy of the current mirror is reduced, which results in a 5% to 20% error between the compensation current and the base current of Q_{111}/Q_{112}, which makes it impossible to fully compensate for the base current.

For an ideal amplifier, the input bias current is expected to be zero. For an n-type transistor, the input bias current is I_C/β. A wider bandwidth implies a high I_C and input bias current, which is a lower input impedance and current detection accuracy. Therefore, this study proposes a high-performance base current compensation circuit to make the input bias current near zero.

As shown in Fig. 4, the proposed structure includes a bias circuit composed of R_6, R_7, R_8 and a base current compensation circuit composed of Q_{21}–Q_{24} and current source I_5. Here, Q_{24} and Q_1/Q_2, Q_{25} and Q_7 were identical. I_5 is equal to I_{C1}/I_{C2},

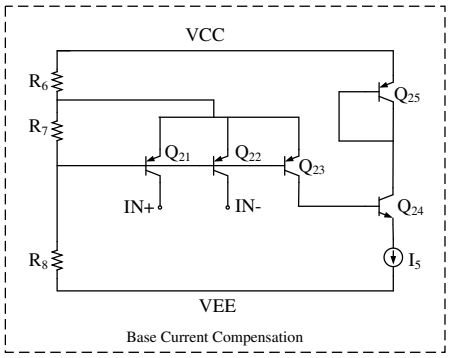

FIGURE 4. Base current compensation.

and the base current of Q_{24} is expressed as follows:

$$I_{B24} = I_{B1} = I_{B2} \tag{10}$$

where I_{C1} is the collector current of Q_1. I_{b1}, I_{b2}, and I_{B24} are the base currents of Q_1, Q_2, and Q_{24}, respectively. Q_{21}, Q_{22}, and Q_{23} are identical and simultaneously biased at the same voltage between the base and emitter. Therefore, the equation for the collector currents of Q_{21}, Q_{22}, Q_{23} is given by the Eq. (11).

$$I_{C23} = I_{C21} = I_{C22} \tag{11}$$

The collector of Q_{23} is connected to the base of Q_{24}, and the collector current of Q_{23} is given by Eq. (12).

$$I_{C23} = I_{B24} \tag{12}$$

According to Eqs. (9), (10), and (11), the following formula can be expressed:

$$I_{C21} = I_{C22} = I_{B1} = I_{B2} \tag{13}$$

According to Eqs. (13), Q_{21} and Q_{22} supply the base current needed by transistors Q_1 and Q_2, respectively. The base current is theoretically completely compensated, and the input bias current is near zero.

However, due to the dispersion of the transistor's β value during the manufacturing process, it is difficult for the base current to be zero. To evaluate the mismatch in process fabrication, the paper employed Monte Carlo simulations to assess its impact on the studied architecture in Section 4. In this study, instead of using complex current mirrors for current copying, we leveraged the relationship between transistor current and area for equivalent current compensation. Additionally, resistors R_6, R_7, and R_8 are high-precision metal-film resistors. The design also allows for later resistor trimming to ensure engineering reliability.

3.3. Push-Pull Output Stage

The internal circuit diagram of the output stage is shown in Fig. 5. The output stage is composed of a buffer, a current driver circuit, and a class-B push-pull output stage with low output impedance. The common-collector amplifier (Q_{26}, current source I_6) is used to realize the impedance transformer. The current driver circuit (Q_{30}, Q_{31}, Q_{27}, R_{10}, and R_9) provide base currents of Q_{28} and Q_{29}, respectively, and the output current is β times the base current of Q_{28} and Q_{29}.

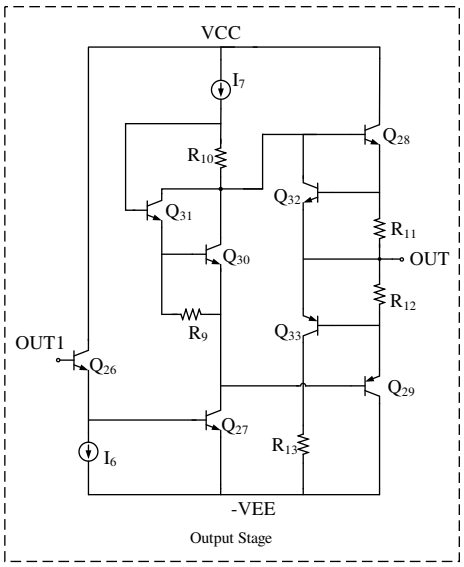

FIGURE 5. Output stage.

4. THE SIMULATION RESULTS

The proposed OPA with a new CMFB and base current compensation circuit was designed and simulated based on a complementary bipolar process. Fig. 6 shows a layout view of the proposed OPA (2.85 mm $\times$ 1.5 mm), and Fig. 7 exhibits a 134 dB open-loop-gain and 1.7 MHz bandwidth (GBW). The current consumption of the proposed OPA was 900 µA with a supply voltage of $\pm$15 V. Fig. 8 shows the CMRR of the OPA, which was approximately 84 dB. Fig. 9 shows the input noise voltage (0.1 to 10 Hz), and the input-referred integrated peak-to-peak noise voltage ($V_{P\text{-}P}$) was approximately 0.4 µ$V_{P\text{-}P}$.

As shown in Fig. 10, the offset voltage of the OPA was counted. The maximum input offset voltage was approximately 60 µV. Fig. 11 indicates the input bias current from $-45°$ to 85°, and the maximum input bias current is less than 400 pA. The simulation results shown in Fig. 11 illustrate the dramatic reduction in the input bias current achieved by the proposed base-current compensation circuit. However, the effects of device parameters mismatch under temperature variations and slight differences in V_{be} because IR drops in metal interconnects make it challenging to achieve perfect compensation for the base current of the input stage. The saturation current (Is) of a bipolar transistor increases with temperature, which causes the input bias current to also increase with temperature.

The Monte Carlo analysis reveals a mean value about 33 PA and standard deviation of 200 pA for the base compensation current, as observed from the statistical histogram in Fig. 12. This value is low enough to attest to the robust nature of the circuit. Additionally, a metal-film resistor is employed for R_6, R_7, R_8 to enhance the design's manufacturability and reliability.

Table 1 shows the performance of the proposed OPA compared to other previously published three-stage OPAs. The proposed OPA has lower current and input bias current owing to the current reuse technique of the CMFB loop circuit and the new base current compensation design.

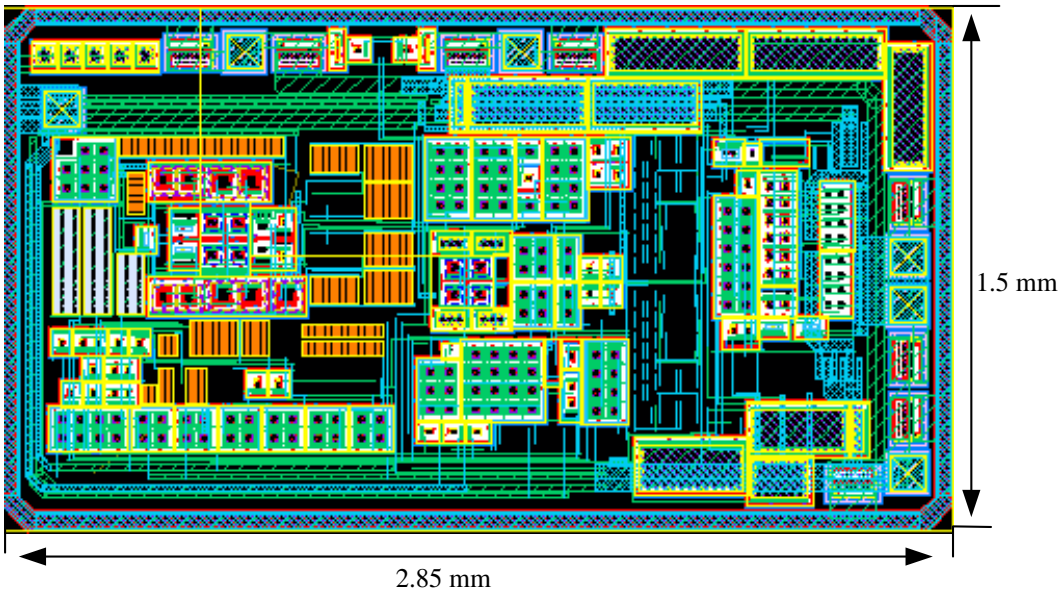

FIGURE 6. Layout view of proposed operational amplifier.

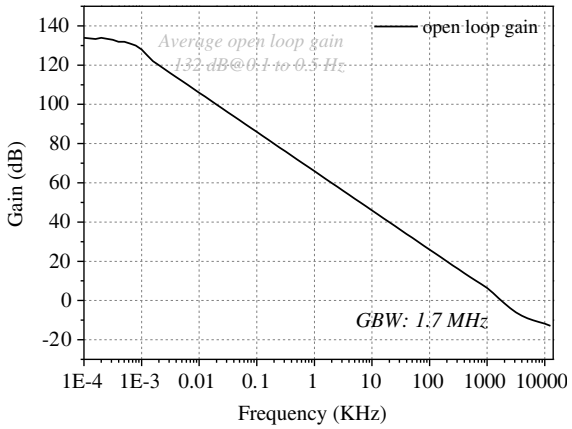

FIGURE 7. Simulation results of open loop gain and bandwidth.

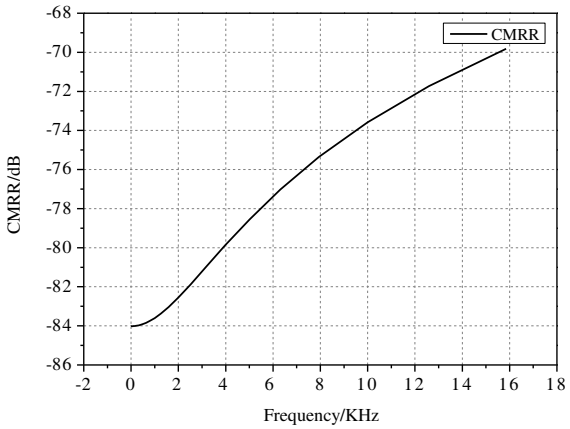

FIGURE 8. Simulation results of CMRR versus frequency.

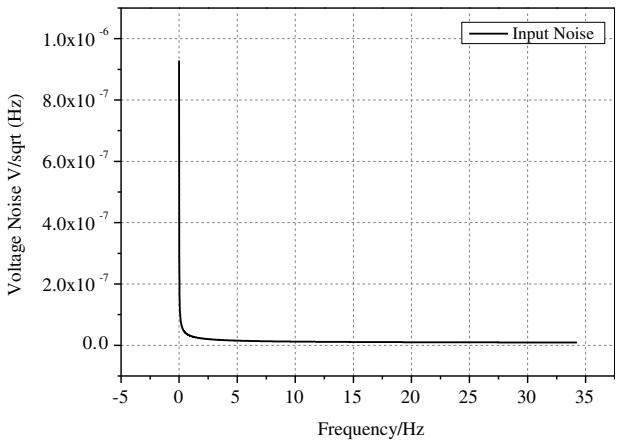

FIGURE 9. Simulation results of input noise voltage.

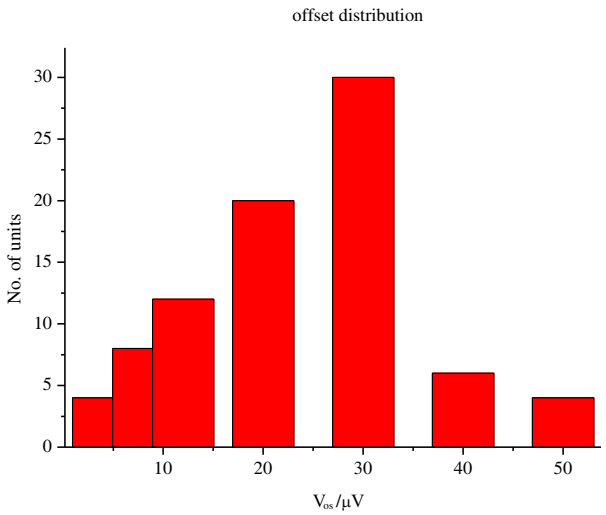

FIGURE 10. Simulation results of input offset voltage distribution.

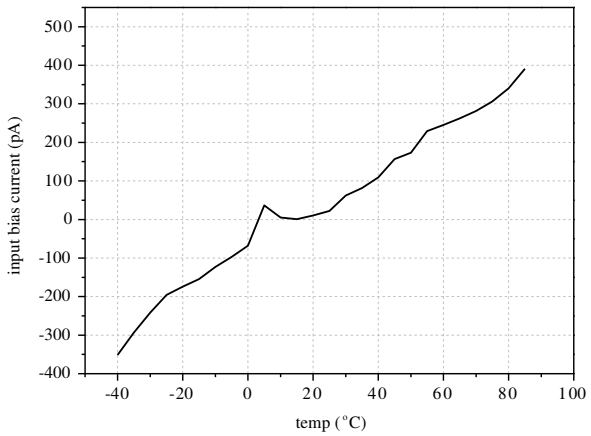

FIGURE 11. The simulation results of the input bias current.

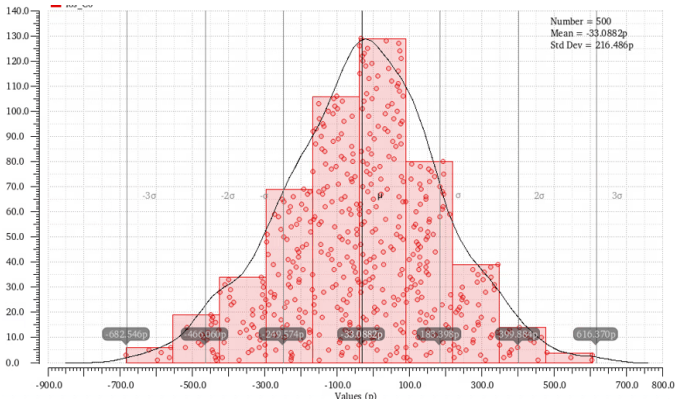

FIGURE 12. The MC result of base current.

TABLE 1. Peformance comparison with prior arts.

Parameter	This work	[12]	[11]	[13]
Process	bipolar	bipolar	bipolar	bipolar
Supply voltage (V)	15	15	15	15
GBW (MHz)	1.7	0.3	0.5	1
Supply Current (mA)	0.9	1.7	-	0.928
Input Bias Current (pA)	50	2000	2.891	700
Open Loop Gain (dB)	134	130	113.9	126
Input Offset Voltage (μV)	35	10	9.3	30
Input voltage noise @ (0.1 to 10 Hz) (μV_{P-P})	0.4	-	-	-
AREA (mm^2)	4.275	3.68	-	-

5. CONCLUSION

This paper presents a new CMFB loop and a base current compensation structure for an OPA. Compared with traditional architectures, the CMFB loop based on current reuse technology provides a stable common-voltage with a lower power (0.9 mA). The new base-current compensation structure can effectively reduce the input bias current. Meanwhile, it provides a high open-loop gain (134 dB), low input offset voltage (35 μV) and input-referred integrated peak to peak noise voltage (0.4 μV_{P-P}). Our design suggests a concise OPA architecture for a low offset, low noise, low input bias current, and high gain.

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