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A Cross-Connected T-Type Asymmetrical Multilevel Inverter with Reduce Components Count for Renewable Energy Applications

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ABSTRACT: This study offers a reduced device count (RDC) asymmetrical cross-connected seventeen-level T-type (CT-type) inverter. The proposed approach contains eight power switches, four self-voltage balancing capacitors, and two direct current (DC) sources. The recommended architecture reduces the necessity to generate negative half-cycle for an H-bridge, hence minimizing the voltage stress across the switches. The capacitor and DC sources are cascaded with the switches to produce the desired number of levels. Because of its substantial autonomy and high voltage balancing capability, this design is particularly beneficial to the integration of renewable energy sources into the grid. Pulse width modulation based on the level-shifted approach provides gate driver signals for the inverter circuit. A comparative analysis is undertaken to validate the efficacy of the suggested topology, which is differentiated from previously published topologies based on the number of DC sources, capacitor count, switches, drivers, and total standing voltage. Finally, the viability of the proposed topology is investigated by the simulated results and is further verified by a laboratory prototype. The total harmonic distortion (THD) of the voltage and current is obtained as 7.2% and 1.3%, respectively.

1. INTRODUCTION

Multilevel Inverters (MLIs) have played a leading role in various applications for high and medium voltage/power ratings. The MLIs usage in large areas is dominated by power electronics devices, such as electric vehicles, wind turbines, active power filters, grid-connected photo-voltaic (PV) systems, induction motor control, because of their ability to synthesize high-voltage outputs [1–5]. MLIs can generate various output voltage levels by incorporating multiple capacitors, power semiconductor switches, DC supplies, and diodes. Technically, MLIs are sound in delivering high efficiency, modularity, low THD, high voltage levels, etc. MLIs are broadly classified into three types: Neutral Point Clamped (NPC), Cascaded H-bridge (CHB), and Flying Capacitor (FC). CHB has gained more interest among researchers in these technologies as it overcomes the drawback of the other two, i.e., high switching losses, unbalanced DC voltage, and the use of more capacitors. Some recently developed and traditional MLI topologies presented in [6, 7] have been briefly reviewed for this work.

Multiple DC source-based CHBs are more appealing than single DC MLIs as of their higher reliability and modularity. Moreover, asymmetric CHB has less complex control than symmetric configurations and significantly increases voltage levels with reduced device count [8, 9]. On the other hand, the count of isolated DC voltage sources required in CHB is significantly higher. Previously, MLIs were limited by needing more DC sources and semiconductor switches. Over the last few years, extensive research has been conducted on improving MLI configuration in every feasible way. In [10–12], MLIs with switched-DC, switched-diode, and switched-capacitor configurations have been proposed. In [13], asymmetric switched-DC MLI has fewer components than traditional circuitry. The proposed topologies in [14] and [15] are cost-effective and perform better in the switched DC source. Even with a reduced device count, these configurations can provide both negative and positive voltage polarity. Besides that, significantly higher voltage levels can be obtained by connecting multiple fundamental units in series. In the presence of an integrated H-bridge, optimized structures in [16, 17] revealed that 15 levels could be generated using 16 interrupter numbers and 7 DC sources in the basic unit. Voltage levels using different DC sources can be generated by having lower switching stress by modifying the same. Refs. [18–20] presented and validated the symmetrical and asymmetrical topologies using various pulse width modulation techniques (PWM). Refs. [21–23] investigated switched DC-based topologies that can replace traditional MLIs. Two switches connected by a DC link to generate the required voltage level are proposed in [24]. A negative voltage level was created by incorporating an H-bridge into the initial design. This MLI modification was improved in [25], which added two capacitors to get more levels out of each module.

Conventional MLIs can be combined to produce multiple voltage levels in a hybrid form. Some hybrid topologies proposed in [26] are classified as symmetrical MLIs. Because of the unequal DC input voltage, symmetric MLIs generate high voltage levels with reduced device count (RDC). An unconven-

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tional asymmetrical topology is presented in [27] by utilizing power switches to demonstrate higher voltage levels, reducing stress from semiconductor switches. Also, a modified H-bridge topology proposed in [27] has unequal voltage DC supplies. Therefore, different bridges in symmetrical MLIs operate at different voltages. Consequently, switches associated with the high-voltage bridge must be capable of withstanding high voltage. However, the primary design objective of MLIs may be compromised because this method uses low-rating switches for high-power applications, even though it can significantly increase voltage levels. This disadvantage affects asymmetrical MLIs that use the voltage balancing method. Furthermore, the asymmetrical MLIs proposed in [26, 27] are composed of self-balancing bridges with equal DC-link voltages primarily designed in a symmetrical configuration. So, no self-balancing circuit is required, making inverter control simpler.

The proposed MLI is meant to boost the output voltage level while assuring the smart setup of semiconductor switches. The economical design also ensures that the number of power devices is minimal. This paper introduces asymmetrical cross-connected T-type (CT) MLI configurations. In a symmetrical configuration, there are two DC voltage supplies and four capacitors of the same rating, allowing it to produce four negatives, four positives, and one zero for nine different voltage levels. DC voltage sources in CT-type modules have followed the ratio of 1:3 for asymmetric configuration. As a result, the CT-type module can produce 17 (eight negatives, eight positives, and zero) distinct voltage levels. CT-type modules are included in the suggested asymmetric topology so as to produce the voltage levels of the negative half without the additional assistance of a CHB. Only 2 DC sources, 4 capacitors, and 8 switches were used.

This paper has the following structure. Section 2 discusses the circuit and the working of the proposed CT-Type-MLI. In addition, this section also provides asymmetric configuration and modes of operation, as well as module extension with output voltage level generation. Section 3 presents the modulation and control techniques followed by the simulation results for the proposed CT-Type MLI. The complete test rig and laboratory results are discussed in Section 4. Section 5 provides a full discussion of the power loss and efficiency of the proposed MLI, and Section 6 presents a detailed comparison of the recent topologies with the proposed CT-Type topology. The paper's conclusion is finally found in Section 7.

2. GENERALISED TOPOLOGY OF THE PROPOSED MLI

2.1. Circuit Configuration and Its Working

Figure 1 illustrates a schematic diagram of a basic CT-type multilevel inverter. It consists of 1 DC source, 2 capacitors, 2 unidirectional switches, and 1 bidirectional switch. The DC supply's bidirectional switches prevent short circuit currents by facilitating blockage of both current polarities. Moreover, using the proposed MLI DC-Link capacitors inherently achieves self-voltage balance. This module has generated three-level output voltage.

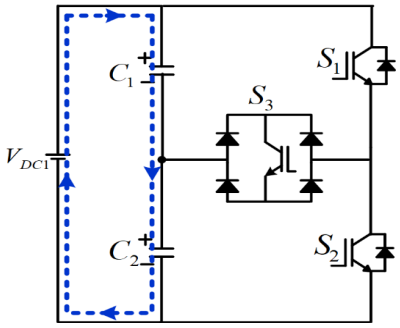


FIGURE 1. Basic cell of single-phase CT-type multilevel inverter.

Figure 2 illustrates the generalized structure of the proposed asymmetric single-phase CT-Type MLI module. A pair of power switches connect the two fundamental modules, inductance (L) and resistance (R). The L module and R module are connected by unidirectional switches S_1 and S_2, and vice versa. Both modules are connected to the load (L and R). This arrangement can produce multiple voltage levels despite having a reduced power device count. Higher voltage levels are expected to significantly lower THD and low switching frequency.

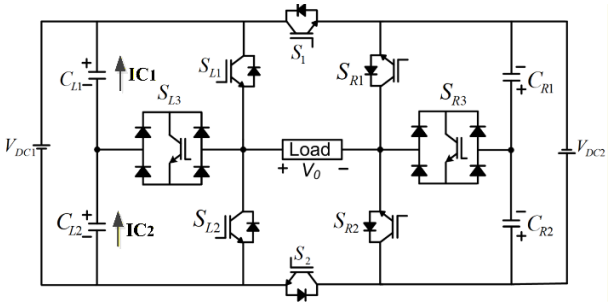
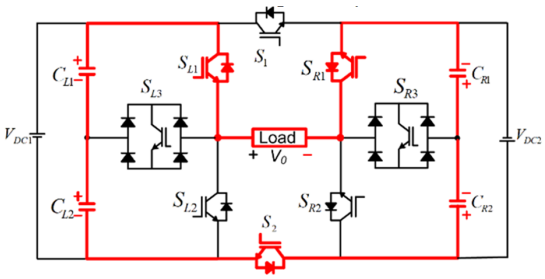


FIGURE 2. Generalized single-phase CT-type MLI module.

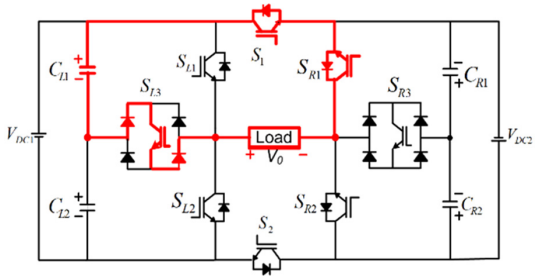
2.2. Analytical Analysis of Capacitor Values

The capacitor starts charging and discharging as a connected series with the load and in parallel across the voltage source respectively [7]. In the proposed CT-type MLI, the capacitor's charging-discharging significantly impacts the levels of the output voltage. Therefore, it is critical to identify the appropriate value of the capacitor. The capacitance value is determined by the operating frequency and the load current. The capacitor's largest voltage ripple occurs during the discharging phase, as described in [1]. Consequently, the capacitance value is calculated using the worst case of the capacitor's discharge duration. The voltage ripple must be within a specific range to be considered acceptable. When the ripple voltage is kept to a minimum, it reduces losses, thereby improving the efficiency of the proposed topology. In Fig. 2, it can be seen that the DC input voltage source is connected in series with both capacitors. As a result, the identical current flows through them during charging so that the same charge accumulates on them. Therefore,

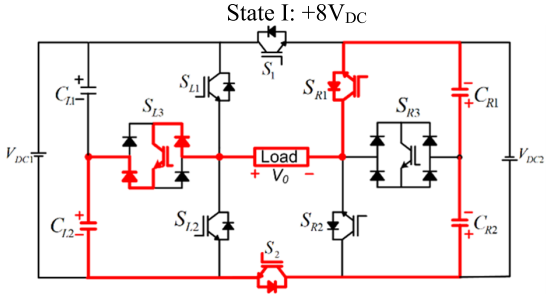
$$I_{C1} = I_{C2} \Rightarrow Q_{C1} = Q_{C2} \Rightarrow C_1 \cdot V_{C1} = C_2 V_{C2} \quad (1)$$



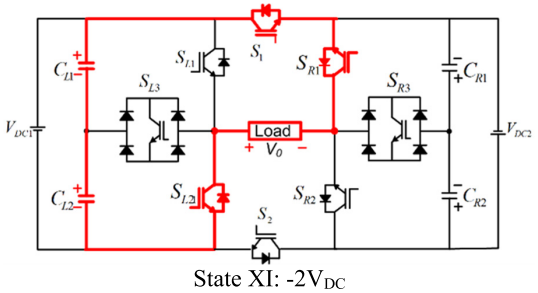
State I: $+8V_{DC}$



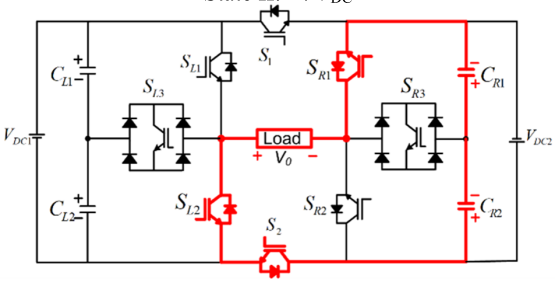
State X: $-V_{DC}$



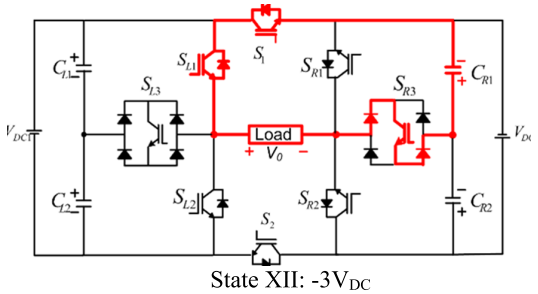
State II: $+7V_{DC}$



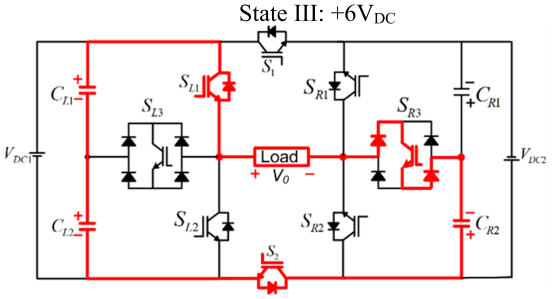
State XI: $-2V_{DC}$



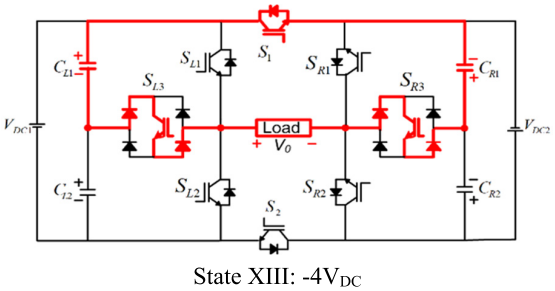
State III: $+6V_{DC}$



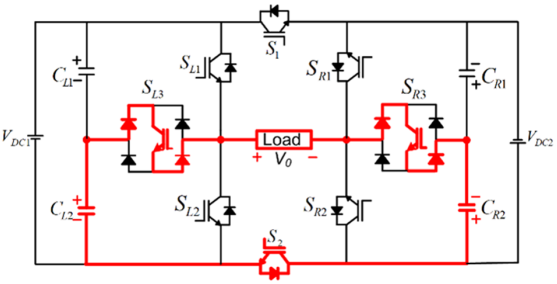
State XII: $-3V_{DC}$



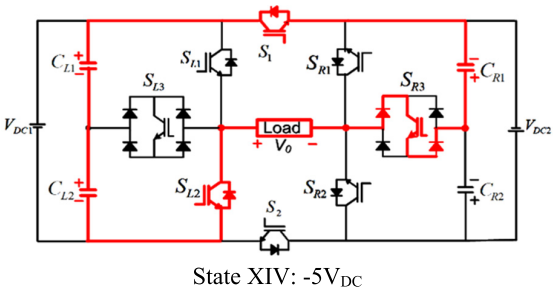
State IV: $+5V_{DC}$



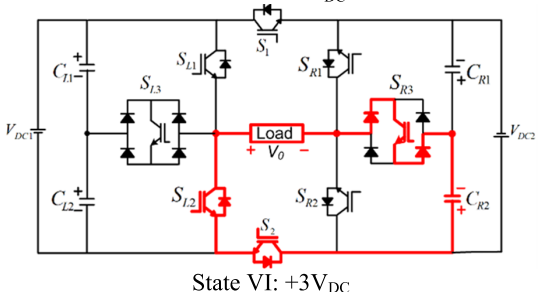
State XIII: $-4V_{DC}$



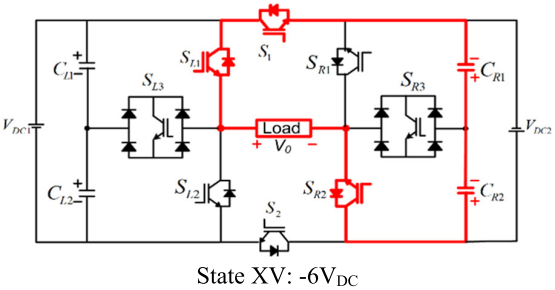
State V: $+4V_{DC}$



State XIV: $-5V_{DC}$



State VI: $+3V_{DC}$



State XV: $-6V_{DC}$

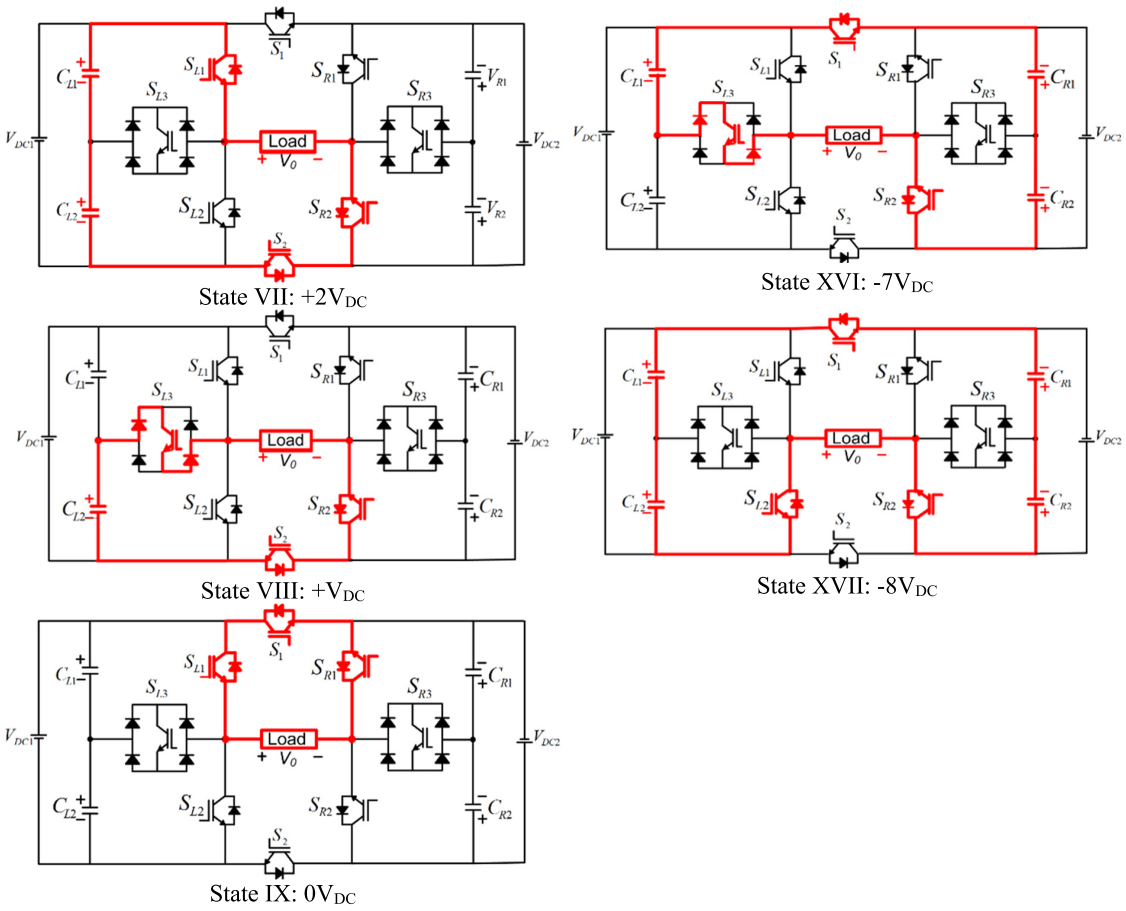


FIGURE 3. Different switching states.

When identical capacitance values are used, Eq. (1) achieves

$$\begin{cases} C_1 V_{C1} = C_2 V_{C2} \\ V_{C1} = V_{C2} \end{cases} \Rightarrow C_1 = C_2 \tag{2}$$

As a result, Eq. (2) provides identical values for the capacitances C_1 and C_2, i.e., $C_1 = C_2$. Each capacitor's maximum charge drawn is expressed as:

$$\Delta Q_C = I_L \int_{t_S}^{t_f} \sin(2\pi f_0 t)\, dt \tag{3}$$

where time interval $[t_S, t_f]$ demonstrates the worst conceivable state for each capacitor; I_L and f_0 indicate the load current amplitude and output fundamental frequency, respectively. Finally, it should be noticed that the capacitance values of capacitors C_1 and C_2 are identical, and when load is connected, the equivalent capacitance (C_{eq}) is expressed as:

$$C_{eq} \geq \frac{\Delta Q_C}{K \cdot V_{eq}} \tag{4}$$

K represents a scaling or ripple factor that relates the voltage ripple ΔV_C to the equivalent voltage V_{eq}, while V_{eq} denotes the equivalent voltage across the capacitor.

The equations provide the resistive load's output current as:

$$I_L(t) = \begin{cases} \frac{V_{dc}}{R_L} & \text{for } t_1 \leq t \leq t_2 \\ \frac{2V_{dc}}{R_L} & \text{for } t_2 \leq t \leq t_3 \\ \frac{3V_{dc}}{R_L} & \text{for } t_3 \leq t \leq \frac{T}{4} \end{cases} \tag{5}$$

However, the resistive-inductive load's output current is determined by the following equation:

$$I_L(t) = I_{\max} \sin(\omega t - \alpha)\, dt \tag{6}$$

The appropriate capacitor ranges under *RL* and pure resistive loads are obtained from (7) by solving Eqs. (3)–(6).

$$C_2 = C_1 \geq \frac{2 \int_{t_3}^{0.25T} I_L(t) dt}{K \cdot V_{eq}} \tag{7}$$

The proposed CT-type topology's circuit parameters are $R = 20\,\Omega$ and $40\,\Omega$, $L = 20\,\text{mH}$ and $40\,\text{mH}$, $K = 0.05$, $f_{ref} = 50\,\text{Hz}$, and the equivalent capacitance of both capacitors connected in series is $C_1 = C_2 \geq 1780\,\mu\text{F}$. Additionally, it indicates that it is necessary to select a minimum of two identical capacitors for the inverter, adhering to the specified requirements, the load conditions, and maintaining a capacitor voltage tolerance of 5% for ripple. In Sections 3 and 4, the nearest widely recognized capacitance value is selected for both model and experimental validation.

TABLE 1. Switching states of 17-level asymmetric configuration.

States	S_{L1}	S_{L2}	S_{L3}	S_1	S_2	S_{R1}	S_{R2}	S_{R3}	O/P	C_{L1}	C_{L2}	C_{R1}	C_{R2}
1	1	0	0	0	1	1	0	0	+8E	Discharging	Discharging	Discharging	Discharging
2	0	0	1	0	1	1	0	0	+7E	-	Discharging	Discharging	Discharging
3	0	1	0	0	1	1	0	0	+6E	-	-	Discharging	Discharging
4	1	0	0	0	1	0	0	1	+5E	Discharging	Discharging	-	Discharging
5	0	0	1	0	1	0	0	1	+4E	-	Discharging	-	Discharging
6	0	1	0	0	1	0	0	1	+3E	-	-	-	Discharging
7	1	0	0	0	1	0	1	0	+2E	Discharging	Discharging	-	-
8	0	0	1	0	1	0	1	0	+E	-	Discharging	-	-
9	1	0	0	1	0	0	1	0	0	-	-	-	-
10	0	0	1	1	0	1	0	0	−E	Charging	-	-	-
11	0	1	0	1	0	1	0	0	−2E	Charging	Charging	-	-
12	1	0	0	1	0	0	0	1	−3E	-	-	Charging	-
13	0	0	1	1	0	0	0	1	−4E	Charging	-	Charging	-
14	0	1	0	1	0	0	0	1	−5E	Charging	Charging	Charging	-
15	1	0	0	1	0	0	1	0	−6E	-	-	Charging	Charging
16	0	0	1	1	0	0	1	0	−7E	Charging	-	Charging	Charging
17	0	1	0	1	0	0	1	0	−8E	Charging	Charging	Charging	Charging

2.3. Asymmetric CT-Type Topology

A 17-level asymmetrical CT-type MLI with active current paths (*Red line*) is illustrated in Fig. 3, and different switching states are tabulated in Table 1. E represents the fundamental or base unit of DC-link voltage in the asymmetrical configuration of the 17-level multilevel inverter. A 17-level configuration has DC-links voltage of R and L modules 3E ($V_{C1R} = V_{C2R} = 3E$) and E ($V_{C1L} = V_{C2L} = E$), respectively.

2.4. Voltage Stress Calculations

Asymmetric operation TSV can be estimated as the switches' maximum voltage standing capacity in the OFF state. The sum of these voltages is used to calculate the proposed CT-Type MLI TSV. Table 1 tabulates the TSV calculation for the proposed CT-Type MLI for asymmetrical configuration. Further, the equations are given as:

$$\begin{aligned} V_{S1} &= E + E = 2E,\ V_{S2} = E + E = 2E, \\ V_{S3} &= 3E + 3E = 6E, \qquad (8) \\ V_{S4} &= 3E + 3E = 6E, \\ V_{S5} &= E + E + 3E + 3E = 8E, \qquad (9) \\ TSV &= V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} \\ &\quad + V_{S7} + V_{S8} = 36E. \qquad (10) \end{aligned}$$

3. SIMULATION STUDY

3.1. Modulation and Control Method of MLI

MLIs employ a variety of modulation techniques, such as low switching frequency techniques (e.g., active-harmonic elimination, selective-harmonic elimination, and nearest level control) and high switching frequency techniques (e.g., multi-carrier pulse width modulation and space-vector pulse width modulation). With appropriate modification, the proposed CT-type topology can be modified using any of these techniques. In the level shifted (LS) PWM approach, the triangular carrier signals are contrasted with the sinusoidal reference signal. Gate pulse is generated for switching devices at various voltage levels. $V_{ref\text{-}peak}$ denotes the peak value of the waveform; V_{car} represents the carrier amplitude; and modulation index (MI) [4] will be obtained using Eq. (10).

$$\text{MI} = \frac{V_{ref\text{-}peak}}{5V_{car}} \qquad (11)$$

The proposed circuit employs the phase opposition disposition (POD) approach to create gate pulses. Fig. 4(a) shows the schematic diagram of the control technique, and Fig. 4(b) shows time-domain waveform of LS-PWM. A single sinusoidal reference waveform is compared against four high-frequency triangular carrier signals ($C1(t)$ to $C4(t)$), each phase-shifted by 90° (or π/4 radians) relative to the previous one, enabling finer voltage steps and lower switching harmonics. Each carrier is individually compared with the reference in dedicated comparators, producing four binary PWM signals that represent switching decisions for the inverter legs. The individual PWM outputs are summed (aggregated) to form a multilevel gate signal with five discrete levels (from 0 to 4), which is then mapped via a look-up table (LUT) to generate the final switching pulses for the power switches, ensuring proper dead-time and synchronization. Due to the switching redundancy of particular voltage levels, a specific switching state is chosen to reduce the higher to lower voltage levels switching of the IGBT. PWM signals generated for switches S_1 to S_7 are decided by the location of high-frequency carriers.

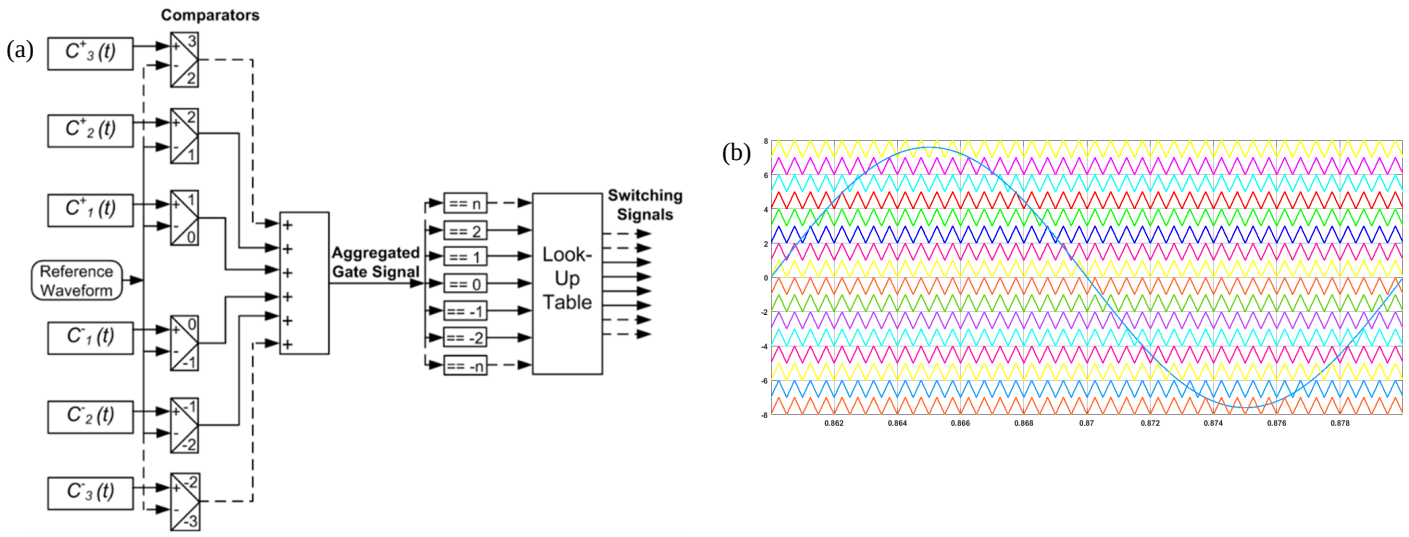


FIGURE 4. (a) Block diagram of control method. (b) Corresponding waveform.

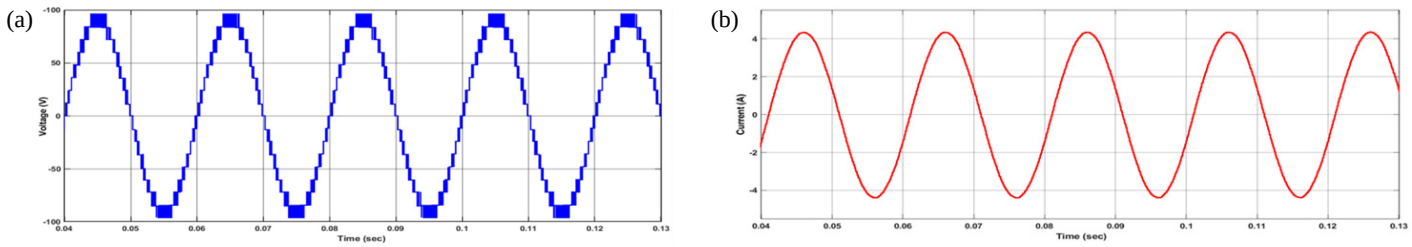


FIGURE 5. (a) Output voltage. (b) Load current.

3.2. Simulation Results

MATLAB/Simulink software is used in this subsection to implement the proposed CT-type MLI with LS-PWM modulation. The simulation parameters are tabulated in Table 2. In the asymmetrical configuration, the input source $V_{DC1} = 24$ V and $V_{DC2} = 72$ V is applied to get the desired output. Fig. 5(a) illustrates the 17-level voltage output waveform for the proposed topology in an asymmetric configuration. The peak value of output voltage is $V_{BB} = 96$ V at 17 levels of voltage. The proposed CT-type topology load current waveform in an asymmetric configuration is shown in Fig. 5(b). Fig. 6(a) illustrates the voltage across capacitors (C_{L1} and C_{L2}) in an asymmetric configuration. Similarly, Fig. 6(b) shows the voltage across capacitors (C_{R1} and C_{R2}) in an asymmetric configuration.

TABLE 2. Simulation parameters.

Parameters	Ratings
Switching frequency	$f_s = 3150$ Hz
Modulation index	$m_a = 0.85$
Load value	$R = 20\,\Omega$, $L = 20$ mH
Modulating wave frequency	$f_m = 50$ Hz
Capacitors	$C_2 = C_1 = 2200$ µF
Rated DC voltage	$V_{DC1} = 24$ V & $V_{DC2} = 24$ V

4. EXPERIMENTAL SETUP RESULTS

A laboratory prototype has been developed with power switch modules, gate drivers, and isolated power supplies to validate the proposed CT-type topology. The representation of the experimental test rig is illustrated in Fig. 7. The values of various components and parameters are listed in Table 3. A dSPACE-1104 controller is used for implementing the simulated gate pulses and control signal on an experimental setup.

Asymmetric model is constructed by providing $V_{C1L} = V_{C2L} = 24$ V and $V_{C1R} = V_{C2R} = 72$ V. The inverter's DC-link

TABLE 3. Parameters of experimental setup.

Parameters	Value
Capacitor (LGU2A222MELA)	2200 µF
DC Source (lead acid battery)	28 Ah
Driver circuit (TLP250(F))	10–35 V
Output voltage frequency	50 Hz
Switching frequency	3150 Hz
IGBT switch (GW30NC120HD)	1200 V, 30 A
Digital storage oscilloscope (DL-750E)	6-channel
Controller board (dSPACE-1104)	-
Single-phase power analyzer (Fluke)	-
Load (RL Load)	$R = 40\,\Omega$, $L = 40$ mH $R = 20\,\Omega$, $L = 20$ mH

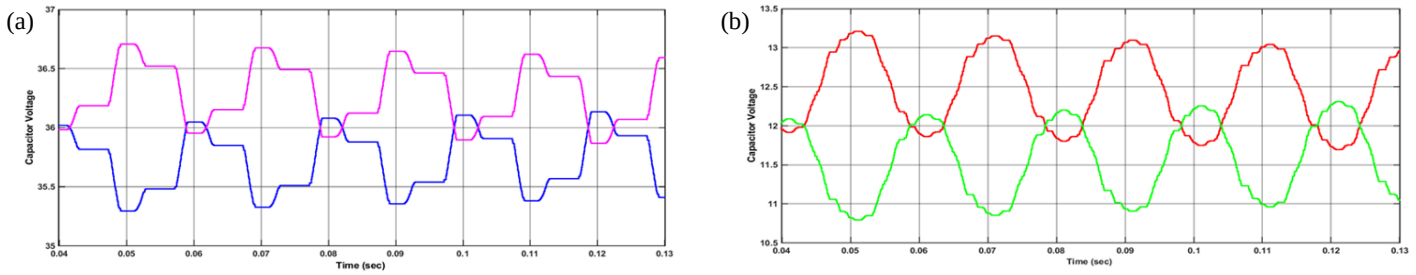


FIGURE 6. Voltage across capacitors. (a) C_{L1} and C_{L2}, (b) C_{R1} and C_{R2}.

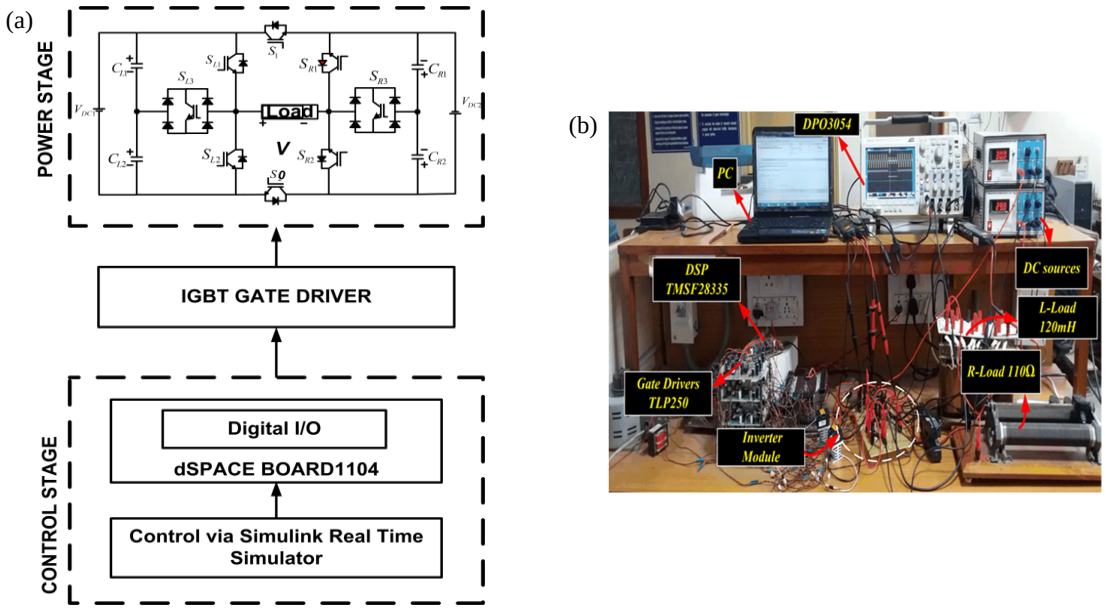


FIGURE 7. Laboratory snapshot of the experimental setup.

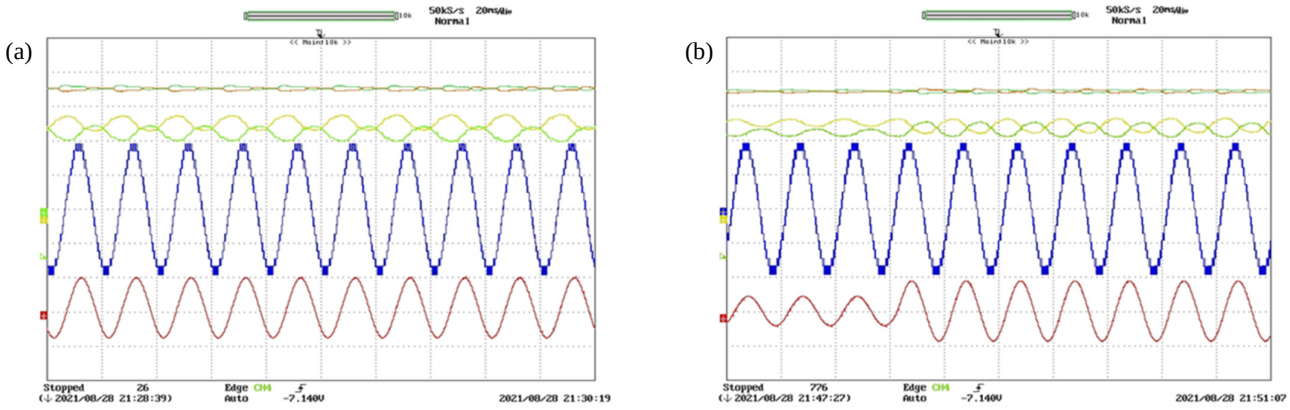


FIGURE 8. Experimental results, (a) capacitors voltage (C_{L1} and C_{L2}), load current, and output voltage with ($R = 20\,\Omega$, $L = 20$ mH), (b) capacitors voltage of (C_{R1} and C_{R2}), load current, and output voltage with ($R = 40\,\Omega$, $L = 40$ mH).

voltage is 96 V in total. A single-phase RL load with $R = 40\,\Omega$ & $20\,\Omega$ and $L = 40$ mH & 20 mH has connected to the module output.

The prototype is created utilizing four equal DC supplies in asymmetric operation, with $V_{C1L} = V_{C2L} = V_{C1R} = V_{C2R} =$ 12 V, bringing the total inverter DC-link voltage to 48 V. In steady-state and dynamic load conditions, experimental results of capacitor voltage, output voltage, and load current are illustrated in Figs. 8(a) and 8(b). Figs. 9(a) and 9(b) show 7.2% of voltage THD and 1.3% of current THD.

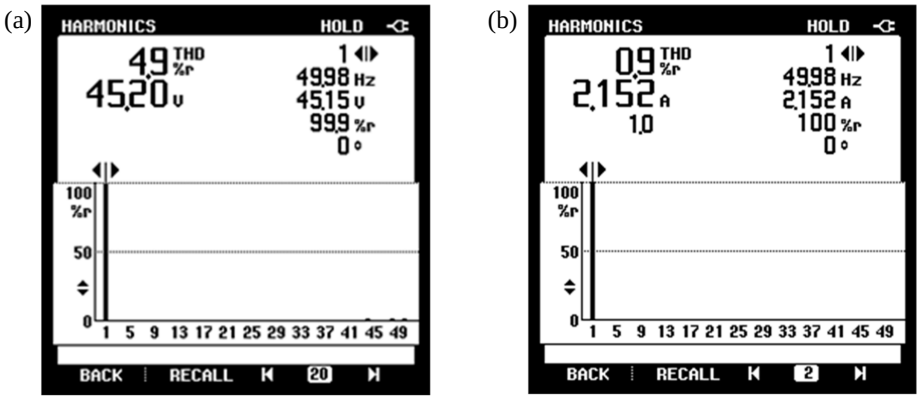


FIGURE 9. Experimental results with load ($R = 20\,\Omega$, $L = 20\,\text{mH}$) showing: (a) Output voltage THD; (b) Output current THD.

TABLE 4. Comparison of topologies (MLLs) to generate 17-level output based on the component requirement.

Topologies	Capacitors and DC supplies	Diodes	Power switches	Driver circuit	TSV	Total components	CF/Level		
							$\alpha = 0.5$	$\alpha = 1$	$\alpha = 1.5$
Diode Clamp MLI	16	48	32	32	32	96	6.57	7.51	8.48
Cascaded H-bridge MLI	8	32	32	32	32	72	5.18	6.10	7.04
Flying capacitor MLI	16	32	32	32	32	80	5.63	6.59	7.51
[26]	4	14	10	10	36	28	2.70	3.76	4.82
[27]	4	12	12	12	40	28	2.82	4	5.17
Proposed CT-type MLI	6	8	8	8	36	22	2.47	3.52	4.58

5. LOSS CALCULATION

In the proposed CT-type topology, power switches are primarily associated with two categories of losses: switching losses and conduction losses. Conduction losses (P_C) occur due to the flow of current in switches when they are in the ON state. The insulated gate bipolar transistor (IGBT) and the anti-parallel diode within the MLI switch conduct the associated load current. As a result, P_C is determined by adding the conduction losses in the IGBT and anti-parallel diode ($P_{C,D}$). We estimate $P_{C,IGBT}$ and $P_{C,D}$ as follows:

$$P_{C,IGBT} = n_{IGBT}(t) \cdot \left[\frac{1}{2\prod}\int_0^{2\Pi} [V_{ON,IGBT} I + R_{ON,IGBT} I^{\beta+1} d(\omega t)]\right] \quad (12)$$

$$P_{C,D} = n_D(t) \cdot \left[\frac{1}{2\prod}\int_0^{2\Pi} [V_{ON,D} + R_{ON,D} I^2 d(\omega t)]\right] \quad (13)$$

$$P_C = P_{C,IGBT} + P_{C,D} \quad (14)$$

where $n_{IGBT}(t)$ is the duty cycle; $V_{ON,IGBT}$ is the on-state zero-current collector-emitter voltage drop (threshold voltage) of the IGBT; $R_{ON,IGBT}$ is the on-state collector-emitter resistance of the IGBT; I is the instantaneous value of the collector current flowing through the IGBT; β is an exponent or a scaling factor related to the current dependency of the conduction losses; ω is the angular frequency similarly in case of diode.

6. COMPARISON ASSESSMENTS

A comparison of numerous topologies with characteristics analogous to the proposed topology has been given in this section. The proposed CT-Type MLI topology is compared with standard topologies, such as diode clamped, FC-MLIs, CHB, and topologies in [27]. It is observed that CT-Type MLI provides significantly higher output level than other topologies found in the literature. It indicates that, compared to other topologies, the total number of components required to produce a given number of levels is significantly lower in the proposed topology, which can be seen in Table 4, while the comparison between simulated and experimental results ia tabulated in Table 5. For example, the FC-MLI, CHB-MLI, diode clamped, and topologies components needed for the asymmetric CT-Type MLI to generate 17-level output are 22, which is substantially lower than those required in conventional topologies and topologies given in [22]. TSV is much higher in CT-Type MLI than in standard topologies, and we must use switches with larger reverse blocking capability. Cost factor (CF) [4] for the proposed MLI to determine the cost-effectiveness is obtained using Eq. (15).

$$\text{CF} = \frac{[N_{dc} + N_s + N_{dio} + N_{cap} + \alpha(\text{TSV})] * nV_{dc}}{N_{levels}} \quad (15)$$

TABLE 5. Comparison between simulated and experimental results.

Parameter	Simulation ($R = 20\,\Omega$, $L = 20\,\text{mH}$)	Experimental ($R = 20\,\Omega$, $L = 20\,\text{mH}$)	Simulation ($R = 40\,\Omega$, $L = 40\,\text{mH}$)	Experimental ($R = 40\,\Omega$, $L = 40\,\text{mH}$)	% Deviation
Peak Output Voltage	96 V (17 levels)	∼48 V (scaled prototype)	96 V (17 levels)	∼48 V (scaled)	$< 5\%$ (scaled)
Switching Frequency	3150 Hz	3150 Hz	3150 Hz	3150 Hz	0%
Modulation Index	0.85	0.85	0.85	0.85	0%
Capacitor Voltage	CL1/CL2: 24 V, CR1/CR2: 72 V	CL1/CL2: 12 V, CR1/CR2: scaled	Same as left	Stable balancing observed	$< 5\%$ ripple

where 'N_{dio}' is the total number of diodes, 'N_S' the total number of switches, 'N_{cap}' the capacitor count, 'N_{DC}' the number of DC supplies, n the scaling factor, 'α' the weight coefficient, and 'TSV' the total standing voltage.

7. CONCLUSION

This work presents a single-phase CT-Type MLI topology with reduced device count. Also, the operating principles, control design, and TSV are explained in detail. The DC-link capacitors achieve self-voltage balance. The main benefit of the proposed work is its capability to generate negative voltage levels without using a modified H-bridge. The proposed topology can be used for high output voltage waveforms without putting additional stress on the power switches. The cascading of modular structures is used to extend the proposed topology for high-voltage levels (17 levels and 289 levels) with a reduced device count. Therefore, this CT-Type MLI is suitable for renewable energy systems and high-voltage/power applications. Several simulated and experimental results of the proposed CT-Type MLI at different load conditions are presented to show the effectiveness of the topology. The proposed CT-Type is superior to other recently developed MLI topologies on the basis of number of drivers, capacitors, DC sources, and power switches, thereby making the entire system simpler and less expensive. Capacitors maintain self-balancing within 5% ripple in both cases (2200 µF used), confirming theoretical design. Hardware THD values (7.2% voltage, 1.3% current) indicate practical performance suitable for renewable integration. Hence, the proposed topology's performance in various operational situations is satisfactory.

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