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Design of a π-Type Broadband Flat Negative Group Delay Circuit

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ABSTRACT: This study proposes a novel π-type circuit topology designed to achieve broadband and flat negative group delay (NGD) characteristics. Featuring a simple structure composed entirely of passive lumped elements, the proposed design offers significant advantages in terms of ease of fabrication, low cost, and seamless integration into larger microwave systems. First, a comprehensive theoretical analysis was conducted to establish the operational principles and derive the design equations. We then systematically investigated the sensitivity of the circuit's performance to variations in individual component values, which provides crucial guidelines for practical implementation. To validate our theoretical findings, a physical prototype with compact dimensions of 32 mm $\times$ 35 mm was designed and fabricated. Experimental results demonstrate that at the center frequency of 107.5 MHz, the circuit achieves an NGD of -2.27 ns with an insertion loss of 19.5 dB. Notably, the circuit maintains a wide flat NGD bandwidth of 151 MHz, exhibiting a group delay fluctuation of merely 4.1% across the band. These results confirm the effectiveness and robustness of the proposed circuit for broadband microwave applications.

1. INTRODUCTION

Group delay refers to the negative derivative of the phase of a signal that changes with frequency as it passes through a system, reflecting the delay characteristics of signal transmission in the system. When group delay is negative, it indicates that the phase of the signal has advanced in certain frequency bands after passing through the system, which is in contrast to the traditional signal delay (positive group delay). Early research focused mainly on the mechanism of the NGD phenomenon and its characteristics in the frequency domain. Through theoretical analysis [1, 2], researchers have gradually revealed the inherent relationship between NGD and electromagnetic wave propagation characteristics, thereby providing a solid theoretical basis for subsequent circuit design.

The unique properties of NGD circuits make them applicable to multiple fields [3]. For example, the proposed NGD circuit can be used in microwave communication systems to achieve broadband constant phase response [4], reduce the size of feedforward amplifiers, improve their efficiency, optimize beam deflection problems in phase array antenna systems [5], reduce filter passband delay, enhance power divider bandwidth, etc. These applications not only improve the performance of the system, but also expand the practical application range of NGD circuits.

Researchers have designed a series of microwave devices with novel characteristics to further enhance the performance and application value of NGD circuits [6]. These new devices not only retain the unique properties of NGD circuits but also have higher stability and broader application prospects. With the deepening of research, researchers have begun to use various components and structures to design NGD circuits. Circuits based on technologies such as left-handed materials and coupled microstrip lines are constantly emerging, each with its own characteristics; however, there are still some challenges and unresolved issues. For example, it is necessary to further reduce circuit losses, broaden bandwidth, and improve stability.

To address these issues, researchers have continuously optimized circuit designs to achieve flat NGD circuits with wider frequency bands and lower losses [7, 8]. In [9], an NGD circuit composed of microstrip lines was proposed, with an NGD of -1.11 ns and an insertion loss of 9.75 dB. The flat NGD bandwidth was 6.1%, and the group delay fluctuation was $\pm 11.5\%$. In the study of flat NGD circuits, many scholars have used a fluctuation of 8% as a standard [10], which has an NGD of about -0.5 ns and an insertion loss over 15 dB under this standard. Similarly, many scholars have used a fluctuation of 20% as a standard, which has an NGD of -0.2 ns and an insertion loss of 14 dB under this standard in [11]. Subsequently, scholars attempted to connect a flat NGD circuit with other communication modules [12, 13], aiming to balance its phase characteristics while endowing the circuit with more functions. However, the NGD values of the proposed flat NGD circuits were mostly between 0 and -1 ns, and these circuits cannot function properly in communication systems with significant group delays.

Therefore, this study proposes a broadband flat NGD circuit with -2.29 ns. This study consists of four parts. The second part describes the circuit structure and conducts a theoretical analysis of the circuit transfer function and group delay, exploring the influence of various component parameters on the circuit. The third part presents the circuit theory and simulation

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results and compares them with other research results to demonstrate that the circuit has lower NGD and broadband advantages. The final section presents the conclusions of the study.

2. DESIGN AND ANALYSIS OF BROADBAND FLAT NGD CIRCUIT

The π-type broadband flat NGD circuit structure proposed in this study is illustrated in Fig. 1. The two branches of the circuit have the same structure, consisting of passive components, such as resistors, capacitors, and inductors. Because the circuit is a two-port circuit, the S-parameter matrix was adopted to analyze and calculate the circuit. The S-parameter matrix of the two-port circuit is given by Equation (1). In a passive symmetric network, the input and output reflection coefficients are in accordance with $S_{11} = S_{22}$. $S_{21}(\mathrm{j}\omega)$ represents the transmission coefficient of energy from port 1 to port 2, and for reciprocal networks, $S_{21} = S_{12}$.

$$[S(\mathrm{j}\omega)] = \begin{pmatrix} S_{11}(\mathrm{j}\omega) & S_{12}(\mathrm{j}\omega) \\ S_{21}(\mathrm{j}\omega) & S_{22}(\mathrm{j}\omega) \end{pmatrix} \tag{1}$$

where ω is the angular frequency, and j represents the imaginary unit. The total impedance Z calculation equation of this circuit is shown in Equation (2), where Z_1 is the impedance of the left branch, Z_2 the impedance of the series branch, and Z_3 the impedance of the right branch, Their specific calculations are shown in Equation (3). According to the relevant theory of microwave circuits, the parameters of the $ABCD$ matrix corresponding to the π-type circuit are shown in Equation (4), where Y_1 is the admittance of the left branch, and Y_2 is the total admittance of the series branch and the right branch, as shown in Equation (5). The relationship between the $ABCD$ matrix and S_{21} is shown in Equation (6), where Z_0 is the characteristic impedance of the circuit, and $Z_0 = 50\,\Omega$.

$$Z = \frac{Z_1 * (Z_2 + Z_3)}{Z_1 + (Z_2 + Z_3)} \tag{2}$$

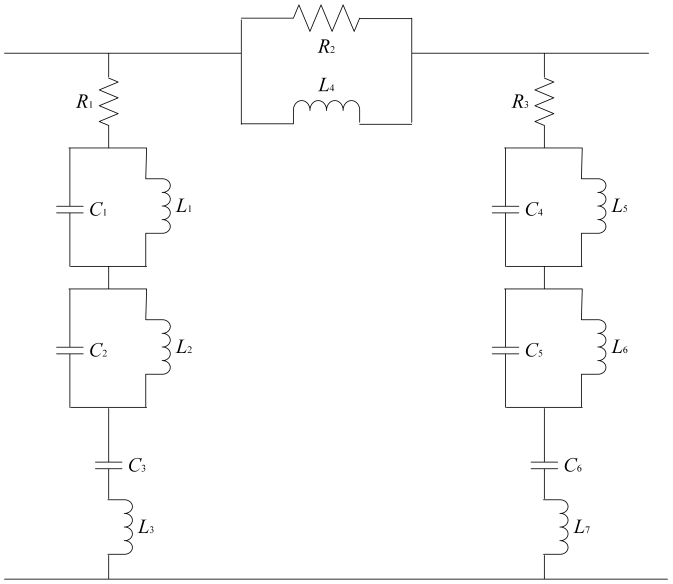

FIGURE 1. Structure diagram of broadband flat NGD circuit.

$$\begin{cases} Z_1 = R_1 + L_3\mathrm{j}\omega - \frac{\mathrm{j}}{C_3\omega} - \frac{L_1\mathrm{j}\omega}{C_1L_1\omega^2-1} - \frac{L_2\mathrm{j}\omega}{C_2L_2\omega^2-1} \\ Z_2 = \frac{R_2L_4\mathrm{j}\omega}{R_2+L_4\mathrm{j}\omega} \\ Z_3 = R_3 + L_7\mathrm{j}\omega - \frac{\mathrm{j}}{C_6\omega} - \frac{L_5\mathrm{j}\omega}{C_4L_5\omega^2-1} - \frac{L_6\mathrm{j}\omega}{C_5L_6\omega^2-1} \end{cases} \tag{3}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{Y_2} \\ Y_1 & 1+\frac{Y_1}{Y_2} \end{bmatrix} \tag{4}$$

$$\begin{cases} Y_1 = \frac{-1}{-R_1-L_3\mathrm{j}\omega+\frac{\mathrm{j}}{C_3\omega}+\frac{L_1\mathrm{j}\omega}{C_1L_1\mathrm{j}\omega^2-1}+\frac{L_2\mathrm{j}\omega}{C_2L_2\mathrm{j}\omega^2-1}} \\ Y_2 = \frac{1}{R_3+L_7\mathrm{j}\omega-\frac{\mathrm{j}}{C_6\omega}-\frac{L_5\mathrm{j}\omega}{C_4L_5\mathrm{j}\omega^2-1}-\frac{L_6\mathrm{j}\omega}{C_5L_6\mathrm{j}\omega^2-1}+\frac{L_4R_2\mathrm{j}\omega}{R_2+L_4\mathrm{j}\omega}} \end{cases} \tag{5}$$

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + C * Z_0 + D} \tag{6}$$

Group delay is defined as the negative reciprocal of the phase to angular frequency relationship, and its calculation formula is shown in Equation (7).

$$\tau(\omega) = -\frac{\partial\phi(\omega)}{\partial\omega} \tag{7}$$

where τ represents the group delay, and $\varphi(\omega)$ (or $\angle S_{21}$) represents the phase function. The specific calculation of this phase function is shown in Equation (8).

$$\phi(\omega) = \angle S_{21} = \tan^{-1}\frac{\mathrm{Im}[S_{21}]}{\mathrm{Re}[S_{21}]} \tag{8}$$

3. PARAMETER ANALYSIS OF FLAT NGD CIRCUIT

To investigate the performance of the proposed NGD circuit and assess the impact of each component on the overall circuit, this study employed a research methodology that involved controlling a single variable. In the electronic and radio frequency (RF)/microwave circuit schematic simulation environment, Advanced Design System (ADS) of Keysight Technologies, each component was simulated respectively, and the simulation results are discussed and analyzed.

3.1. Analysis of the Impact of Resistances on Flat NGD Circuit

By varying the value of R_1 while keeping the other components constant in the circuit, we can observe the result on the simulation platform to understand how resistance R_1 impacts the overall performance. For example, when $R_1 = 20\,\Omega$, $C_1 \sim C_6 = 150\,\mathrm{pF}$, $L_1 \sim L_3 = L_5 \sim L_7 = 3.9\,\mathrm{nH}$, $R_2 = 50\,\Omega$, $L_4 = 470\,\mathrm{nH}$, the simulated results obtained by changing R_1 from 5 to 50 Ω are presented in Table 1. Notably, as the value of R_1 increases, the insertion loss of the proposed circuit decreases. However, the group delay and NGD bandwidth of the circuit increase accordingly. After reaching a certain value, the change becomes relatively slow. In addition, the group delay performance of the circuit flattens as R_1 increases. Waveform diagrams corresponding to the flat circuit at different values of R_1 are shown in Fig. 2. Because R_1 and R_3 have a symmetric relationship in the proposed π-type circuit structure, their effects on the circuit are identical. To investigate the

TABLE 1. Performance of flat NGD circuits with different R_1 values.

R_1 (Ω)	IL (dB)	NGD at f_0 (ns)	NBW (MHz)	FNBW (MHz)
5	28.34	−7.47	123.0	*
20	19.57	−2.29	151.6	107.5
50	15.83	−1.49	162.0	135.0

TABLE 2. Performance of flat NGD circuits with different R_2 values.

R_2 (Ω)	IL (dB)	NGD at f_0 (ns)	NBW (MHz)	FNBW (MHz)
10	13.47	−1.66	152.5	100.5
50	19.57	−2.29	151.0	107.5
100	23.54	−2.66	150.5	112.5

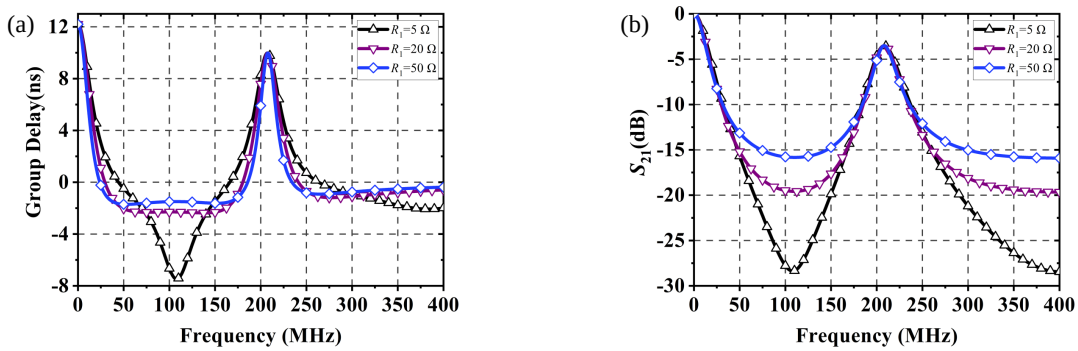

FIGURE 2. Simulation results with different R_1 values. (a) Group delay. (b) S_{21}.

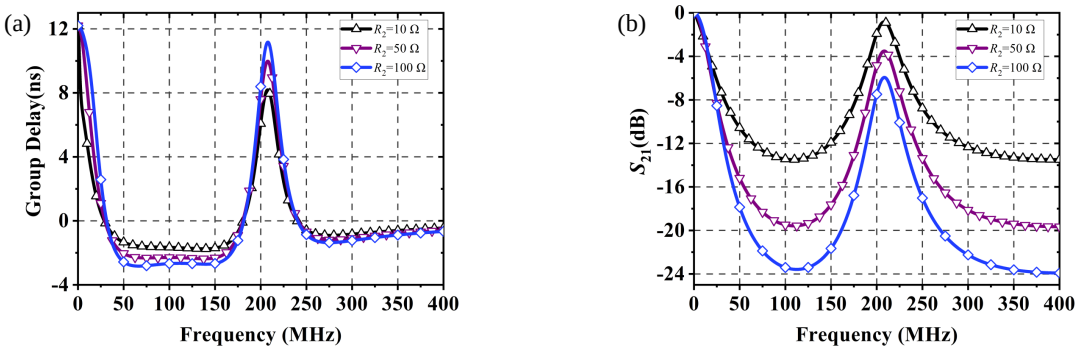

FIGURE 3. Simulation results with different R_2 values. (a) Group delay. (b) S_{21}.

impact of R_2 on circuit performance, while maintaining a constant value for the other components, R_1 was set to 20 Ω, and simulations were conducted with varying values of R_2. The simulation results are listed in Table 2. It can be observed that as R_2 increases, the insertion loss increases, and the group delay at the center frequency decreases, but the bandwidth of the circuit remains essentially unchanged. As shown in Fig. 3, the change in R_2 has little impact on the NGD bandwidth of the flat circuit. The performance of the circuit is evaluated in terms of Insertion Loss (IL), Negative Group Delay Bandwidth (NBW), and Flat NGD Bandwidth (FNBW). The FNBW is defined as the frequency range over which the NGD fluctuation is within $\pm X\%$.

3.2. Analysis of the Impact of Capacitances on Flat NGD Circuit

Because C_1, C_2, C_4, and C_5 have symmetric relationships in the circuit structure, their effects on the circuit are the same. To analyze their influence on the circuit performance, C_1 was selected for simulation testing while keeping the values of the other components unchanged except for C_1. When the values of C_1 are set as 50 pF, 150 pF, and 200 pF, simulations are conducted on the circuit. The obtained data are presented in Table 3. It can be seen from these data that as the value of C_1 increases, both the group delay and NGD bandwidth of the circuit decrease, while the change in the insertion loss of the circuit is negligible. As shown in Fig. 4, it can be more intuitively observed that C_1, C_2, C_4, and C_5 mainly affect the bandwidth of the circuit. The larger the capacitance value is, the smaller the bandwidth is.

Because C_3 and C_6 have a symmetric relationship in the circuit structure, C_3 was selected for simulation testing to analyze their impact on circuit performance. The values of the components other than C_3 were kept constant. Simulations were performed on the circuit when the values of C_3 were 50 pF, 150 pF, and 200 pF. The obtained data are presented in Table 4. It can be observed that as the value of C_3 increases, both the insertion loss and the NGD bandwidth of the circuit increase, while the group delay decreases. However, as shown in Fig. 5, the changes in the insertion loss and group delay are extremely

TABLE 3. Performance of flat NGD circuits with different C_1 values.

R_1 (Ω)	IL (dB)	NGD at f_0 (ns)	NBW (MHz)	FNBW (MHz)
50	19.49	−2.18	155.5	114.0
150	19.57	−2.29	151.0	107.5
200	19.46	−2.37	139.5	102.0

TABLE 4. Performance of flat NGD circuits with different C_3 values.

C_3 (pF)	IL (dB)	NGD at f_0 (ns)	NBW (MHz)	FNBW (MHz)
50	17.48	−1.77	146.5	*
150	19.57	−2.29	151.0	107.5
200	19.58	−2.30	153.5	117.0

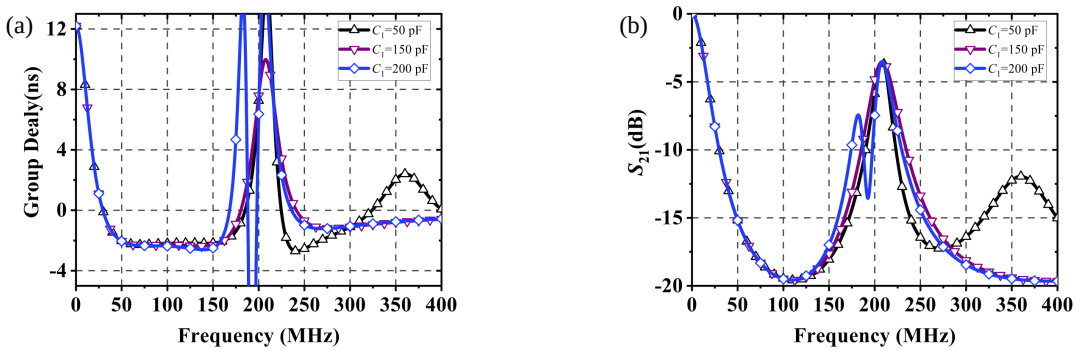

FIGURE 4. Simulation results with different C_1 values. (a) Group delay. (b) S_{21}.

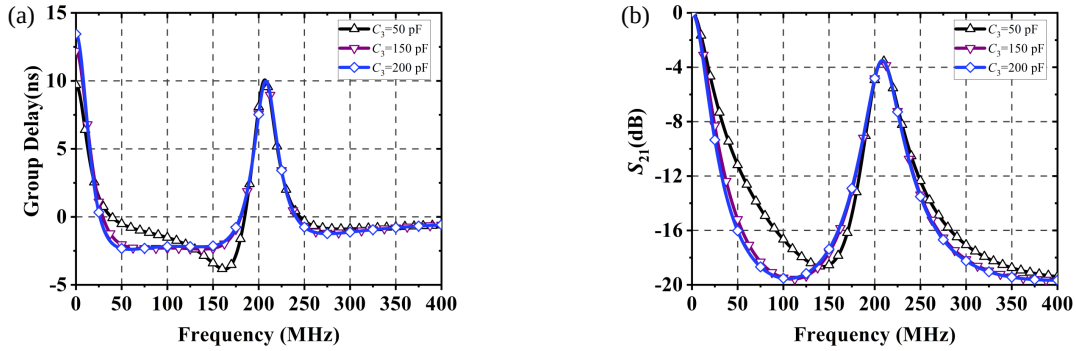

FIGURE 5. Simulation results with different C_3 values. (a) Group delay. (b) S_{21}.

TABLE 5. Performance of a flat NGD circuit when L_1 value changes.

L_1 (nH)	IL (dB)	NGD at f_0 (ns)	NBW (MHz)	FNBW (MHz)
0.9	19.50	−2.02	158.5	122.5
3.9	19.57	−2.29	151.0	107.5
5.9	19.38	−2.58	127.0	83.0

TABLE 6. Performance of a flat NGD circuit when L_3 value changes.

L_3 (nH)	IL (dB)	NGD at f_0 (ns)	NBW (MHz)	FNBW (MHz)
0.9	19.49	−2.18	152.5	114.0
3.9	19.57	−2.29	151.0	107.5
5.9	19.56	−2.35	151.0	100.0

small. Moreover, when the value of C_3 is relatively small, the circuit waveform does not exhibit a flat characteristic. As the value of C_3 increases, the circuit becomes increasingly flat.

3.3. Analysis of the Impact of Inductances on Flat NGD Circuit

Similarly, L_1, L_2, L_5, and L_6 had symmetrical positions in the circuit. Therefore, to study their impact on the circuit, L_1 was taken as an example for the simulation analysis. When the values of other components in the circuit remain unchanged, the circuit performance is compared with the values of L_1, being 0.9 nH, 3.9 nH, and 5.9 nH, respectively, as shown in Table 5. As the value of L_1 increases, the group delay and NGD bandwidth decrease, as the insertion loss of the circuit remains essentially unchanged. As shown in Fig. 6, there are no significant fluctuations in the insertion loss or group delay in the flat part of the circuit. It can be seen that L_1, L_2, L_5, and L_6 mainly affect the NGD bandwidth of the circuit.

When the values of the other components in the circuit remain unchanged, and only the value of L_3 is changed to study the influence of L_3 and L_7 on the circuit, the simulation results

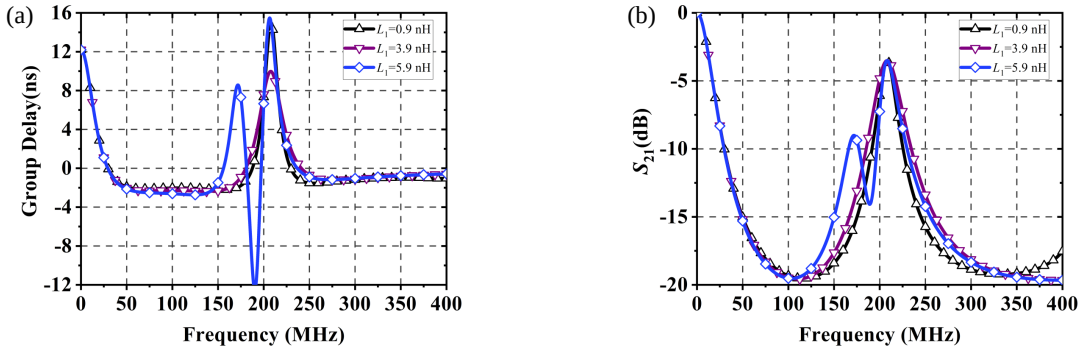

FIGURE 6. Simulation results produced by different L_1 values. (a) Group delay. (b) S_{21}.

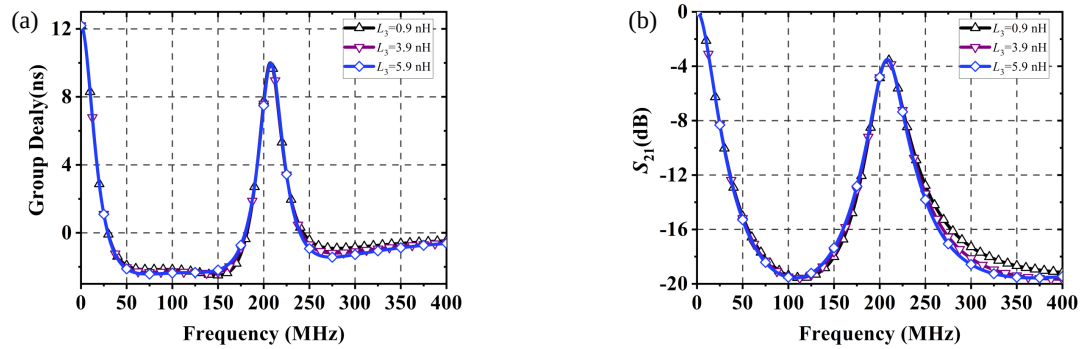

FIGURE 7. Simulation results produced by different L_3 values. (a) Group delay. (b) S_{21}.

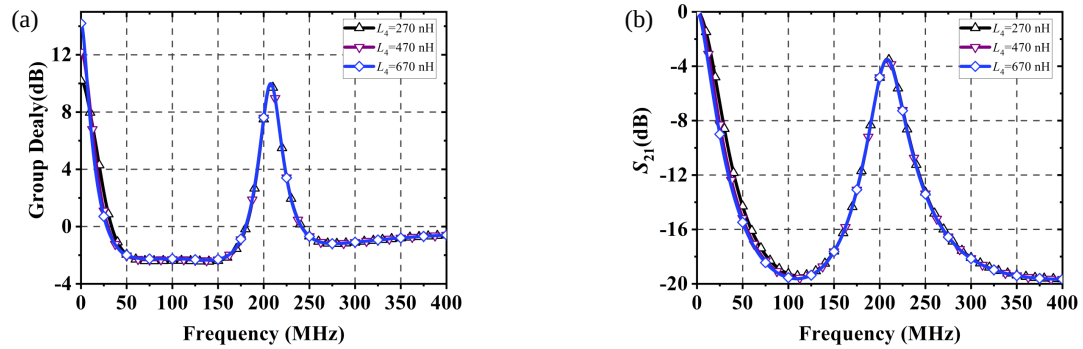

FIGURE 8. Simulation results produced by different L_4 values. (a) Group delay. (b) S_{21}.

TABLE 7. Performance of a flat NGD circuit when L_4 value changes.

L_3 (nH)	IL (dB)	NGD at f_0 (ns)	NBW (MHz)	FNBW (MHz)
270	19.35	−2.37	147.5	104.0
470	19.57	−2.29	151.0	107.5
670	19.60	−2.25	152.5	106.5

are shown in Table 6. The group delay, NGD bandwidth, and insertion loss of the circuit change, but the fluctuations are relatively small. As shown in Fig. 7, the value of L_3 increases, and only the flat NGD bandwidth of the circuit decreases significantly. Because the structures of L_3 and L_7 are symmetrical, they have the same effect on the circuit.

When the values of the other components in the circuit remain unchanged, the simulation results of the circuit with the values of L_4 being 270 nH, 470 nH, and 670 nH, respectively, are shown in Table 7. It can be found that even when the value of L_4 changes significantly, the variations of the circuit parameter are still relatively small. As shown in Fig. 8, when the value of L_4 increases, the insertion loss and NGD bandwidth of the circuit increase slightly.

4. CIRCUIT SIMULATION AND ACTUAL MEASUREMENT RESULTS

After the above simulation and discussion, the component parameters listed in Table 8 were selected to form the physical circuit. When designing the printed circuit board (PCB), FR-4 epoxy laminate was chosen as the board material with di-

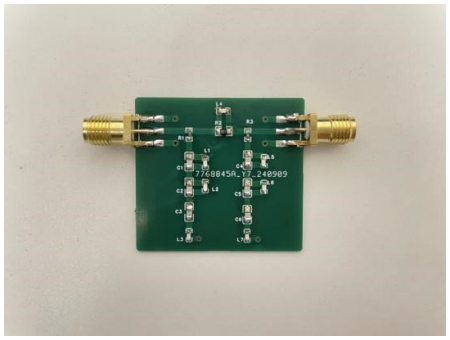

FIGURE 9. Multi-band NGD circuit generated by cascade.

Component parameters	Value
R_1, R_3	20 Ω
$C_1 \sim C_6$	150 pF
$L_1 \sim L_3, L_5 \sim L_7$	3.9 nH
R_2	50 Ω
L_4	470 nH

TABLE 8. Component parameters of broadband flat NGD circuit.

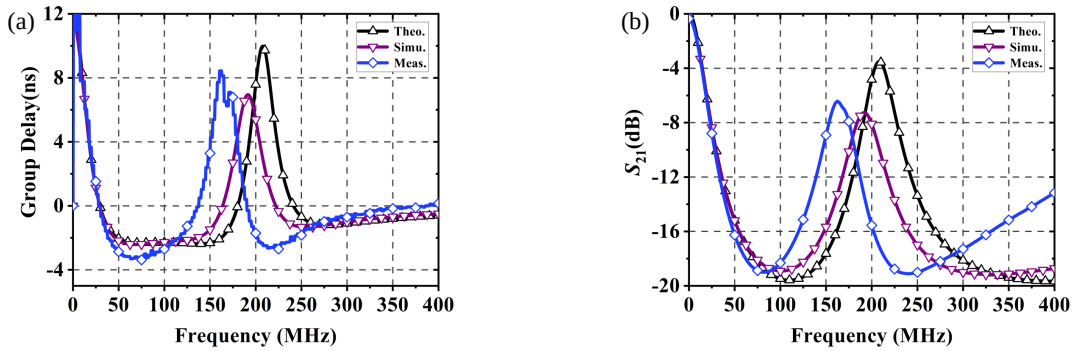

FIGURE 10. Comparison of theoretical, simulated, and measured results of the proposed flat circuit. (a) Group delay. (b) S_{21}.

TABLE 9. Measurement results and performance comparison of flat NGD circuit.

Circuit Type (nH)	IL (dB)	NGD at f_0 (ns)	NBW (MHz)	FNBW (MHz)
Theoretical circuit	19.6	−2.29	151.0	107.5
Simulation circuit	18.9	−2.28	135.5	80.5
Measured circuit	19.0	−3.22	106.5	41.5

mensions of 32 mm × 35 mm. The thickness of the board was 0.8 mm, and to ensure a reference impedance of 50 Ω, a line width of 47.32 mil and copper thickness of 1 oz were set. The physical appearance of the PCB is shown in Fig. 9. The completed physical circuit was connected to a dual-port Vector Network Analyzer (VNA) to measure its actual performance. The measurement results, simulation results, and theoretical values of the circuit performance are compared in Table 9 with the corresponding waveforms shown in Fig. 10. Owing to the influence of parasitic parameters between the components in the parallel circuit and the trace inductance introduced by the PCB interconnects, there is a small deviation between the measured and theoretical values. However, the proposed circuit demonstrates excellent NGD performance with a measured value of −3.23 ns.

$$GD\ fluctuation = \tau_1 - \tau_0 \tag{9}$$

TABLE 10. Performance of a flat NGD circuit when L_4 value changes.

Reference (nH)	IL (dB)	NGD at f_0 (ns)	NBW (MHz)	GD ripple
[14]	18.3	−0.54	329	14%
[15]	33.1	−0.88	460	25%
[16]	20.8	−0.51	105	10.0%
[17]	32.5	−1.58	448	8.0%
[18]	6.7	−0.50	92	-
[19]	18.0	−0.48	495	19%
This work	19.5	−2.29	151	4.1%

The comparison results are listed in Table 10 by comparing the experimental results with those of other existing studies. Although this design has a certain degree of insertion loss, its NGD performance is significantly better than that of other flat circuits. Moreover, the GD ripple of this circuit is only 4.1%, which avoids the phase distortion of different frequency components and ensures the integrity of the signal waveform during the transmission. The GD ripple is a parameter that reflects the fluctuation level of the group delay in the flat part. Its definition formula is shown in Equations (9) and (10).

$$GD\ ripple = \frac{|GD\ fluctuation/2|}{|\tau_1| + |GD\ fluctuation/2|} \tag{10}$$

5. CONCLUSIONS

In this study, a theoretical analysis was conducted on the proposed π-type circuit, and the generation formulas for various parameters were derived. Subsequently, the influence of each component value on the circuit performance was analyzed and discussed in detail. After the evaluation, a set of values was selected to design and fabricate the physical circuit. Through measurements, it was found that the proposed circuit better balances the relationships among the NGD value, NGD bandwidth, and flatness. The measurement results are consistent with the theoretical design. Compared with other previously proposed flat NGD circuits, this design exhibits a better comprehensive performance. It exhibits favorable NGD performance and can better counteract the positive group delay of other modules in the system link. The flat group delay characteristic avoids the phase distortion of different frequency components, thereby ensuring the integrity of the signal waveform during transmission. The addition of NGD can further optimize the alignment of signals in the time domain, reducing inter-symbol interference, which is particularly crucial in high-speed data transmission. Meanwhile, the flat NGD characteristic indicates that the performance is consistent within the target frequency band, eliminating the need for complex adjustments for different frequencies and simplifying the system design. It should be noted that the practical implementation of the proposed NGD circuit may be affected by component tolerances and PCB fabrication errors. Future work will investigate the sensitivity of the design to these non-idealities and explore robust optimization techniques to ensure reliable performance in real-world applications.

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