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Microstrip Dual-Frequency Voltage Doubling Rectifier Circuit

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ABSTRACT: We present a microstrip dual-frequency rectifier circuit, which includes a voltage-doubling rectifier circuit, a sector-shaped dual-frequency harmonic suppression network, and a Π-shaped dual-frequency impedance matching network. Four fan-shaped microstrip stubs were utilized to suppress the fundamental and higher-order harmonics in the two frequency bands. A microstrip line is employed to form a Π-shaped impedance matching network to achieve impedance matching in both frequency bands. The measured results show that at the input power of 15 dBm, the rectification efficiencies are 50% and 43% at frequencies of 2.45 GHz and 5.80 GHz, respectively. This dual-frequency rectifier circuit can be applied to scenarios such as powering passive RFID tags and IoT sensors.

1. INTRODUCTION

With the rapid development of 5G communication, the Internet of Things (IoT), and wireless sensor networks, diversified power consumption environments have attracted considerable attention for wireless energy transmission technology [1]. As an advanced wireless charging technology, microwave wireless power transfer (WPT) can significantly improve the power-supply limitations of IoT devices. The rectifier circuit plays a crucial role as the core component of microwave wireless transmission and reception energy systems [2]. The rectifier circuit converts the received RF energy into usable directcurrent (DC) power. The key performance indicators of rectifier circuits include radio frequency (RF) to DC power conversion efficiency, bandwidth, and input power range. To improve the conversion efficiency of rectifier circuits and enhance output stability, it is necessary to focus on improving circuit impedance matching and suppressing high-order harmonics [3]. Given the nonlinear characteristics of rectifier circuits, designing a rectifier circuit that combines high efficiency and multiband coverage capability presents certain technical challenges.

Common harmonic suppression networks include Class C [4], Class F [5, 6], and inverse Class F rectifier circuits [7]. Yue et al. [8] used a microstrip line cascade structure to achieve three frequency harmonic suppression, and the rectifier circuit had an RF to DC power conversion efficiency of over 70% at the three frequency bands of 0.915, 2.45, and 5.80 GHz. Zheng et al. [9] utilized three fan-shaped microstrip structures to suppress harmonics and achieved a rectification efficiency of 60.2%. Bui et al. [10] proposed a reverse F-class dual frequency rectification circuit, which achieved conversion efficiencies of 64.5% and 64.2% at 2.32 GHz and 3.48 GHz, respectively, with an input power of 5 dBm. Wu et al. [11] achieved impedance matching in the 2–3 GHz broadband range using a three-stage multilevel transmission line. Halimi et al. [12] employed half wavelength microstrip lines to achieve impedance matching in dual frequency bands. Mansour and Kanaya [13] proposed a matching circuit based on an L-shaped cross-section, which had a conversion efficiency of over 30% in the range of 0.87–2.5 GHz and a measured efficiency of 63% in the range of 1.1–1.35 GHz. In this article, we design a dual-frequency rectification circuit that operates at 2.45 GHz and 5.80 GHz using a $\lambda/4$ harmonic suppression network combined with an impedance matching network.

2. DESIGN METHODOLOGY AND SIMULATION

Figure 1 illustrates the schematic of the designed rectifier circuit, which consists of a signal source, dual-frequency impedance matching network, a voltage-doubler rectifier, a dual-frequency harmonic termination network, and DC load. The rectification part of the circuit uses a double-voltage topology structure to ensure a high rectification efficiency and DC output voltage. The rectifier diode adopts an HSMS268C Schottky diode, and the capacitor adopts a GRM18 1000 pF Murata series surface mount capacitor. The load of the circuit adopted a surfacemount resistor with $R_L = 900\,\Omega$. The dielectric substrate of the circuit was made of an FR4 board with a dielectric constant of 4.4, loss tangent of 0.002, and thickness of 1.6 mm.

Due to the nonlinearity of the diodes, the high-order harmonics generated at the output end have high energy, which affects the output voltage stability. Therefore, a dual-frequency harmonic suppression network needs to be installed between the diode and load. The input impedance of the diode varies with the frequency. To match the 50 Ω impedance of the rectifier circuit with the feeder at both operating frequencies, a dual-frequency impedance-matching network was arranged between the feeder and rectifier structure. The dual-frequency harmonic suppression network consists of four fan-shaped branches and a 1/4 wavelength microstrip line. Four fan-shaped stubs were used to suppress two operating frequency bands and their second harmonics, and the opening angles of all four fan-shaped

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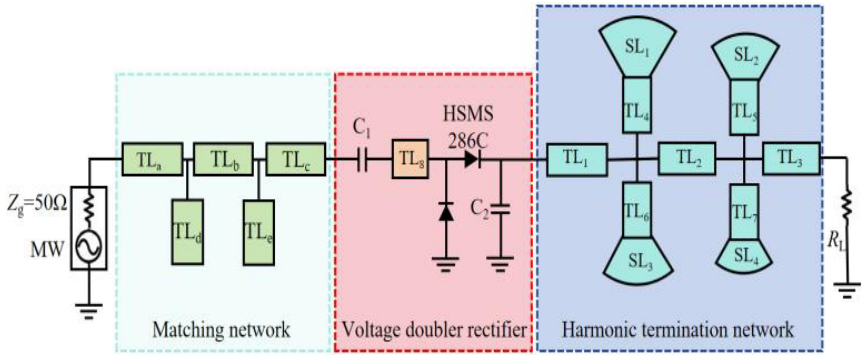

FIGURE 1. Schematic of the proposed rectifier.

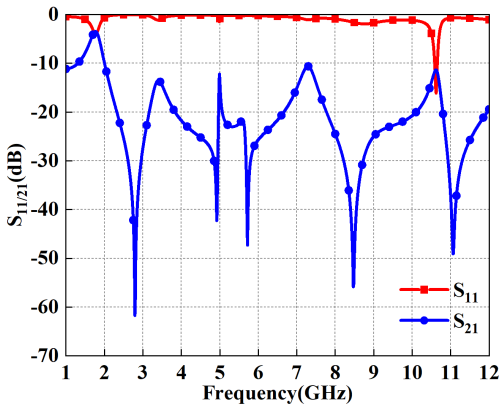

FIGURE 2. S-parameters of harmonic termination network.

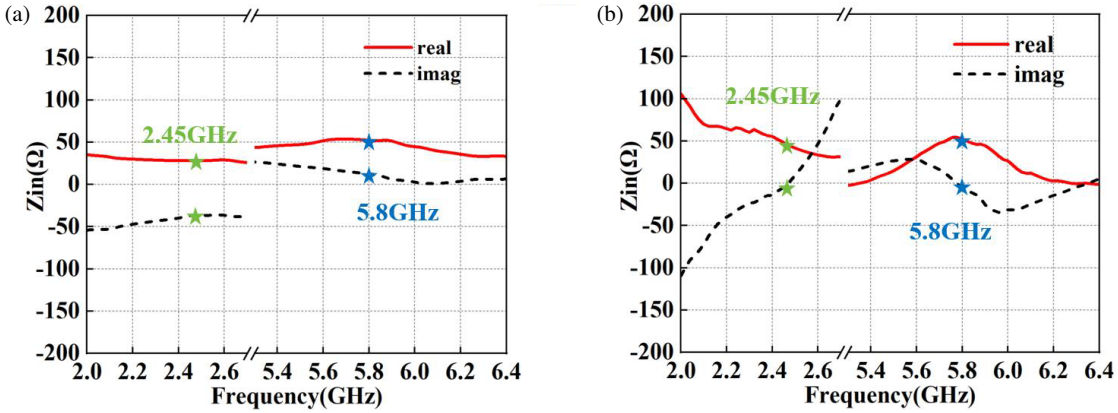

FIGURE 3. (a) Input impedance after connecting the double-voltage rectification structure. (b) Input impedances after loading the dual-frequency impedance-matching network.

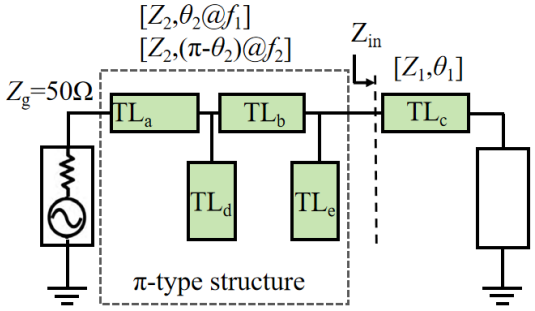

FIGURE 4. Schematic of the proposed harmonic termination network.

branches were 70°. Figure 2 shows the S-parameter curve of the dual-frequency harmonic suppression network. At the fundamental (2.45 GHz and 5.80 GHz) and second harmonic (4.90 GHz and 11.60 GHz) signals in the target frequency band, the S_{21} parameters reached −23.76 dB, −29.93 dB, −35.46 dB, and −24.24 dB, respectively. The S_{21} parameters of the four important frequency points are all less than −20 dB, effectively suppressing the fundamental frequency and second-harmonic signals. The input impedance, after connecting the double-voltage rectification structure to the dual-frequency harmonic suppression network and load, is shown in Figure 3(a). The input impedances in the 2.45 GHz and 5.80 GHz frequency bands are $(28.34 - \mathrm{j}36.92)\,\Omega$ and $(52.29 + \mathrm{j}12.54)\,\Omega$, respectively. The designed dual-frequency impedance-matching network is illustrated in Figure 4. Initially, a microstrip line TLc is added in front of the diode, and by adjusting the parameters of microstrip line TLc, the input impedances $Z_{\mathrm{in1@2.45\,GHz}}$ and $Z_{\mathrm{in1@5.80\,GHz}}$ of the rectifier circuit at the two target frequency points are tuned to be conjugated. Using microstrip lines TL$_a$ and TL$_b$ with the same characteristic impedance at both frequency points and complementary electrical lengths, and simultaneously loading parallel branches TL$_d$ and TL$_e$ to form a Π-shaped impedance-matching network, impedance-matching is achieved. After loading the dual-frequency impedance-matching network, the input impedances of the rectifier circuit at the 2.45 GHz and 5.80 GHz frequency bands are $(48.96 - \mathrm{j}2.33)\,\Omega$ and $(51.61 - \mathrm{j}4.37)\,\Omega$, respectively, as displayed in Figure 3(b). The dual-frequency impedance-matching network enables the rectifier circuit to achieve 50 Ω impedance-matching in both frequency bands.

The relationship between the S_{11} parameter and rectification efficiency of the circuit as a function of frequency was simulated using the advanced design system (ADS) software, as shown in Figure 5. According to Figure 5(a), the reflection coefficients of the proposed circuit at 2.45 GHz is −22.12 dB, and the reflection coefficient at 5.80 GHz is −21.91 dB, with −10 dB bandwidths of 2.12–2.54 GHz and 5.48–6.14 GHz, respectively. Figure 5(b) indicates that the rectification efficiency

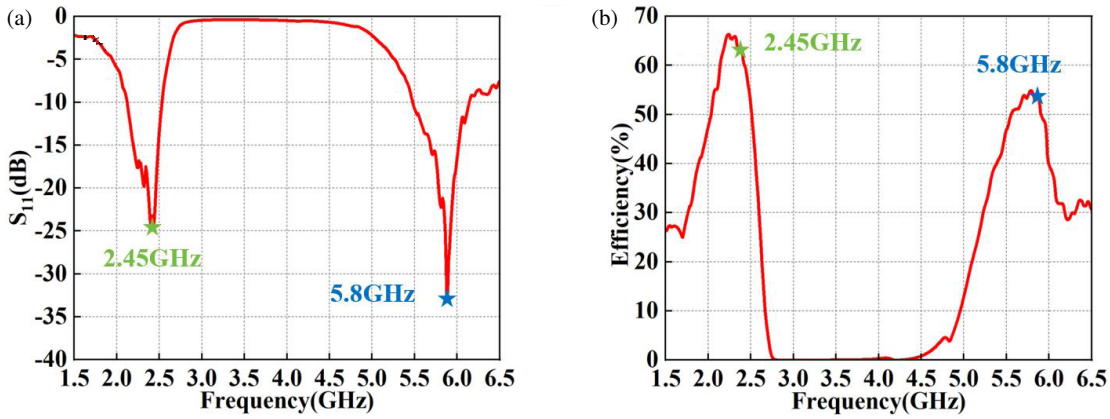

FIGURE 5. (a) Variation of S_{11} with frequency. (b) Variation of rectification efficiency with frequency.

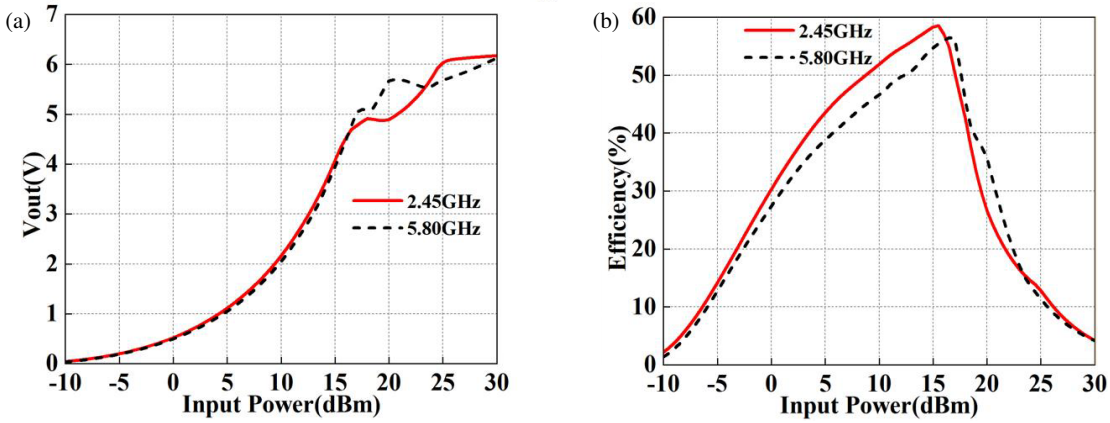

FIGURE 6. (a) Variation of output voltage with input power. (b) Variation of rectification efficiency with input power.

of the circuit is 58.31% at 2.45 GHz and 54.69% at 5.80 GHz, with 50% rectification efficiency of 2.04–2.51 GHz and 5.56–5.90 GHz, respectively. Obviously, the dual-frequency rectification circuit exhibits good matching performance at both 2.45 GHz and 5.80 GHz frequency points.

The simulation results show that the output voltage of the 2.45 GHz and 5.80 GHz frequency bands at an input power of $-10 \sim 30$ dBm is shown in Figure 6(a). The output voltages in both frequency bands show an overall upward trend with increasing input power, with a faster increase at $-10 \sim 15$ dBm and stabilization after 15 dBm. At 15 dBm, the output voltage is 4.1 V for both bands. Figure 6(b) shows that the rectification efficiency of the circuit in the two frequency bands first increases and then decreases with an increase in the input power, reaching a peak of nearly 60% near 15 dBm. After exceeding 15 dBm, the rectifier diode may be damaged because the output voltage exceeds the breakdown voltage, resulting in a decrease in the rectification efficiency.

3. IMPLEMENTATION AND MEASUREMENT RESULTS

We fabricated and tested an optimized dual-frequency rectification circuit, using 1.6 mm pitch SMA RF connectors for the feeding line. The layout and detailed dimensions of the designed dual-frequency rectification circuit are shown in Figure 7(a). The fabricated rectifier circuit is illustrated in Figure 7(b). The RF power signal used for testing was generated by an Agilent N5181A signal generator, and the DC voltage at the output end is measured using a multimeter. The rectification efficiency is calculated by measuring the voltage across the output resistance with a multimeter. The formula for calculating the RF-DC conversion efficiency of the rectifier circuit is $\eta_{RF-DC} = \frac{P_{DC}}{P_r} = \frac{V_{DC}^2}{R_L P_r} \times 100\%$, where V_{DC} and R_L represent the DC output voltage and load value of the rectifier circuit, respectively, and P_{DC} and P_r denote the DC power output of the rectifier circuit and RF power from the signal generator, respectively. The S-parameters of the rectifier circuit were tested using an Agilent N5230C vector network analyzer, and the results are shown in Figures 2, 5, and 8.

TABLE 1. Comparison with some prior rectifiers.

Ref.	Frequency (GHz)	Input Power (dBm)	Max efficiency	Size (λ^2)
12	2.45, 5.80	0	51.8% 39.7%	0.39×0.49
14	3.50, 5.80	5	54.5%, 41.2%	0.87×0.29
This work	2.45, 5.80	15	50%, 43%	0.77×0.32

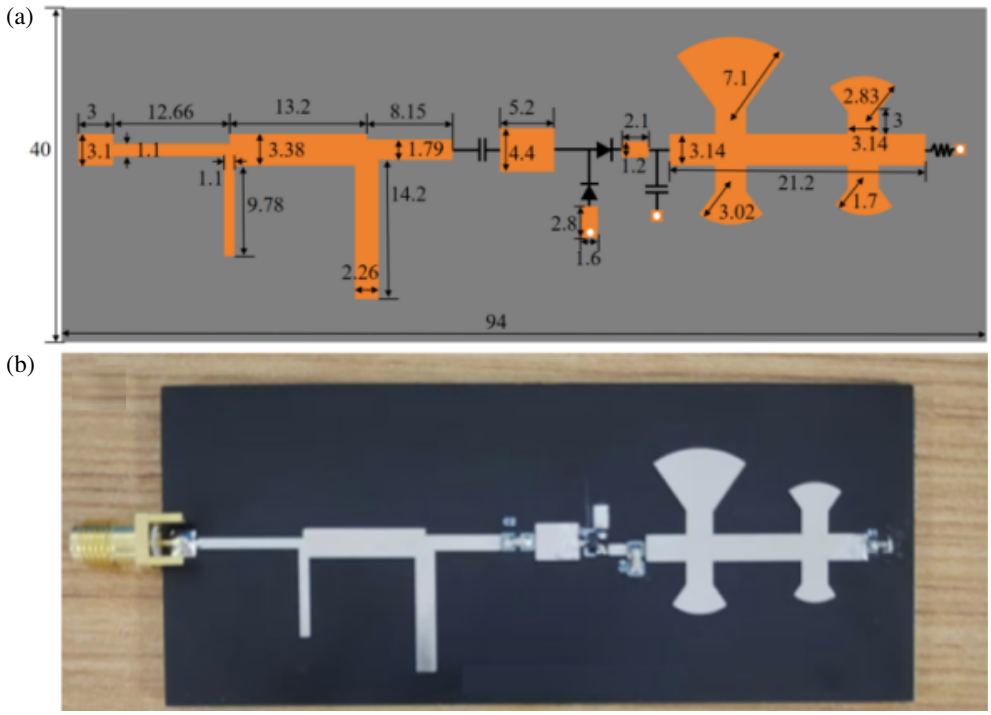

FIGURE 7. (a) Layout (Unit: mm). (b) Photograph of the proposed rectifier (Manufacturing process used for the prototype is CNC milling).

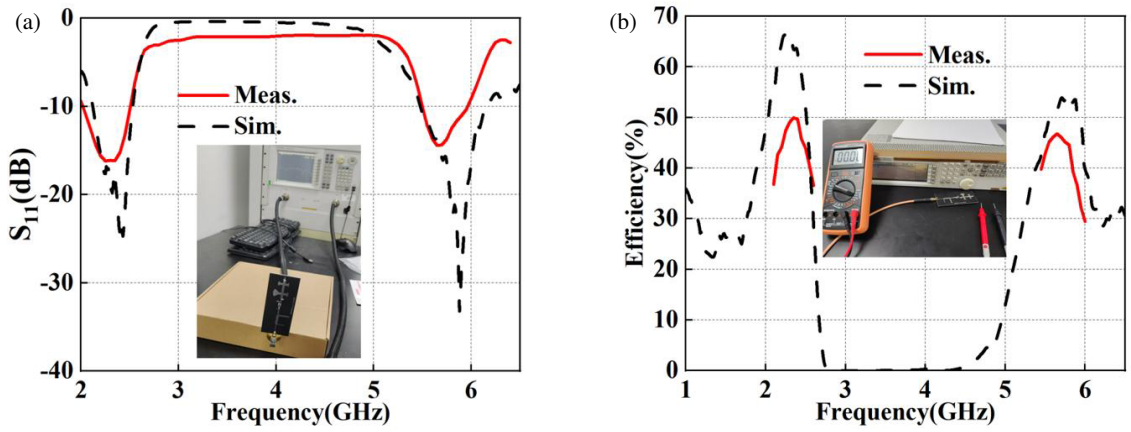

FIGURE 8. (a) Measured and simulated S_{11} parameters. (b) Measured and simulated RF-DC conversion efficiencies at 15 dBm input power.

Figure 8(a) shows the simulated and measured S_{11} parameters of the rectifier circuit with a -10 dB bandwidth of $2.03 \sim 2.51$ GHz and $5.49 \sim 5.97$ GHz, respectively. We can find that the S_{11} parameters are -13.26 dB at 2.45 GHz and -12.67 dB at 5.80 GHz. The simulated and measured conversion efficiencies are shown in Figure 8(b). Under the condition of an input power of 15 dBm, the rectification efficiencies are 50% at 2.45 GHz and 43% at 5.80 GHz, respectively. There were some slight deviations between the test and simulation results, which were mainly caused by processing and testing errors. A performance comparison between the designed rectifier circuit in our work and the rectifier reported in the existing literature is shown in Table 1. Compared with the rectifier circuits in [12, 14], the proposed rectifier circuit has a higher efficiency in the high-frequency band (5.80 GHz).

4. CONCLUSION

We have designed a microstrip dual-band voltage-doubling rectifier circuit, which employs a fan-shaped dual-band harmonic suppression network to suppress high-order harmonics in two operating frequency bands, and a π-shaped impedance matching network was designed to match the impedance at dual frequency bands and improve rectification efficiency. The actual test results show that the maximum rectification efficiency of the proposed rectifier reaches 50% and 43% at frequencies of 2.45 GHz and 5.80 GHz, respectively. The designed rectifier circuit is small and inexpensive, and can be used for microwave wireless energy transmission applications.

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