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A Compact Two-Layer Diplexer with High Isolation Using a Hybrid Filtering Approach for 5G Co-Site Applications

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ABSTRACT: This paper presents a compact two-layer diplexer based on a vertically stacked architecture with hybrid filtering, in which a dual-band bandpass power divider (PD) is integrated with low-pass (LPF) and high-pass filters (HPF). The design utilizes a double-layer dielectric substrate: the upper layer integrates a dual-band bandpass filter (BPF) and a Wilkinson PD, while the lower layer incorporates low-pass and high-pass filtering sections. Metallized vias and impedance-matching networks are employed to enable tight inter-layer coupling and ensure excellent electrical performance within a miniaturized footprint. The results indicate that the proposed diplexer achieves insertion losses below 4 dB and 4.5 dB in the two passbands (3.4–3.8 GHz and 4.7–5.0 GHz), respectively (including the inherent 3 dB loss of the power divider), input return losses exceeding 13 dB and 11 dB, respectively, approximately 45 dB out-of-band rejection at $\pm$400 MHz from the passband edges, and inter-port isolation better than 30 dB. These characteristics satisfy the stringent requirements for multi-band co-site operation in 5G base stations and terminal devices.

1. INTRODUCTION

The rapid deployment of fifth-generation (5G) wireless systems has driven radio frequency (RF) front-ends toward unprecedented levels of integration, miniaturization, and multi-band functionality [1]. Within this context, diplexers — critical components that enable simultaneous transmission and reception by isolating distinct frequency channels — must deliver not only high selectivity and low insertion loss but also robust inter-band isolation and compatibility with other RF building blocks, such as filters and power dividers (PD) [2].

Conventional high-performance diplexers often rely on non-planar architectures, including waveguide cavities [3, 4] and high-temperature superconducting (HTS) resonators [5, 6]. Although these technologies offer ultra-high quality factors (Q), their bulky form factors, fabrication complexity, and HTS-cryogenic operational requirements render them impractical for mass-deployed 5G user equipment and compact base stations. Alternative miniaturized solutions based on surface acoustic wave (SAW) [7] or low-temperature co-fired ceramic (LTCC) [8] platforms provide moderate integration but suffer from limited Q factors and fabrication tolerances, resulting in compromised out-of-band rejection and elevated insertion loss, particularly in the n77/n78/n79 sub-6 GHz 5G bands.

Planar microstrip implementations, commonly realized by cascading a T-junction PD with parallel bandpass filters (BPFs) [9–11], offer design simplicity but face fundamental scalability challenges at higher frequencies. As operational bands shift toward the upper sub-6 GHz and millimeter-wave ranges, such layouts exhibit excessive footprint, degraded isolation due to parasitic coupling, and insufficient stopband attenuation, hindering their suitability for dense RF front-end integration.

Recent efforts to overcome these limitations have explored advanced resonator topologies, such as rectangular open-loop resonators and multi-mode stub-loaded structures, to improve selectivity and suppression [12, 13]. Nevertheless, these approaches remain constrained to single-layer substrates, limiting opportunities for functional stacking and vertical signal routing [14–16]. In contrast, the advancement of multilayer printed circuit board (PCB) fabrication technologies and reliable vertical interconnects — particularly metallized through-vias — has enabled the multilayer integration of RF passive components [17–20]. This paradigm facilitates concurrent optimization of electrical performance and physical compactness by distributing functional blocks across multiple substrate layers.

Building upon this trend, we propose a compact two-layer diplexer based on a vertically stacked hybrid filtering architecture, specifically tailored for dual-band 5G co-site operation in the n78 (3.3–3.8 GHz) and n79 (4.4–5.0 GHz) bands. The architecture employs a double-layer dielectric substrate: the upper layer integrates a dual-band BPF with a second-order Wilkinson PD, while the lower layer hosts dedicated low-pass and high-pass filtering sections that replace conventional bandpass branches. Vertical signal transfer between layers is achieved via impedance-engineered metallized vias, and a tailored matching network ensures broadband input/output matching across both passbands. This co-design strategy enables a footprint of only 32.56 mm $\times$ 22 mm while achieving $>$ 30 dB port isolation, $<$ 4.5 dB insertion loss, and 45 dB out-of-band suppression-performance metrics that align with stringent 5G infrastructure requirements.

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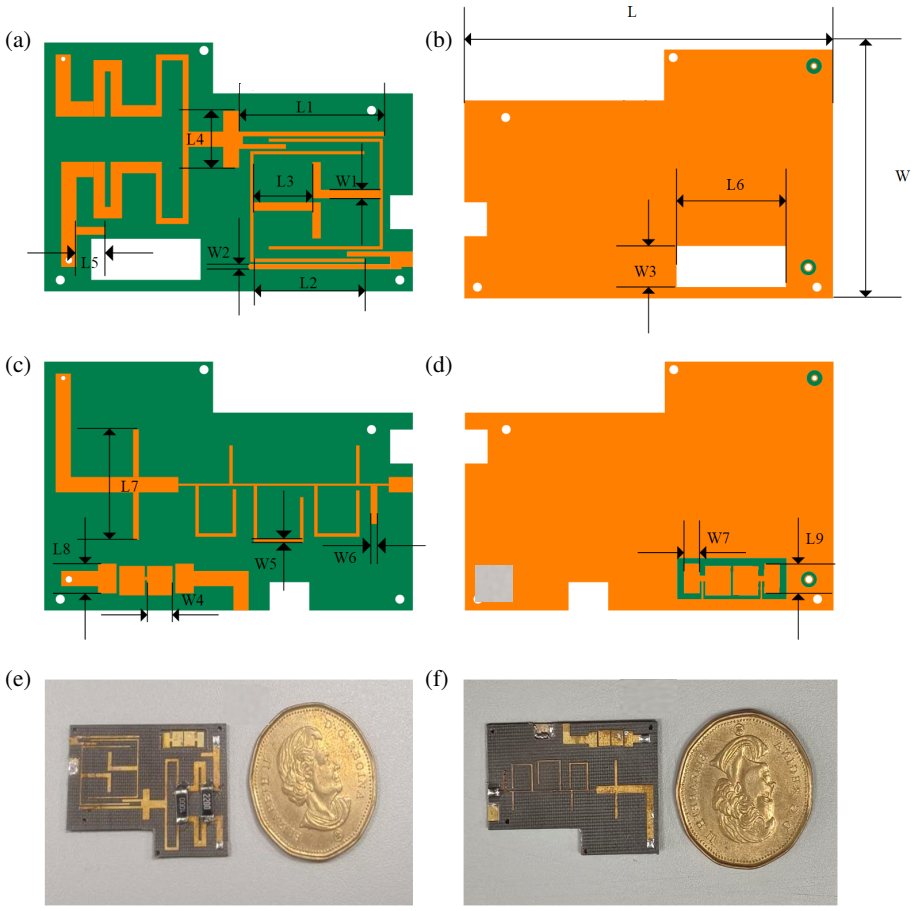

FIGURE 1. Layout and fabricated prototype of the proposed diplexer. (a) Top and (b) bottom metal layers of the upper substrate (Sub1), integrating the dual-band BPF and Wilkinson PD. (c) Top and (d) bottom metal layers of the lower substrate (Sub2), housing the LPF and HPF. (e) Front and (f) back photographs of the prototype.

2. CONFIGURATION AND RESULTS

The proposed diplexer employs a vertically stacked substrate architecture to form a compact two-layer RF front-end diplexer based on hybrid filtering, as illustrated in Fig. 1. Unlike conventional diplexer designs that utilize two parallel BPFs, this work adopts a hybrid filtering strategy: a dual-band BPF combined with a Wilkinson PD is implemented on the upper substrate (set as Sub1), while dedicated low-pass (LPF) and high-pass (HPF) filters are integrated on the lower substrate (set as Sub2). This configuration enables efficient band separation using complementary filtering responses rather than duplicated bandpass paths, thereby reducing circuit redundancy and enhancing stopband rejection.

Both substrates have a relative permittivity $\varepsilon_r = 2.65$, loss tangent $\tan\delta = 0.002$, and individual thickness of 0.508 mm, resulting in a total stack height of 1.016 mm. A shared ground plane is maintained between the two layers to ensure a consistent reference potential across the entire structure. The overall footprint is 32.56 mm × 22 mm, and the fabricated prototype is shown in Figs. 1(e)–(f). The key dimensions (in mm) are: $L = 32.56$, $W = 22$, $L_1 = 12.84$, $L_2 = 9.8$, $L_3 = 5.2$, $L_4 = 5.03$, $L_5 = 2.56$, $L_6 = 9.66$, $L_7 = 9.76$, $L_8 = 2.63$, $L_9 = 2.6$, $W_1 = 0.75$, $W_2 = 0.425$, $W_3 = 3.63$, $W_4 = 2.25$, $W_5 = 0.3$, $W_6 = 0.6$, and $W_7 = 1.63$.

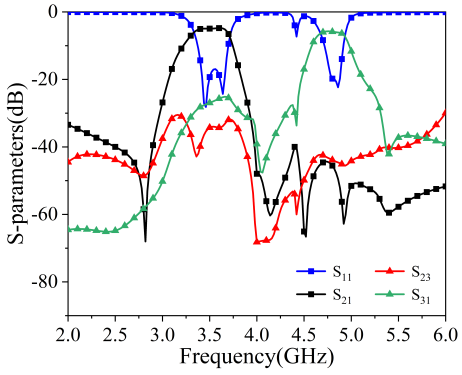

FIGURE 2. Simulated S-parameters of the diplexer. $|S_{21}|$ and $|S_{31}|$ represent transmission to the low-band and high-band output ports, respectively; $|S_{11}|$ denotes input return loss; $|S_{23}|$ indicates inter-port isolation.

On Sub1 (Figs. 1(a)–(b)), the dual-band BPF targets the 5G n78 and n79 bands, providing initial channel selection and out-of-band attenuation. The integrated second-order Wilkinson PD equally splits the filtered signal into two matched output paths with inherent isolation provided by lumped resistors.

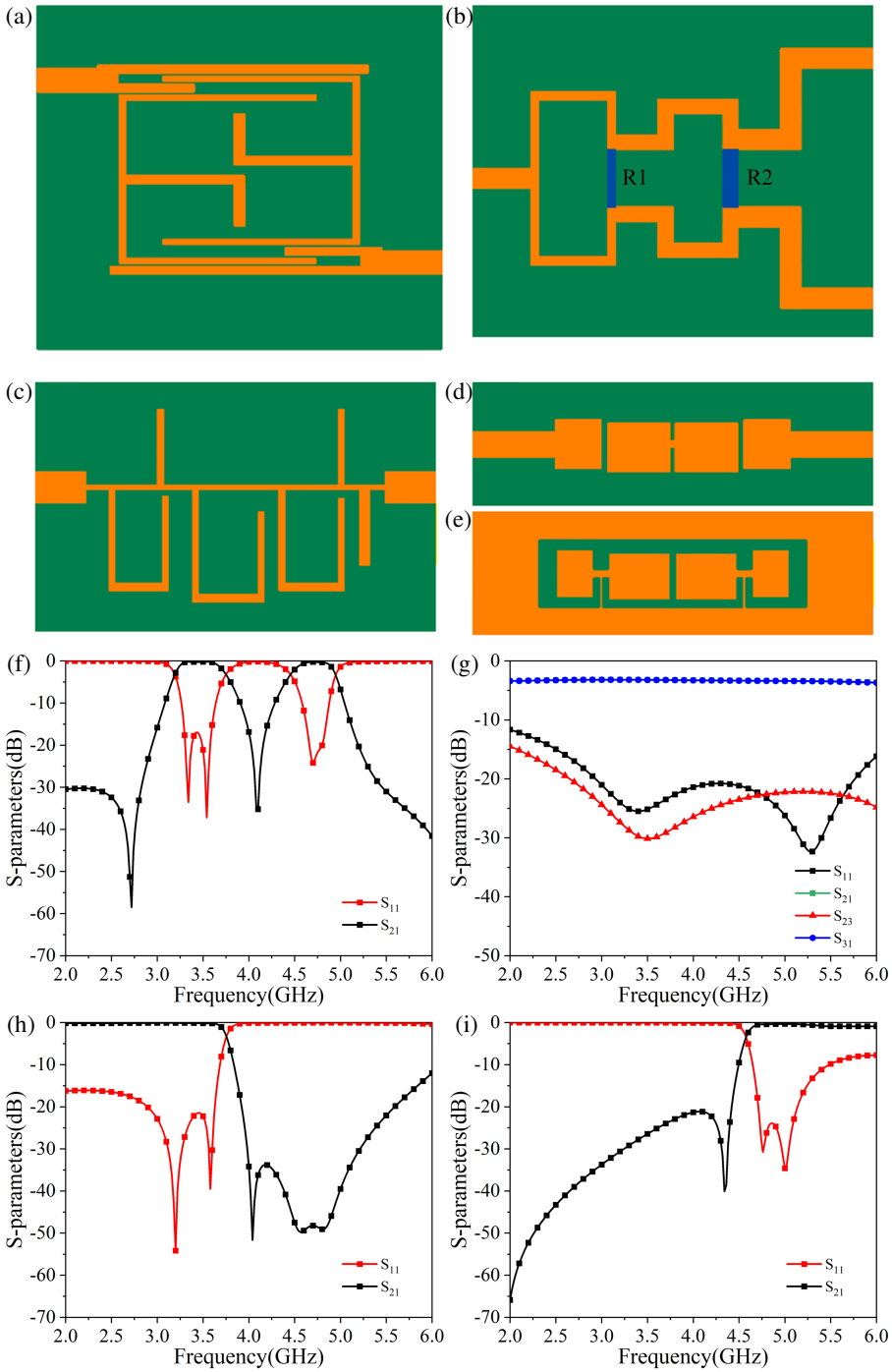

FIGURE 3. Layouts and simulated responses of the four constituent modules. (a) Dual-band BPF. (b) Second-order Wilkinson PD. (c) LPF. (d) Top and (e) bottom layers of the HPF incorporating coupled patches and a DGS. (f)–(i) Corresponding S-parameters.

Sub2 (Figs. 1(c)–(d)) hosts the LPF and HPF that further refine each branch. The LPF passes the lower band (n78) while suppressing frequencies above 3.8 GHz, including harmonics and out-of-band interference. Conversely, the HPF transmits the upper band (n79) and attenuates signals below 4.6 GHz. Together, they ensure clean and isolated dual-band outputs at their respective ports.

Inter-layer signal routing is accomplished through metallized through-vias connecting the PD outputs on Sub1 to the LPF and HPF inputs on Sub2. To avoid shorting to the common ground plane, anti-pad clearance rings of radius 0.7 mm are etched around each via location. The via radii are optimized to 0.2 mm for the LPF path and 0.3 mm for the HPF path.

Simulation results (Fig. 2) confirm the diplexer's performance: within the operating frequency bands of 3.3–3.75 GHz and 4.65–5.0 GHz, the insertion losses are less than 3.8 dB and 4.2 dB, respectively; the input return losses in both bands are greater than 15 dB; and the inter-port isolation is better than 30 dB. Moreover, stopband rejection reaches approximately 50 dB at offsets of ± 400 MHz from the passband edges, demon-

strating strong suppression of adjacent-channel interference, critical for co-site 5G deployments.

3. DESIGN PROCESS

As Fig. 3 shows, the diplexer is developed through a modular design approach, followed by co-optimization to address inter-stage impedance mismatches inherent in cascaded passive networks.

3.1. Dual-Band Bandpass Filter and Power Divider

A dual-band BPF targeting the 5G n78 and n79 bands is first synthesized using a pair of open-circuited stub-loaded resonators (Fig. 3(a)). Each resonator is tuned to one passband, while an interdigital coupled feed structure provides simultaneous and balanced excitation to both modes. This configuration enables sharp roll-off and deep out-of-band rejection without increasing circuit order. Simulation (Fig. 3(f)) confirms that this filter achieves good impedance matching and low insertion loss across the two operating bands of 3.3–3.8 GHz and 4.5–5.0 GHz.

To ensure equal power division across the dual-band spectrum, a second-order Wilkinson PD is integrated adjacent to the filter (Fig. 3(b)). The design employs two quarter-wavelength impedance-transforming sections and surface-mount isolation resistors. Simulated results (Fig. 3(g)) show consistent 3.0 ± 0.3 dB splitting from 3.3 to 5.0 GHz, with input/output return losses better than 20 dB and inter-output isolation above 25 dB-sufficient for subsequent filtering stages.

3.2. Low-Pass and High-Pass Filtering Sections

Rather than replicating bandpass responses, the lower-frequency branch is processed by a compact LPF and the higher-frequency branch by an HPF, as shown in Figs. 3(c)–(e).

The LPF adopts a meandered open-stub topology (Fig. 3(c)), which provides steeper transition and stronger harmonic suppression than conventional stepped-impedance designs. The meandering reduces the occupied area by approximately 35% without compromising electrical length. Simulation (Fig. 3(h)) shows < 0.8 dB insertion loss up to 3.8 GHz and > 50 dB rejection at 4 GHz.

The HPF (Figs. 3(d)–(e)) leverages a symmetric multi-layer structure combining coupled rectangular patches, series inductive lines, and a complementary split-ring defected ground structure (DGS). The DGS introduces a transmission zero near 4.2 GHz, enhancing stopband attenuation below the n79 band. The vertical coupling between top and bottom patches improves passband flatness. As shown in Fig. 3(i), the HPF achieves < 1.0 dB insertion loss from 4.65 to 5.0 GHz and > 40 dB suppression at 4.3 GHz.

3.3. Integrated Matching Network Synthesis

Directly cascading the four independently optimized modules resulted in degraded input matching and elevated inter-port leakage due to cumulative impedance discontinuities. These discontinuities mainly arise from the filter-divider junctions, vertical via transitions, and heterogeneous loading conditions introduced by the LPF and HPF on the lower substrate. To resolve this issue, three open stubs — denoted as stub 1, stub 2, and stub 3 (Fig. 4) — were inserted: stub 1 at the input of the PD, stub 2 at the output port preceding the via to Sub2, and stub 3 at the output port following the via to Sub2. Specifically, stub 1 compensates the residual reactive mismatch introduced by the dual-band BPF-PD junction; stub 2 partially counteracts the inductive parasitics associated with the vertical via transition; and stub 3 further adjusts the impedance presented to the LPF and HPF on Sub2, thereby mitigating reflections caused by inter-layer coupling and filter loading.

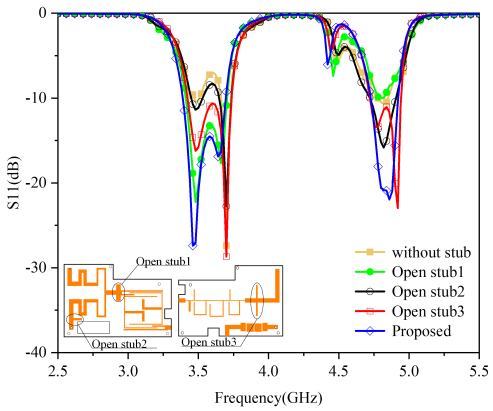

FIGURE 4. Simulation results of four structures with significant differences in S_{11} among the eight stub combinations.

An exhaustive parametric study evaluated all eight combinations of these stubs (without any stub, with only stub 1, only stub 2, only stub 3, stub 1 + stub 2, stub 1 + stub 3, stub 2 + stub 3, and stub 1 + stub 2 + stub 3). As summarized in Fig. 4, four of the eight stub combinations exhibit a pronounced impact on S_{11}, among which the configuration using all three stubs simultaneously achieves $|S_{11}|$ exceeding 15 dB across both passbands, representing a 6–8 dB improvement compared with the unmatched case. This result indicates that the three stubs collectively form a distributed matching network that compensates the cumulative reactive effects introduced by the two-layer vertically stacked architecture, rather than relying on a single localized matching element.

4. VERIFICATION AND COMPARATIVE ANALYSIS

The fabricated prototype of the designed diplexer was subjected to physical testing. The device under test and measurement setup are shown in Fig. 5(a). Measurements were performed using a vector network analyzer. SMA-K connectors with a characteristic impedance of 50 Ω and an operational frequency range of DC-6 GHz were used during testing. The resistors employed were surface-mount components of the 2010 package type (nominal resistance: $R1 = 100\,\Omega$, $R2 = 220\,\Omega$).

Figures 5(b) to (d) compare the measured and simulated S-parameters. The measured passbands are centered at 3.6 GHz and 4.85 GHz, with 3-dB bandwidths of 3.4–3.8 GHz (11.1%) and 4.7–5.0 GHz (6.2%). The measured S_{21}, which repre-

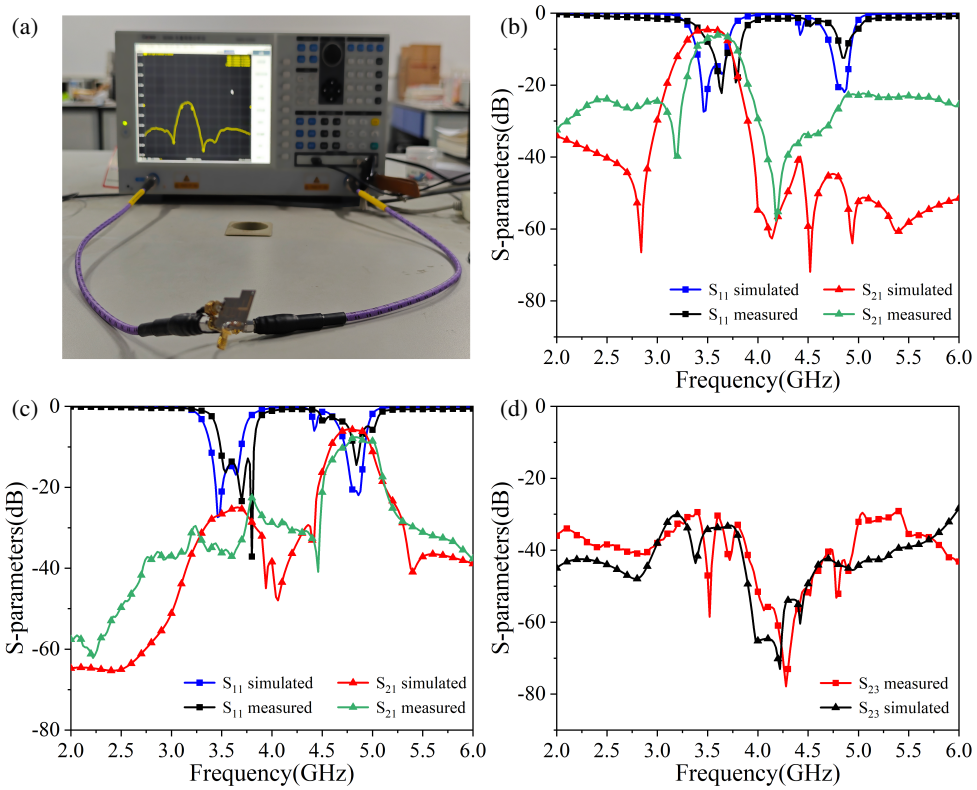

FIGURE 5. Measured and simulated performances of the fabricated diplexer. (a) Measurement setup. (b) S-parameters of the low-frequency output port. (c) S-parameters of the high-frequency output port. (d) Isolations.

sents the insertion loss, reaches 4 dB and 4.5 dB in the two bands, respectively, (including the inherent 3 dB loss of the power divider as well as the additional circuit loss), which are slightly higher than the simulated values but remain superior or comparable to most reported diplexer implementations. In particular, compared with single-layer planar integrated structures (e.g., Ref. [10], which reports total insertion losses of 4.8 dB/4.8 dB, corresponding to additional circuit losses of approximately 1.8 dB/1.8 dB), the proposed architecture achieves a comparable or even lower excess loss of 1.0–1.5 dB while simultaneously realizing a significantly higher level of functional integration, including a bandpass filter, power divider, low-pass filter, and high-pass filter (BPF + PD + LPF + HPF). Furthermore, the isolation between the output ports ($|S_{23}|$) exceeds 30 dB within the passbands, and the out-of-band rejection shows a sharp roll-off characteristic, both of which are critical for co-site operation.

Slight deviations from the simulated results are observed in terms of return loss level and passband edges, which can be attributed to practical non-idealities associated with the multilayer implementation. In particular, the metallized through-vias introduce additional parasitic inductance and capacitance that are difficult to fully capture using idealized via models, especially at the higher-frequency band. Minor layer-to-layer misalignment and substrate thickness tolerances during PCB fabrication may also slightly affect the effective electrical lengths of critical transmission lines, leading to small shifts in the measured passband edges. In addition, the SMA connector transitions and soldering interfaces, which are not included in the full-wave simulations, introduce extra discontinuities that predominantly influence the measured return loss. Despite these non-ideal effects, the measured responses preserve the overall filtering characteristics predicted by simulation, indicating good robustness of the proposed design under practical implementation conditions.

Beyond absolute performance metrics, the proposed two-layer hybrid architecture exhibits favorable stability against fabrication-related uncertainties. Unlike conventional single-layer diplexers that rely on tightly coupled in-plane resonant elements and parallel bandpass branches, the present design distributes the filtering and power-division functions across two substrate layers. This vertical functional partitioning mitigates the accumulation of sensitivity to local fabrication variations, such as line-width deviations and etching tolerances, which often leads to pronounced passband distortion or isolation degradation in single-layer implementations. Moreover, by replacing duplicated bandpass branches with complementary low-pass and high-pass filtering paths, the proposed architecture avoids high-sensitivity multi-resonant junctions that are particularly vulnerable to fabrication imperfections. As a result, the measured performance demonstrates stable passband characteristics and high port isolation, indicating improved fabrication tolerance compared with conventional single-layer designs.

A comprehensive performance comparison between the proposed diplexer and several recent state-of-the-art designs is summarized in Table 1. Unlike the referenced works, which primarily rely on sophisticated single-layer planar topologies, such as T-junctions with bandpass filters (BPFs) [10, 16], multi-

TABLE 1. Comparison of the diplexer in this work with those in the references.

Refs.	Center Freq. (GHz)	Insertion Loss (dB)	Isolation (dB)	Size ($\lambda_g \times \lambda_g$)	Integration/Filtering Scheme
[10]	1.8/2.4	4.8/4.8	> 20	N/A	Single-layer, PD + BPF
[13]	2.14/2.84	$< 1.19/1.42$	> 25	2.11×0.68	Single-layer, BPF + Multi-Resonant Junction
[15]	6.9/9.1	$< 1/< 2$	> 15	1.03×0.8	Single-layer, BPF + EBG + Notch Filters
[16]	3.5/5	$< 3.9/< 4.9$	> 8	0.35×0.27	Single-layer, PD+BPF
This work	3.6/4.85	$< 4/< 4.5$	> 30	0.42×0.62	Two-layer, BPF + PD + LPF + HPF

resonant junctions [13], or electromagnetic bandgap (EBG) structures with notch filters [15], the proposed diplexer introduces innovation through the vertical stacking and integration of different filter classes, including a BPF, PD, LPF, and HPF. This unique "bandpass-power-division-high/low-pass" architecture not only achieves a highly compact structure but also provides superior port isolation (> 30 dB) and enables excellent out-of-band suppression by fundamentally replacing the conventional dual-bandpass channelizer. The measured results confirm that this two-layer hybrid approach successfully meets the stringent requirements for size-constrained, multi-band co-site applications in 5G systems.

5. CONCLUSIONS

This paper has presented the design, fabrication, and characterization of a compact two-layer diplexer for 5G co-site applications in the n78 and n79 bands. By adopting a vertically stacked two-layer substrate architecture, the proposed topology integrates a dual-band BPF and a Wilkinson PD on the upper layer, while employing dedicated LPF and HPF on the lower layer to achieve band separation — eliminating the need for two parallel bandpass branches. Vertical interconnection is realized through impedance-engineered metallized vias, and a co-designed microstrip matching network ensures broadband input matching across both operational bands.

The fabricated prototype occupies a compact footprint of only 32.56 mm $\times$ 22 mm. The measured results indicate passbands of 3.4–3.8 GHz and 4.7–5.0 GHz, where the insertion losses are less than 4 dB and 4.5 dB, respectively, and the inter-port isolation exceeds 30 dB. A stopband rejection of approximately 45 dB is achieved at ± 400 MHz from the passband edges. The close agreement between simulation and measurement validates the effectiveness of the two-layer vertical integration strategy. This work provides a practical and scalable solution for highly integrated RF front-ends in 5G base stations and multi-band terminal devices.

Although the proposed diplexer already achieves a compact footprint through vertical functional partitioning, further miniaturization remains feasible. Benefiting from the design flexibility provided by the two-layer architecture, additional size reduction can be realized through deeper functional integration and more compact multilayer folding layouts. Moreover, the use of substrates with higher dielectric constants offers an effective approach to further reducing the overall size without compromising isolation performance.

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