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Design of an Ultra-Wideband LDMOS Power Amplifier Based on a Two-Stage Harmonic Suppression Network

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ABSTRACT: This study proposes an improved output matching design technique based on a two-stage harmonic suppression network, with the core innovation being a hybrid matching mode combining microstrip lines and lumped-parameter components in output matching. In the first-stage harmonic suppression network, a third-order Butterworth filter served as the prototype. Utilizing the Richards transformation and Kuroda rule, it is converted to a cross-shaped microstrip line, achieving high-frequency matching while suppressing second-harmonic components. The second-stage harmonic suppression network employs two series-connected LC resonant circuits to suppress the third- and fifth-harmonics. To broaden the bandwidth and enhance the circuit stability, an improved negative feedback structure based on a second-order Butterworth low-pass filter prototype was introduced. Practical circuit testing within the 0.4–1.2 GHz operating bandwidth demonstrated an output power ranging from 40.1 to 41.3 dBm and drain efficiency exceeding 51.63%, robustly validating the effectiveness of this approach.

1. INTRODUCTION

In the era of rapid advancements in wireless communication technology, radio frequency power amplifiers have become one of the core components in modern communication systems, playing a crucial role in the performance of communication links [1]. With the widespread adoption of 5G technology and the gradual advancement of 6G technology, communication systems are increasingly demanding low power consumption, high bandwidth, and low latency. Their performance directly affects the system energy efficiency, transmission quality, and equipment cost of signals, imposing higher requirements on the design of RF power amplifiers [2–4].

Harmonic suppression technology has remained a significant and popular research focus for operating across a wide bandwidth range. Numerous studies have proposed broadband power amplifier designs based on harmonic suppression networks. In [5–15], various power amplifier topologies were proposed to achieve high efficiency and harmonic suppression performance. Refs. [13, 14] designed a broadband power amplifier based on second-harmonic impedance control, where the proposed method starts from the inverse Class F mode and extends it to a series of modes. Ref. [7] employed a fifth-order Chebyshev filter, utilizing an odd-even mode group analysis method for filter computation; however, this design only considers fundamental impedance matching. Ref. [15] proposed a design method for a high-efficiency continuous Class-F power amplifier using a quasi-elliptic low-pass filter matching network, whose passband can be adjusted according to the operating frequency band, with harmonics controlled via a wide stopband structure. Ref. [16] proposed a combined design scheme for a second-harmonic-tuned broadband power amplifier and branch-loaded parallel-coupled line microstrip bandpass filter, achieving impedance matching only for the fundamental and second harmonics.

Based on the reviewed literature, it can be observed that some designs incorporate theoretically innovative improvements to the amplifier impedance design, enabling bandwidth expansion. However, many still cannot fully overcome bandwidth limitations within an octave range because of the difficulty in overlapping high-order harmonics in the low-frequency band with fundamental waves in the high-frequency band [17, 18]. Some approaches combine filter structures with power amplifiers to enhance overall efficiency and reduce the design footprint. However, the filter structures employed are sometimes complex and fail to adequately address the requirements for a wide bandwidth and flatness performance [16, 19]. Therefore, designing a broadband power amplifier capable of effectively suppressing higher-order harmonics while further optimizing the design process and innovating the design concepts holds significant theoretical importance and practical application value.

Through circuit simulation using Keysight Advanced Design System (ADS) software, efficient output is achieved across the 0.4–1.2 GHz frequency range under operating conditions of 28 V drain voltage and 2.3 V gate voltage. Within the operational bandwidth, the amplifier demonstrated significant suppression of the second, third, and fifth harmonics. This design is important for civilian wireless communications, medium-to-low-orbit satellite communications, and industrial applications.

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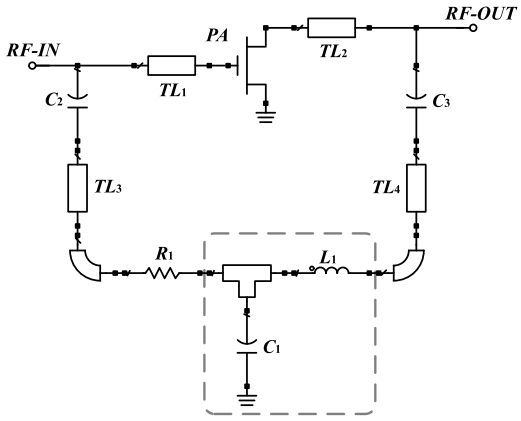

FIGURE 1. Negative feedback network based on a Butterworth filter.

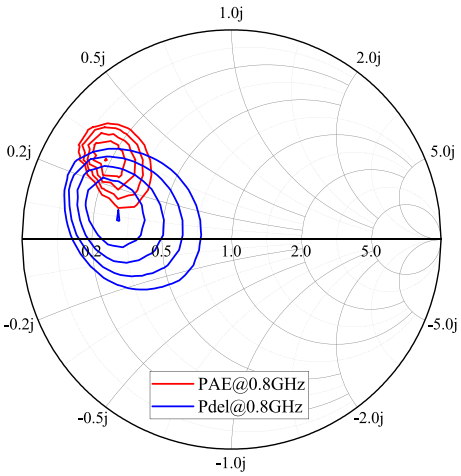

FIGURE 2. Smith chart trajectories at 0.8 GHz.

2. NEGATIVE FEEDBACK STRUCTURE BASED ON A BUTTERWORTH FILTER

The core principle of feedback structures is to utilize the filter's performance at different frequencies to suppress the characteristics around the center frequency, compensating for deviations away from the center frequency. This flattens the overall performance of the amplifier and expands the bandwidth. This design employs a novel negative feedback structure, utilizing a Butterworth low-pass filter as the topological prototype for the feedback circuit design.

To ensure that the operating bandwidth of the power amplifier is fully covered by the filter's transition band, the filter's cutoff frequency is defined as 0.3 GHz, with the bandwidth fully encompassed by the filter's transition band.

The calculations yield $L = 22.5\,\text{nH}$ and $C = 9\,\text{pF}$. The design process commenced after determining the topological prototype of the feedback structure. Because the feedback structure bridges the gate and drain of the transistor, capacitors must be added at both ends to block the mutual interference between the DC currents. The final topological transformation process is illustrated in Fig. 1.

To determine the optimal output matching impedance of the power amplifier, Fig. 2 presents the Smith chart trajectories of the power (Pdel) contour and power-added efficiency (PAE) contour derived from load-pull analysis at the center frequency of the 0.8 GHz target band. By traversing the load impedance across the Smith chart, the optimal impedance point is selected within the overlapping region of the power and efficiency contours, ensuring sufficient output power while maintaining high efficiency. In this design, the optimal load impedance is chosen as $Z = 12.53 + \text{j}12.51\,\Omega$.

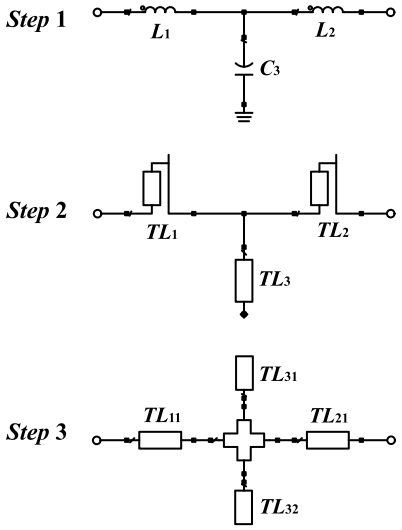

FIGURE 3. Transformation process of the first-order harmonic suppression network.

3. OUTPUT MATCHING STRUCTURE BASED ON A TWO-STAGE HARMONIC SUPPRESSION NETWORK

3.1. A Harmonic Suppression Network Based on Richards Transform and Kuroda Rule

As the operating frequency increases, distributed transmission lines such as microstrip lines are more suitable for power amplifier (PA) matching networks than lumped components. Lumped components suffer from serious parasitic effects and performance degradation near their self-resonant frequency (SRF). The increased losses also reduce the quality factor, output power, and efficiency of the PA. In contrast, microstrip lines feature stable performance, no obvious self-resonance, and can be flexibly designed to realize impedance matching and harmonic suppression.

To enable the power amplifier in this design to operate seamlessly across the ultra-wideband range of 0.4–1.2 GHz, the first stage harmonic suppression network employs microstrip lines for impedance matching. Fig. 3 illustrates the transformation process of the first-stage harmonic suppression network. Utilizing the Richards transformation and Kuroda's rule, along with ADS simulation software, the third-order Butterworth filter was converted into a cross-junction microstrip line. Richards transformation equates an open (short-circuited) transmission line segment to distributed inductive (capacitive) elements.

The core principle of Kuroda's rule is to perform equivalent transformations on circuit structures while preserving certain circuit characteristics (such as transmission characteristics and frequency response). Fig. 4 illustrates one of the four trans-

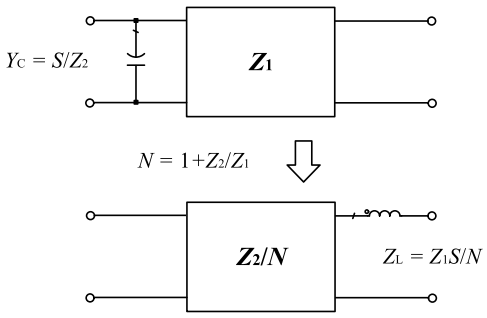

FIGURE 4. The transformation process of the Kuroda rule.

formation forms within Kuroda's rule: The $ABCD$ parameter matrix of the entire circuit equals the product of the $ABCD$ parameter matrices of each unit circuit. For the original circuit above, the $ABCD$ parameter matrix of the entire network is:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_L = \begin{bmatrix} 1 & 0 \\ \frac{S}{Z_2} & 1 \end{bmatrix} \frac{1}{\sqrt{1-S^2}} \begin{bmatrix} 1 & Z_1 S \\ \frac{S}{Z_1} & 1 \end{bmatrix} = \frac{1}{\sqrt{1-S^2}} \begin{bmatrix} 1 & Z_1 S \\ S\left(\frac{1}{Z_1}+\frac{1}{Z_2}\right) & 1+\frac{Z_1}{Z_2}S^2 \end{bmatrix} \quad (1)$$

For the transformed circuit below, the $ABCD$ parameter matrix for the entire network is:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_R = \frac{1}{\sqrt{1-S^2}} \begin{bmatrix} 1 & \frac{Z_2}{N} S \\ \frac{N}{Z_2} S & 1 \end{bmatrix} \begin{bmatrix} 1 & \frac{Z_1}{N} S \\ 0 & 1 \end{bmatrix} = \frac{1}{\sqrt{1-S^2}} \begin{bmatrix} 1 & \frac{S}{N}(Z_1+Z_2) \\ \frac{N}{Z_2} S & 1+\frac{Z_1}{Z_2}S^2 \end{bmatrix} \quad (2)$$

Because of $N = 1 + Z_2/Z_1$, it can be concluded that

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_L = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_R \quad (3)$$

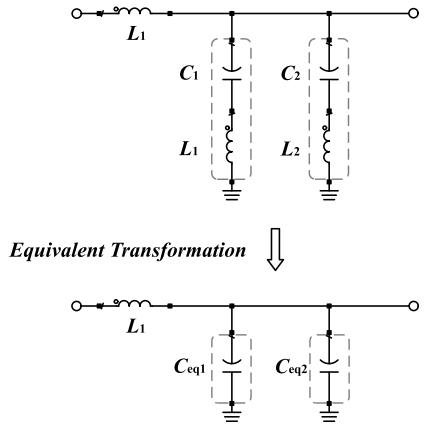

FIGURE 5. Equivalent network of two series-connected LC resonant circuits.

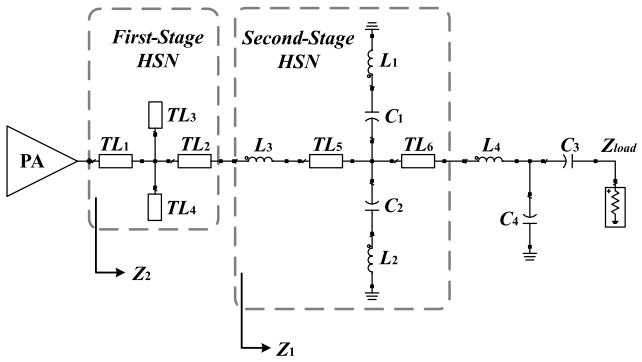

FIGURE 6. Output matching network circuit diagram.

3.2. A Harmonic Suppression Network Based on Two Series-Connected LC Resonant Circuits

The second-level harmonic suppression network employed lumped components. Fig. 5 shows the equivalent network of the two series-connected LC resonant circuits. Circuits L_1 and C_1 form the first branch with a resonant frequency of $3\omega_0$. Circuits L_2 and C_2 form a second branch with a resonant frequency of $5\omega_0$. These circuits suppress the third- and fifth-harmonic signals, respectively. The loop impedance of an ideal series LC resonant circuit is

$$Z = jwL + \frac{1}{jwC} = j\left(wL - \frac{1}{wC}\right) \quad (4)$$

Setting the virtual component to zero yields the resonant angular frequency ω_0 and resonant frequency f_0:

$$\begin{cases} w_0 = \frac{1}{\sqrt{LC}} \\ f_0 = \frac{1}{2\pi\sqrt{LC}} \end{cases} \quad (5)$$

Figure 6 shows the overall circuit of the output matching network, where the relationship between the output load Z_2 of the power transistor and the output power P_{out} is

$$Z_2 = \frac{(V_{CC} - V_{ces})^2}{2P_{out}} \quad (6)$$

V_{CC} represents the supply voltage, and V_{ces} denotes the voltage between the collector and the emitter. To achieve impedance matching, the impedance Z_1 between the first-stage harmonic suppression network (First-Stage HSN) and second-stage harmonic suppression network (Second-Stage HSN) is defined as

$$Z_1 = \sqrt{Z_2 Z_{\text{load}}} \quad (7)$$

For a series LC resonant network, if resonance occurs at the nth harmonic frequency, then:

$$n\omega_0 = \frac{1}{\sqrt{LC}} \quad (8)$$

Combining (4) and (8) yields:

$$Z = -\mathrm{j}\frac{1}{\left(\frac{n^2}{n^2-1}\right)\omega_0 C} \quad (9)$$

At the resonance point, the resonant network can be equivalent to the capacitance C_{eq}, that is,

$$C_{\text{eq}} = \left(\frac{n^2}{n^2-1}\right) C \tag{10}$$

For the two-path series resonant network in this design, which resonates at the third and fifth harmonic frequencies, their equivalent capacitances are denoted as C_{eq1} and C_{eq2}. Substituting these values into (10) yields:

$$\begin{cases} C_{\text{eq1}} = \frac{9}{8} C_1 \\ C_{\text{eq2}} = \frac{25}{24} C_2 \end{cases} \tag{11}$$

Based on the series and parallel connections between circuit components, we obtain:

$$Z_1 = \text{j}\omega_0 L_3 + \frac{Z_{\text{load}} \frac{1}{\text{j}\omega_0 (C_{\text{eq1}}+C_{\text{eq2}})}}{Z_{\text{load}} + \frac{1}{\text{j}\omega_0 (C_{\text{eq1}}+C_{\text{eq2}})}} \tag{12}$$

According to (12), let $3L_1{=}5L_2$ and $3C_1{=}5C_2$. The final solution is:

$$\begin{cases} C_1 = \frac{4\sqrt{Z_{\text{load}}/Z_1 - 1}}{7 Z_{\text{load}} \omega_0} \\ C_2 = \frac{12\sqrt{Z_{\text{load}}/Z_1 - 1}}{35 Z_{\text{load}} \omega_0} \\ L_1 = \frac{7 Z_{\text{load}}}{36 \omega_0 \sqrt{Z_{\text{load}}/Z_1 - 1}} \\ L_2 = \frac{7 Z_{\text{load}}}{60 \omega_0 \sqrt{Z_{\text{load}}/Z_1 - 1}} \\ L_3 = \frac{Z_1 \sqrt{Z_{\text{load}}/Z_1 - 1}}{\omega_0} \end{cases} \tag{13}$$

3.3. Output Matching Network

Figure 6 shows the overall circuit structure of the output matching network, which consists of a two-stage harmonic suppression network and a fundamental matching network. The first-stage harmonic suppression structure employs Richards' principle and Kurado's rule to transform a third-order Butterworth filter into a cross-junction microstrip line, with the aim of suppressing second harmonic components within the passband. The second-stage harmonic suppression structure utilizes two series-connected LC resonant networks to suppress the third- and fifth-harmonic components. The fundamental matching network comprises a single LC circuit. Additionally, a DC-blocking capacitor C is incorporated at the output to isolate the DC signals while allowing the radio frequency (RF) signals to pass through.

Figure 8(a) shows the output power spectrum simulation results without the harmonic suppression network, whereas Fig. 8(b) presents the results with the harmonic suppression network incorporated. At a frequency of 0.8 GHz and an output power of 41 dBm, the suppression ratios for the 2nd to 5th harmonics improved by approximately 44 dB, 53 dB, 8 dB, and 13 dB, respectively, demonstrating a significant enhancement in harmonic suppression performance.

Through the ADS electromagnetic simulation of the output-matching network, its S-parameters at various frequencies were obtained, as shown in Fig. 9. S_{11} represents the reflection coefficient of the RF signal input port. It is defined as the ratio of the reflected wave amplitude to the incident wave amplitude when the output port is terminated with a 50 Ω matched load. A larger $|S_{11}|(0 < |S_{11}| < 1)$ indicates a more severe reflection, leading to power backflow, reduced efficiency, and compromised transistor stability. S_{21} is the forward transmission coefficient from input to output, defined as the ratio of the output wave amplitude to the input wave amplitude when the output port is connected to a 50 Ω matched load. A smaller $|S_{21}|(0 < |S_{21}| < 1)$ indicates greater transmission loss. At 0.4–1.2 GHz, this output matching network achieves $S_{11} < -17$ dB and $S_{21} > -0.4$ dB, fully meeting design requirements.

4. EXPERIMENTAL RESULTS

4.1. Electromagnetic Simulation

The complete circuit of the proposed ultra-wideband laterally diffused metal oxide semiconductor (LDMOS) power amplifier is shown in Fig. 15. Electromagnetic (EM) simulations were performed using Advanced Design System (ADS) software. Fig. 10 shows the small-signal simulation test results for this design. Return loss RL $= -|S_{11}|$ dB is defined as the ratio of the incident power P_{inc} to the reflected power P_{ref}. A higher return loss indicates a lower reflected power and better impedance matching. Gain S_{21} is defined as the ratio of the output power to the input power, representing the amplification capability of the power amplifier. However, an excessively high gain can easily lead to circuit self-oscillation and amplify noise, thereby affecting the signal-to-noise ratio of the system. In this design, RL < -7 dB and Gain > 14 dB, with the gain flatness maintained between 0.5 and 1.5 dB.

Figure 11 shows the variation curves of drain efficiency (DE) and G_p with the output power for the amplifier at 0.4 GHz, 0.6 GHz, 0.8 GHz, 1 GHz, and 1.2 GHz. Fig. 12 presents the saturated output power (3 dB gain compression), saturated gain, and corresponding drain efficiency at each frequency point. Simulation results indicate a DE of 56.63%–62.89%, a saturated output power of 40.95–42.3 dBm, and a saturated gain

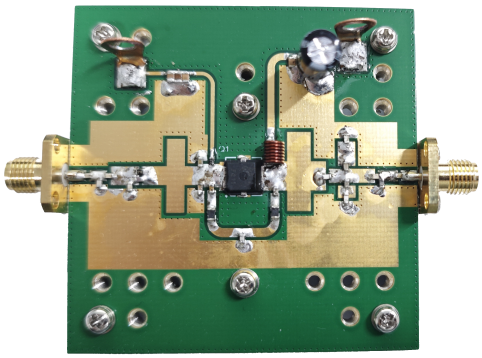

FIGURE 7. Physical implementation of an ultra-wideband LDMOS power amplifier based on a two-stage harmonic suppression network.

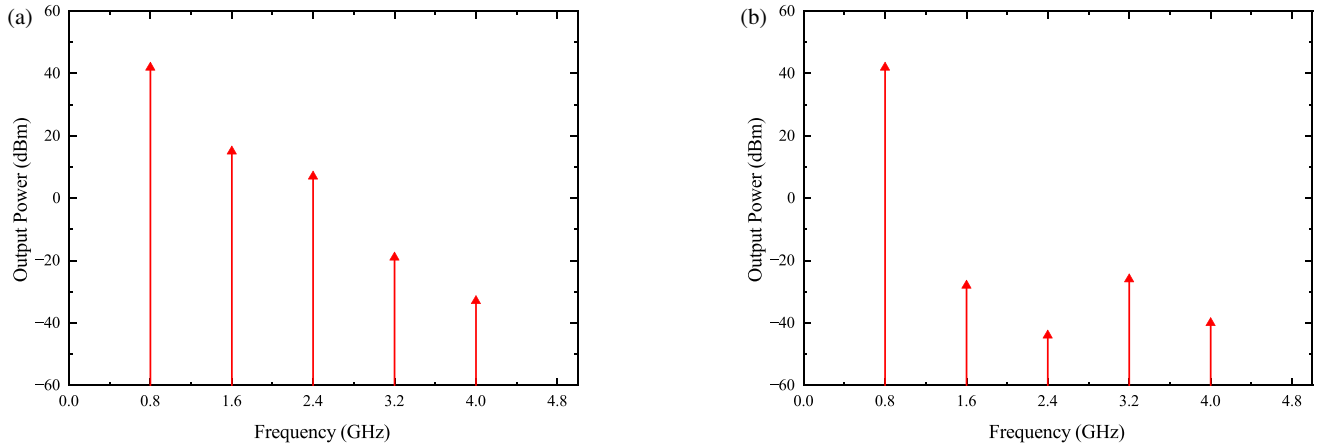

FIGURE 8. Output power spectrum comparison: With and without HSNs.

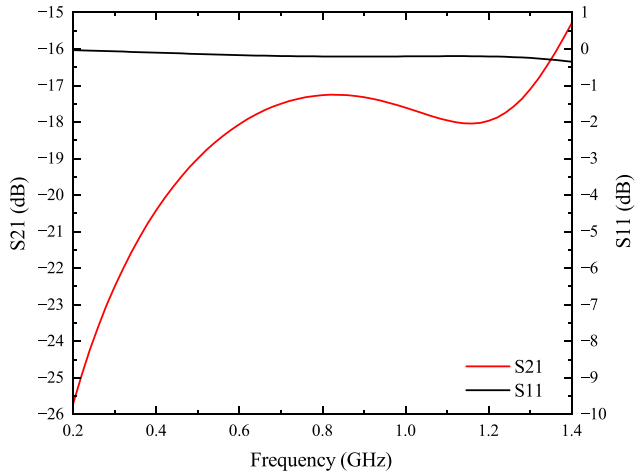

FIGURE 9. Output the S_{11} and S_{21} curves of the matching network.

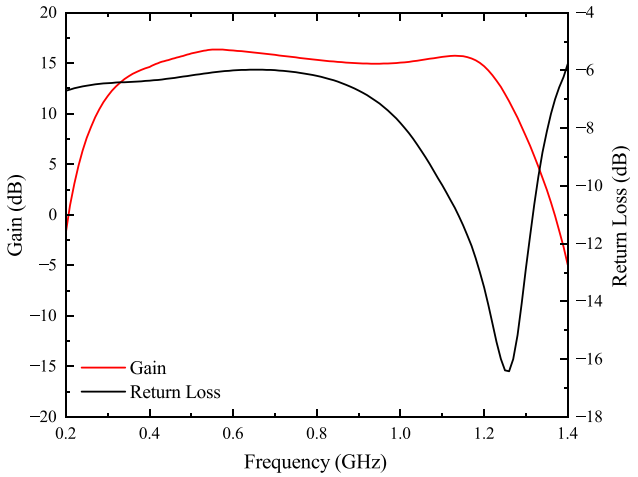

FIGURE 10. Small-signal simulation test results.

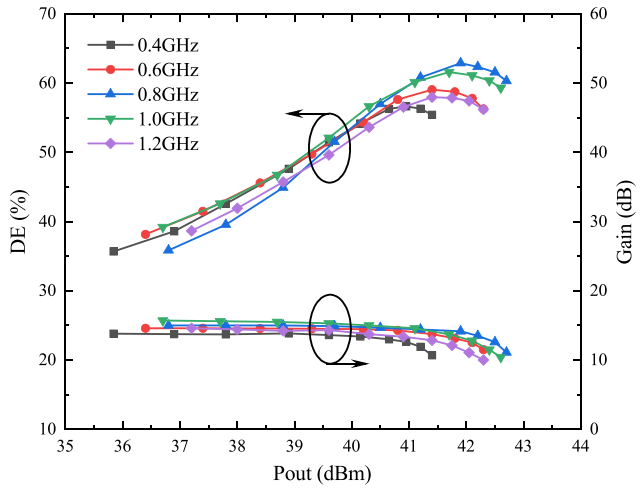

FIGURE 11. Drain efficiency and power gain versus output power curves (under EM simulation conditions).

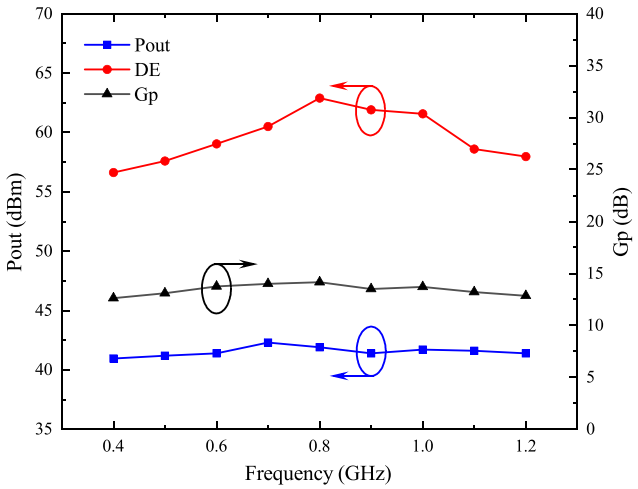

FIGURE 12. Saturated output power, saturated gain, and drain efficiency at each frequency point (under EM simulation conditions).

of 12.61–14.15 dB. These data demonstrate that the designed ultra-wideband LDMOS power amplifier exhibits excellent broadband performance within the target frequency band.

4.2. Physical Testing

Figure 7 shows a photograph of the actual test board, measuring 60 mm × 60 mm and constructed from FR4 material with a

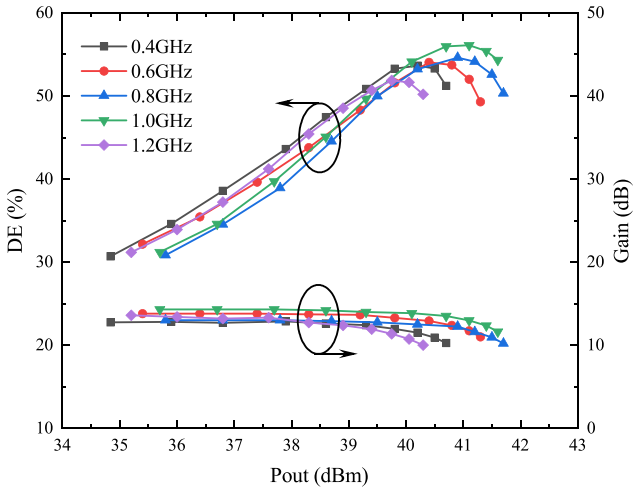

FIGURE 13. Drain efficiency and power gain versus output power curves (under actual test conditions).

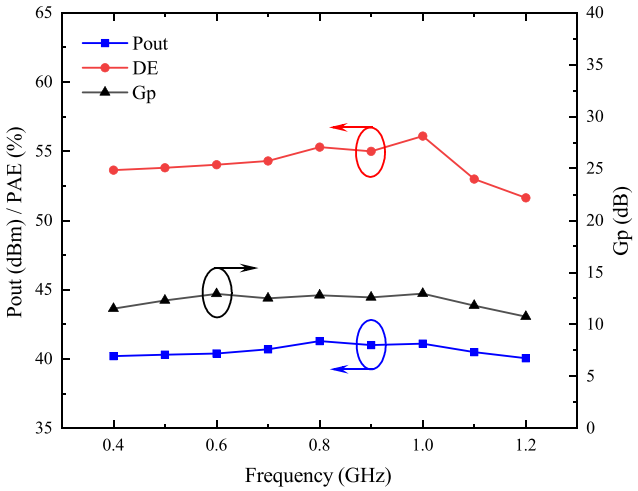

FIGURE 14. Saturated output power, saturated gain, and drain efficiency at each frequency point (under actual test conditions).

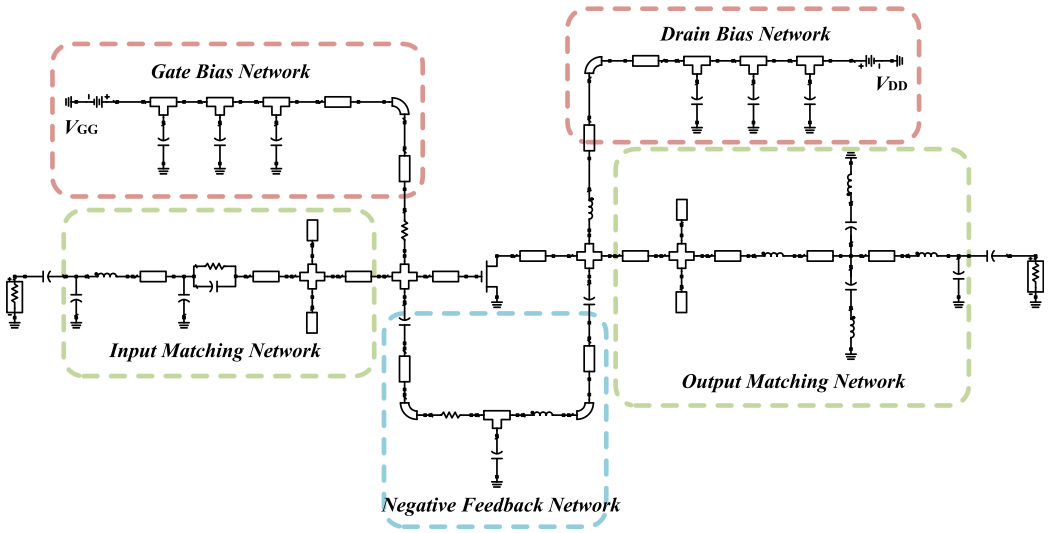

FIGURE 15. Complete circuit of an ultra-wideband LDMOS power amplifier.

thickness of 1 mm. During the actual measurements, the drain-supply voltage of the power amplifier was set to 28 V. At a gate voltage of 2.3 V, the quiescent current, I_{dq}, was 100 mA.

To ensure amplifier stability across the entire bandwidth, a negative feedback circuit based on a Butterworth filter prototype was incorporated. The input-matching network consists of an LC circuit, an RC stabilizing circuit, and a cross-shaped microstrip line with a DC-blocking capacitor. The output matching network employs a two-stage harmonic suppression network combined with an LC fundamental matching circuit that features DC-blocking capacitors. To ensure that the gate bias remains in a high-impedance state, a series resistor was incorporated. In the drain-bias circuit, coil inductance is used for impedance matching and feeding. Capacitors on the bias line serve in power-supply decoupling. Electrolytic capacitors were added during the actual circuit assembly to prevent RF signal leakage in the drain bias circuit.

During actual testing, small-signal characteristics of the designed ultra-wideband LDMOS power amplifier were first measured using a vector network analyzer (VNA). At this stage, the amplifier operated within its linear region. S-parameters from the VNA provided the return loss, small-signal gain, and VSWR, enabling the assessment of amplifier stability and the degree of matching between its ports and 50 Ω impedance. A continuous-wave (CW) signal was employed for large-signal testing of the fabricated power amplifier. A continuous sine wave generated by the RF signal generator is amplified by the driver amplifier, ensuring controllable input signals to the amplifier under test. The output signal, which was attenuated by an attenuator, was displayed on the spectrum analyzer. Additionally, to prevent mutual interference between the driver amplifier and the amplifier under test, an isolator was inserted between them, thereby enhancing isolation.

Figure 13 shows the variation curves of the drain efficiency and gain with the output power measured at multiple frequen-

TABLE 1. Performance comparison table for broadband power amplifiers.

Ref.	Transistor	BW (GHz)	RBW (%)	Psat (dBm)	DE (%)	Gain dB	Size ($W \times L$ mm)
[7]	GaN	1.9–3.1	48	39.3–40.5	48–56.6	9.3–10.7	67×45
[10]	GaN	0.55–3.3	142.9	39.1–42	60.1–76.2	9.1–12	44×83
[16]	GaN	1.6–2.8	55	38–41	49–65	-	67×53
[20]	GaN	1.4–3.6	88	38.8–41.0	56.6–75.8	9–11.1	-
[21]	GaN	0.4–2.0	133	> 40	61–72	11	120×122
[22]	GaN	0.7–3.8	138	39–42.1	59–70	9–12.1	38×57
[23]	GaN	0.5–2.0	120	39.8–42.25	60.1–72	9.5–12.2	-
This work	LDMOS	0.4–1.2	100	40.1–41.3	51.6–56.1	10.8–12.9	60×60

cies. Fig. 14 presents the variation curves of the drain efficiency, gain, and saturated output power with the frequency measured at different output power levels. The measured results indicate that within the 0.4–1.2 GHz band, the saturated output power reaches 40.1–41.3 dBm, with drain efficiency ranging from 51.6% to 56.1% and a power gain ranging from 10.8 to 12.9 dB. Owing to manufacturing tolerances and modeling inaccuracies, the measured results exhibited slight deviations from the simulated performance across the entire frequency band. Overall, this ultra-wideband LDMOS power amplifier still demonstrates excellent performance advantages within its operating bandwidth.

5. CONCLUSION

Table 1 summarizes the operating metrics of various broadband power amplifiers reported in recent years. The comparison results demonstrate that the designed ultra-wideband power amplifier exhibits highly efficient performance across the 0.4–1.2 GHz frequency band. The gain is maintained at 15.5 dB with exceptionally flat broadband gain characteristics, offering significant advantages over traditional power amplifiers that suffer from insufficient low-frequency and high-frequency gain roll-off. The saturated output power exceeds 40.1 dBm, providing ample output power to meet the signal transmission demands in medium-to-high power applications. The drain efficiency surpassed 51.6%, with a maximum efficiency of 56.1%, enabling the efficient conversion of electrical energy into output signals while minimizing energy loss and enhancing overall efficiency. Furthermore, the amplifier offers significant size advantages, facilitating its integration into compact systems. In summary, the designed ultra-wideband LDMOS power amplifier delivers superior performance across the 0.4–1.2 GHz frequency band. It holds significant engineering application value and commercialization potential in critical fields such as communications, radar, testing, and measurement.

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