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Design of a 200-W High-Efficiency Cascaded LDMOS Microwave Source with Digital Power Control

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ABSTRACT: This study designs and experimentally validates a digitally controlled 2.45 GHz solid-state microwave power source for industrial continuous-wave operation. The source employs a cascaded laterally diffused metal oxide semiconductor (LDMOS) architecture integrating a phase-locked loop frequency synthesizer, a multi-stage driver chain, and a closed-loop digital power-control network with 0.5-dB resolution. The final-stage power amplifier (PA) is biased in deep class-AB, and a lumped-element matching network is synthesized — guided by load-pull and harmonic-impedance analysis — to realize a near-short termination at the second harmonic and reduce voltage-current overlap energy. Nonlinear device modelling and system-level analysis are used to predict efficiency and stability. Measurements show a saturated output power of 54.09 dBm, gain of 18.14 dB, and peak power-added efficiency of 61.89% under a 28-V supply. The source achieves accurate continuous-wave (CW) power regulation from 35 to 53 dBm with good thermal stability. These results indicate that combining deep class-AB biasing with second-harmonic near-short termination enables high-efficiency operation in L/S-band industrial microwave sources, and the cascaded digitally controlled architecture provides robust power management for microwave heating and plasma excitation systems.

1. INTRODUCTION

In microwave engineering, high-power microwave sources for industrial applications require a joint consideration of radio frequency (RF) circuit design, electromagnetic field distribution, and thermal management. The 2.45 GHz industrial, scientific, and medical (ISM) band is central to continuous-wave (CW) applications such as microwave heating and wireless power transfer, where the propagation characteristics and a power density distribution directly determine system performance [1, 2]. At this frequency, power-added efficiency (PAE) exceeding 50% has been achieved using harmonic-tuned matching networks [3]. For broadband applications, Zhao et al. [4] improved signal integrity through multi-harmonic control, and studies on 5G communications [5], satellite communications, and deep-bias high-efficiency operation [6, 7] demonstrate the adaptability of gallium nitride (GaN) devices. Song et al. [8] investigated nonlinear modelling and the impact of reactive harmonic loading.

Although GaN devices exhibit superior high-frequency performance, laterally diffused metal oxide semiconductor (LDMOS) technology retains a dominant position in L/S-band CW industrial applications. This preference is attributed to its established cost-effectiveness, excellent electromagnetic compatibility, and proven electro-thermal reliability [9–12]. Recent studies have further validated its robustness in practical scenarios: Cassan et al. [13] demonstrated that, when combined with precise full-wave simulation of bond wires, LDMOS devices can maintain competitive efficiency under CW operation at 2.2 GHz. From a circuit design perspective, realizing the full potential of LDMOS relies heavily on optimal impedance transformation and harmonic termination control [14, 15]. Theoretically, the continuous-mode theory proposed by Cripps et al. [16] established the foundation for efficiency enhancement via harmonic tuning. Building on this framework, Dong et al. [17] achieved a high efficiency of 70% by utilizing an extended inverse class-F mode. These theoretical advancements provide critical guidelines for the design of high-power microwave sources.

This paper proposes a 2.45 GHz digitally controlled cascaded LDMOS microwave source tailored for industrial applications. The primary contribution of this work lies in the integration of a closed-loop digital control network with a synergistic waveform engineering strategy. By implementing real-time power detection and digital attenuation, the system enables precise, programmable CW power regulation with a fine resolution of 0.5 dB. To maximize energy efficiency, deep class-AB biasing is combined with second-harmonic near-short termination to minimize the voltage-current overlap energy, thereby significantly enhancing the PAE. Experimental validation demonstrates that the developed source achieves a saturated output power of 53.38 dBm (54.09 dBm peak) and a gain of 18.14 dB, with a peak PAE reaching 61.89%. Furthermore, the system exhibits robust stability during power regulation across a wide dynamic range of 35 to 53 dBm, with measured fluctuations strictly confined within 0.1 dB.

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2. THEORETICAL MODELLING AND ANALYSIS OF HIGH-EFFICIENCY CASCADED LDMOS POWER AMPLIFIERS

2.1. Nonlinear Device Modelling and Deep Class-AB Operation Mechanism

To accurately predict the dynamic load-line trajectory of the 200 W CW microwave source under large-signal excitation, it is crucial to establish a physics-based nonlinear model for the LDMOS. Unlike ideal switch models, actual devices exhibit significant "soft-compression" characteristics during the transition between the saturation and linear regions [18, 19]. The drain current $i_D(t)$ is modelled as a superposition of the controlled channel current and the nonlinear displacement current:

$$i_D(t) = I_{\mathrm{DSS}}\left(1 - \frac{v_{\mathrm{GS}}}{V_{\mathrm{P}}}\right)^2 \tanh\left(\frac{\alpha v_{\mathrm{DS}}}{V_{\mathrm{GS}} - V_{\mathrm{P}}}\right) + \frac{\mathrm{d}}{\mathrm{d}t}\left[C_{\mathrm{ds}}(v_{\mathrm{DS}})v_{\mathrm{DS}}\right] + C_{\mathrm{gd}}(v_{\mathrm{DS}})\frac{\mathrm{d}}{\mathrm{d}t}(v_{\mathrm{DS}} - v_{\mathrm{GS}}) \quad (1)$$

where I_{DSS} is the saturation drain current; V_{P} is the pinch-off voltage; α controls the knee-voltage characteristics; C_{ds} and C_{gd} are nonlinear parasitic capacitances. Equation (1) shows that reducing the overlap between the high-voltage and high-current regions is key to suppressing AM-PM effects.

In the final-stage design, a deep class-AB bias is adopted to lower static power consumption [20]. The current conduction angle (CCA) expressed as $2\theta_c$, where θ_c is the conduction half-angle, and is set by the quiescent gate bias $V_{\mathrm{GS},q}$ and the input drive V_{in}:

$$\theta_c = \arccos\left(-\frac{V_{\mathrm{GS},q} - V_{\mathrm{P}}}{V_{\mathrm{in}}}\right) \quad (2)$$

For $\pi/2 < \theta_c < \pi$, the drain current becomes a truncated sine wave. Its Fourier expansion yields the DC component.

$$I_{\mathrm{dc}}(\theta_c) = \frac{I_{\max}}{\pi(1 - \cos\theta_c)}(\sin\theta_c - \theta_c\cos\theta_c) \quad (3)$$

which governs average power consumption, and the fundamental component

$$I_1(\theta_c) = \frac{I_{\max}}{\pi(1 - \cos\theta_c)}(\theta_c - \sin\theta_c\cos\theta_c) \quad (4)$$

where $I_1(\theta_c)$ delivers the output power. A comparison of (3) and (4) reveals that deep class-AB slightly reduces I_1 (by shrinking θ_c) but markedly lowers I_{dc}, thereby boosting electronic efficiency [21]. The higher-order Fourier coefficients $(I_2, I_3, \ldots)$ are simultaneously enhanced, providing a physical foundation for subsequent waveform engineering [10].

As summarized in Table 1, CCA directly determines the trade-off between the theoretical maximum drain efficiency and linearity, where the latter is quantified by $\mathrm{BW}_{\mathrm{R-1\,dB}}$ under 1% harmonic distortion (HD). When θ_c is reduced, the quiescent current I_q approaches zero, pushing the theoretical efficiency limit up to 78% (approaching Class-B operation), at the expense of a reduced linear bandwidth and increased distortion. Conversely, when $2\theta_c$ is increased beyond $0.726 \times 2\pi$, the linear bandwidth is significantly widened, but I_q can exceed $0.4 \times I_{\mathrm{Dmax}}$, causing the maximum efficiency to drop below 61.5%. Therefore, a deep class-AB bias point is strategically selected to balance the linearity required for continuous-wave (CW) operation and a sufficiently high efficiency prior to harmonic tuning.

TABLE 1. Performance parameter values corresponding to CCA.

CCA	$\mathrm{BW}_{\mathrm{R\text{-}1\,dB}}$ (1% HD)	I_q/I_{Dmax}	Max Drain Efficiency (%)
$0.5 \times 2\pi$	1.155	0	78
$0.62 \times 2\pi$	1.276	0.27	70
$0.7 \times 2\pi$	1.519	0.37	63
$0.726 \times 2\pi$	1.717	0.40	61.5
$0.758 \times 2\pi$	3.39	0.415	60
$> 0.766 \times 2\pi$	∞	0.428	< 60

2.2. Time-Domain Waveform Engineering and Impedance Sensitivity Analysis

In this section, waveform engineering techniques are introduced to optimize drain efficiency. Assuming that the matching network presents an ideal open or short circuit to higher-order harmonics ($n \geq 4$), the normalized drain voltage waveform $v_{\mathrm{DS}}(\theta)$ can be expressed as

$$v_{\mathrm{DS}}(\theta) = V_{\mathrm{D}} - V_1\cos\theta + V_2\cos(2\theta + \phi_2) + V_3\cos(3\theta + \phi_3) + \sum_{n=4}^{N} V_n\cos(n\theta + \phi_n) \quad (5)$$

where V_n represents the voltage amplitude of the n-th harmonic. By controlling the matching network to realize a near short second-harmonic impedance, $Z_{\mathrm{L}}(2\omega) \approx 0$, the voltage waveform is maintained at a low value during the conduction interval, thereby minimizing the average dissipated power

$$P_{\mathrm{diss}} = \frac{1}{2\pi}\int_{-\pi}^{\pi} v_{\mathrm{DS}}(\theta)i_{\mathrm{D}}(\theta)\mathrm{d}\theta \quad (6)$$

Substituting (3) and (4) into the efficiency definition yields the theoretical upper limit of drain efficiency $\eta_{\mathrm{D,max}}$ in the deep class-AB mode:

$$\eta_{\mathrm{D,max}} = \frac{1}{2}\frac{V_1}{V_{\mathrm{D}}}\frac{I_1(\theta_c)}{I_{\mathrm{dc}}(\theta_c)} = \frac{1}{2}\xi\frac{\theta_c - \sin\theta_c\cos\theta_c}{\sin\theta_c - \theta_c\cos\theta_c} \quad (7)$$

where $\xi = V_1/V_{\mathrm{D}}$ is the fundamental voltage-swing factor. Equation (7) shows that increasing ξ through harmonic tuning is the core pathway to improving efficiency [22].

However, the engineering challenge lies in the sensitivity of efficiency to the impedance phase. The first-order sensitivity of η to the second-harmonic reactance X_{2f} is

$$\frac{\partial\eta}{\partial X_{2f}} \approx -K|I_2|\sin(\Delta\phi_{2f}) \quad (8)$$

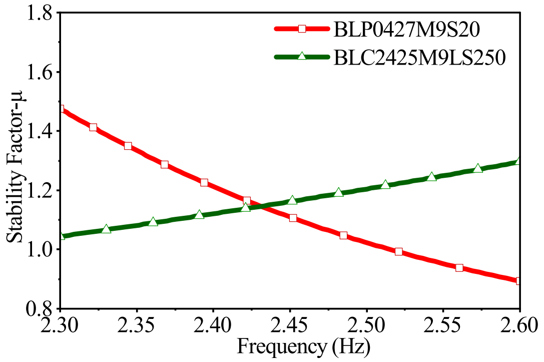


FIGURE 1. Stability factor sweep.

where K is a constant, and $\Delta\phi_{2f}$ is the phase deviation. Equation (8) reveals that the sensitivity is proportional to the harmonic-current amplitude $|I_2|$, implying that deep class-AB requires a significantly higher phase flatness in the matching network than in a traditional class-AB. Theoretical calculations show that this strategy can improve efficiency by approximately 8–12% compared with an untuned state, and its harmonic-termination concept aligns with the waveform-shaping ideas of class-F/continuous modes.

2.3. Cascaded System Modelling and Stability Synthesis

To satisfy the 200 W output requirement, a two-stage cascaded topology is adopted. Owing to the strong nonlinearity of the final stage, the system output $v_{\text{out}}(t)$ is modelled using a Volterra series to characterize AM-AM and AM-PM distortions:

$$v_{\text{out}}(t) = \alpha_1 v_{\text{in}}(t) + \alpha_2 v_{\text{in}}^2(t) + \alpha_3 v_{\text{in}}^3(t) + \dots \tag{9}$$

where the odd-order coefficients (e.g., α_1) dominate in-band distortion. This model is directly used in the design of digital pre-distortion (DPD) algorithms.

The PAE of the cascaded system is determined by the inter-stage gain and efficiency distribution as follows.

The total power-added efficiency of the cascaded system is given by

$$\text{PAE}_{\text{sys}} = \eta_2 \frac{1 - \dfrac{1}{G_1 G_2}}{1 + \dfrac{\eta_2}{\eta_1 G_2}} \tag{10}$$

where G and η denote the gain and drain efficiency, respectively. Equation (10) shows that when G_2 is sufficiently large the influence of the driver-stage efficiency η_1 on the overall PAE is suppressed by the factor G_2, resulting in the design guideline of a "high-linearity driver + high-efficiency final stage" [15, 23]. Simultaneously, the driver stage should be operated with an approximately 3 dB output power backed-off from its $\text{P}_{1\,\text{dB}}$ to avoid a rapid drop in η_i and an increase in the DC component caused by excessive compression [15, 23].

2.4. Second-Harmonic Termination and Stability Analysis

The second-harmonic termination in the final stage is realized using a lumped-element shunt stub that suppresses the second-harmonic voltage without disturbing the optimum fundamental load. The input impedance of an open-circuited stub is

$$Z_{\text{in}}^{\text{open}}(\omega) = -\mathrm{j}Z_0 \cot\left[\beta(\omega)\ell\right] \tag{11}$$

where ℓ is the physical length. By choosing ℓ to be a quarter-wavelength at 2ω we obtain $Z_{\text{in}}^{\text{open}}(2\omega) \approx 0$, that is, a near-short at the second harmonic. At the fundamental frequency $\omega_0 (\beta(\omega_0)\ell \approx \pi/4)$, the stub presents a finite pure reactance of magnitude $\approx Z_0$; co-designing the main matching network reduces its perturbation on the optimum fundamental load (e.g., $Z_{\text{opt}} \approx 1.8 - \mathrm{j}1.2\,\Omega$) to a negligible level [24, 25]. The harmonic near-short drives $v_{\text{DS}}(\varphi)$ towards a half-wave-rectified shape and reduces the voltage-current overlap energy

$$E_{\text{ol}} = \frac{1}{2\pi}\int_{-\pi}^{\pi} v_{\text{DS}}(\varphi) i_{\text{D}}(\varphi) \mathrm{d}\varphi \tag{12}$$

yielding an efficiency improvement of approximately 8–10%. This lumped-element approach retains the waveform-shaping benefits of the class-AB/F and continuous modes without requiring distributed traveling-wave structures [20, 24, 25].

Unconditional stability from DC to $3f_0$ is verified by the geometric stability factor

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{21} S_{12}|} > 1 \tag{13}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. An R-L-C network at the gate terminal ensures $\mu > 1$ without degrading the RF performance; checking $K(\omega) > 1$ and $|\Delta(\omega)| < 1$ across the target band prevents loop instability owing to lumped-element resonances [15, 26]. Under a practical gain distribution (final-stage gain ≥ 10 dB), the system PAE asymptotically approaches that of the deep class-AB final power amplifier (PA), confirming the design strategy of maximizing final-stage efficiency while using the driver stage primarily for linearity and gain.

3. MICROWAVE POWER SOURCE DESIGN

3.1. Overall Architecture

The overall architecture of the high-power microwave source proposed in this study is illustrated in Fig. 2. A microcontroller unit (MCU) controls a phase-locked loop (PLL) to generate a 2.45 GHz small-signal microwave output. This signal passes sequentially through an isolator/attenuator, a first-stage driver amplifier, a digitally controlled attenuator, a second-stage driver amplifier, a low-pass filter, a third-stage driver amplifier, a fourth-stage driver amplifier, and a final-stage power amplifier, ultimately delivering a high-power CW microwave output. The primary function of the first-stage attenuator is to isolate the PLL from subsequent circuits, thereby preventing load-pulling effects on the PLL.

The MCU regulates the digital attenuator using a classical Proportional-Integral-Derivative Controller (PID) algorithm to achieve an output-power step control with a precision of 0.5 dB. As the performance of traditional GaAs MESFETs and silicon bipolar transistors reaches its limits, LDMOS and GaN HEMT devices have become the mainstream choice for modern power applications. LDMOS devices offer high linearity, high output

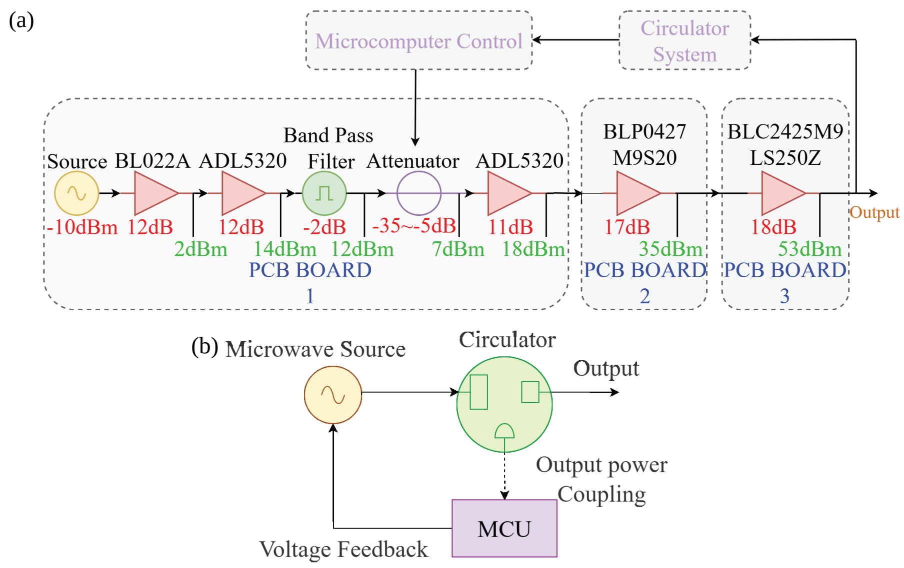


FIGURE 2. Overall framework of microwave source. (a) Microwave source system. (b) Circulator system.

power, superior thermal stability, and cost-effectiveness, making them particularly suitable for communication-base-station applications that demand stringent linearity.

3.2. Frequency Source and Driver Chain

This design employs the ADF4360 as the frequency source. The ADF4360, developed by Analog Devices, is a wideband frequency synthesizer with an integrated voltage-controlled oscillator (VCO) capable of generating fundamental frequencies from 2.2 to 4.4 GHz; internal dividers extend the range down to 137.5 MHz. The device is controlled by an MCU via an SPI interface through six on-chip registers, enabling precise frequency tuning.

After generation, the microwave signal feeds the first- and second-stage driver amplifier. The pre-driver uses a BEREX BL022A enhanced pseudomorphic HEMT (E-pHEMT), which covers 50 MHz–6 GHz, exhibits a 1.5 dB noise figure, and provides 19 dB gain at 1.9 GHz. The first-stage driver was designed and simulated using the Advanced Design System. The bias was set to $V_\mathrm{D} = 5\,\mathrm{V}$, $I_\mathrm{D} = 70\,\mathrm{mA}$ (single 5 V supply). Stability analysis (StabFact) confirms a stability factor greater than unity, preventing self-oscillation. Input/output impedance matching and DC blocking were realized using 15 pF capacitors (Fig. 3(a)).

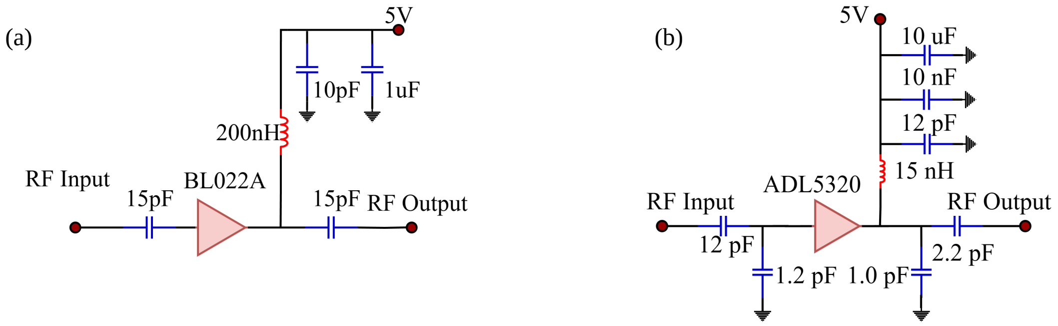
Because the combined output of the first two stages is insufficient to drive the final power amplifiers, a third-stage driver is added. This stage uses an Analog Devices ADL5320, which delivers $\approx$ 13 dB at 2.45 GHz with an output 1 dB compression point of 25 dBm. The device is internally matched; only external DC bias and DC-blocking capacitors are required (bias of 5 V, schematic in Fig. 3(b)).

Figure 3(c) presents the simulation results for the S-parameters and output power of the first-stage driver amplifier (BL022A) at 2.45 GHz CW with a 5 V supply. At 2.45 GHz, the amplifier gain reached 18 dB. With an input power of 0 dBm, the output power underwent compression but still achieved 18 dBm. Similarly, Fig. 3(d) illustrates the S-parameters and output power characteristics for the ADL5320 driver amplifier. At 2.45 GHz, it provides a stable gain of approximately 13 dB and reaches an output 1-dB compression point of 25 dBm under a 5 V supply. This circuit operates in the 1–4 GHz band and features a 6-bit control word, allowing for a stepped attenuation range of 2 to 27 dB with a step size of 0.5 dB. The attenuation level is controlled via an SPI interface, satisfying the amplitude control requirements of the designed microwave power source. As the PLL and amplifiers generate higher-order harmonics, a TDK DEA202450BT-1275A1 low-pass filter is employed to suppress these harmonic components.

3.3. Power Amplifier Stage Design

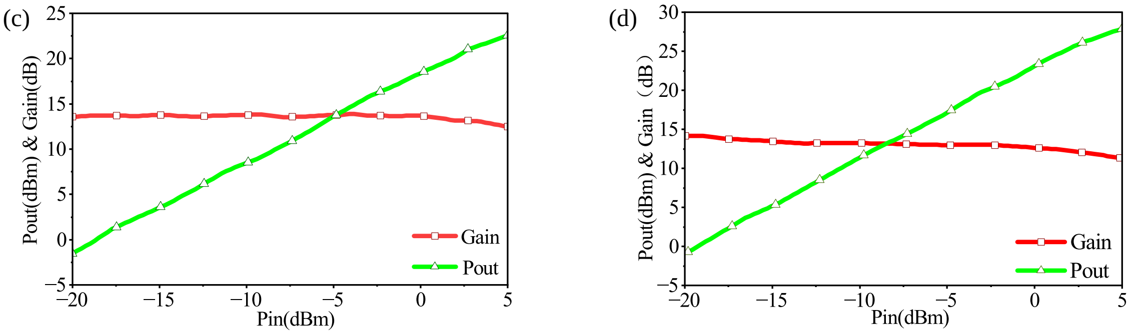
To achieve the 200 W output requirement, the power amplification section employs a cascaded LDMOS architecture matched to 50 Ω, designed on a 0.762 mm Rogers RO4350B substrate ($\epsilon_r = 3.48$, $\tan\delta = 0.002$). Both stages utilize a deep class-AB biasing strategy and non-linear electrothermal modelling to optimize the efficiency-linearity trade-off for industrial CW operation.

The fourth-stage driver utilizes an Ampleon BLP0427M9S20 transistor ($V_G = 2.1\,\mathrm{V}$, $V_D = 28\,\mathrm{V}$), with its detailed circuit topology illustrated in Fig. 4(a). Following the verification of unconditional stability (Fig. 1), harmonic load-pull analysis was performed to refine the impedance trajectory. Fig. 4(b) demonstrates that, at 2.45 GHz, the fundamental load impedance is precisely positioned within the peak PAE contour ($> 60.53\%$), while the second-harmonic trajectory is steered toward a near-short-circuit region on the edge of the Smith chart (Fig. 6(a)). This near-short termination ($Z_L(2\omega) \approx 0$) effectively suppresses the drain voltage during the conduction interval, minimizing the E_{ol}. Time-domain waveforms (Fig. 6(c)) corroborate this, showing the drain voltage being successfully suppressed during the high-current pulse. With $Z_S = 9.082 + j1.003\,\Omega$ and $Z_L = 1.665 - j2.42\,\Omega$



BL022A circuit

ADL5320 circuit



S-parameters and output power for BL022A

S-parameters and output power for ADL5320

FIGURE 3. Pre-stage driver amplifier circuits and their corresponding experimental test results.

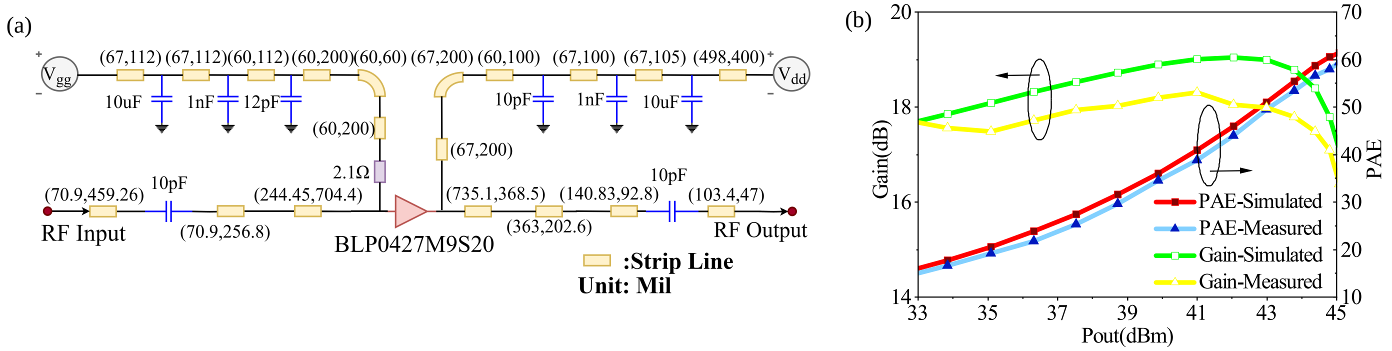


FIGURE 4. BLP0427M9S20 circuit and experimental results. (a) BLP0427M9S20 circuit. (b) S-parameters and output power for BLP0427M9S20.

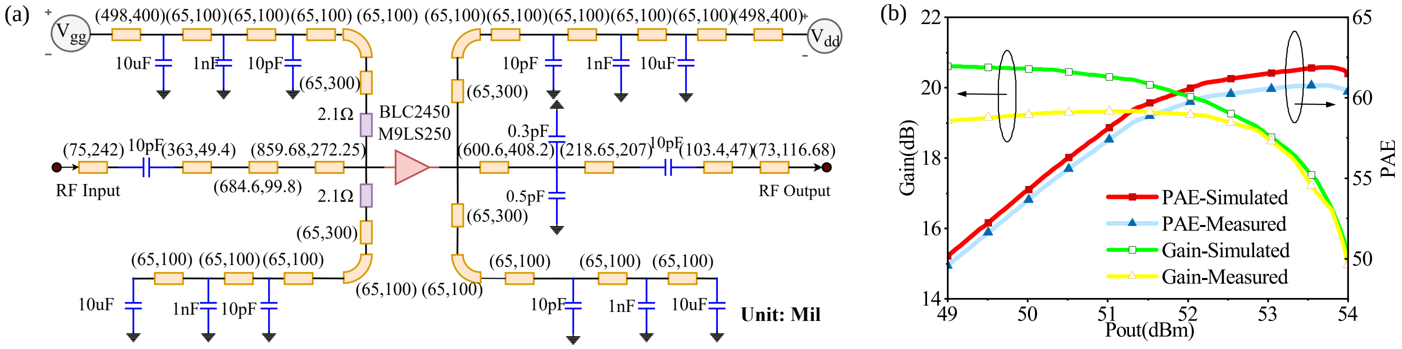
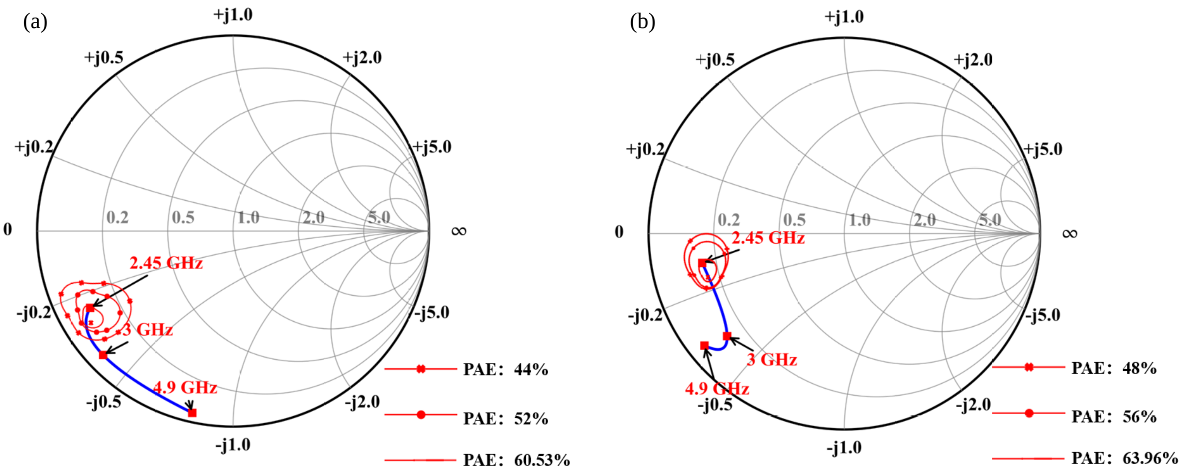
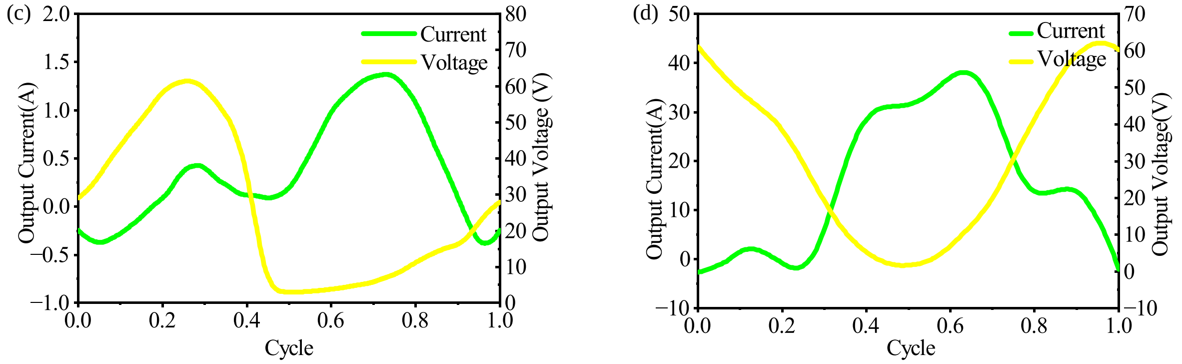


FIGURE 5. BLC2425M9LS250 circuit and experimental results. (a) BLC2425M9LS250 circuit. (b) S-parameters and output power for BLC2425M9LS250.



Harmonic trajectories (Stage 4)

Harmonic trajectories (Stage 5)



I-V waveforms (Stage 4)

I-V waveforms (Stage 5)

FIGURE 6. Analysis of harmonic load-pull trajectories and the corresponding time-domain drain waveforms for Stage 4 and Stage 5.

implemented via a π-type capacitive matching network, this stage achieves a 12.5 dB gain, 45.46 dBm maximum P_{out}, and a peak PAE of 60.58%.

As illustrated in Fig. 5(a), the final 200 W stage employs a BLC2425M9LS250 transistor ($V_G = 1.8\,\text{V}$, $V_D = 28\,\text{V}$). Similar to the driver stage, matching networks ($Z_S = 1.102 - j5.5\,\Omega$, $Z_L = 1.8 - j1.22\,\Omega$) were optimized using harmonic tuning to ensure thermal stability at high power levels. Load-pull analysis (Fig. 6(b)) places the fundamental impedance within a $> 63.96\%$ PAE. The experimental results presented in Fig. 5(b) indicate that the amplifier achieves a saturated output power of 54.09 dBm, a gain of 18.14 dB, and a 1-dB compression point ($P_{1\,\text{dB}}$) of 53.38 dBm. Under a 35.2 dBm drive, the peak PAE reached 61.89%. Fig. 6(d) illustrates the drain voltage and current waveforms of the fifth-stage amplifier in the saturated output state.

3.4. Frequency Source Control and Parameter Configuration

To ensure precise amplitude regulation and maintain high-power stability, a closed-loop control system based on a classical Proportional-Integral-Derivative (PID) algorithm was implemented. The controller dynamically adjusts the drive signal to minimize the error between the setpoint and the actual output. The continuous-domain control law $u(t)$ is defined as:

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau)d\tau + K_d \frac{de(t)}{dt} \tag{14}$$

where $e(t)$ is the instantaneous power error. The controller parameters were empirically optimized to: proportional gain $K_p = 0.81$, integral gain $K_i = 0.1\,\text{s}^{-1}$, and derivative gain $K_d = 0.05\,\text{s}$.

The system's dynamic performance is validated by the Maximum Power Test shown in Fig. 7. Upon commanding a target output of 53.0 dBm (200 W), the system undergoes an initial underdamped transient phase with characteristic oscillations. These fluctuations are effectively attenuated by the

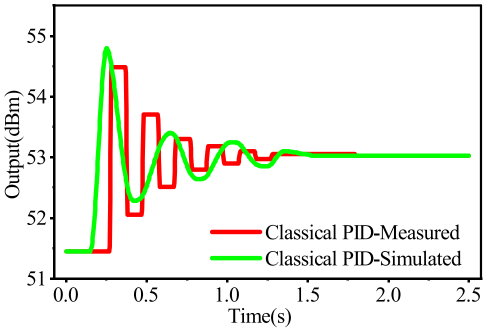


FIGURE 7. PID controller dynamic response.

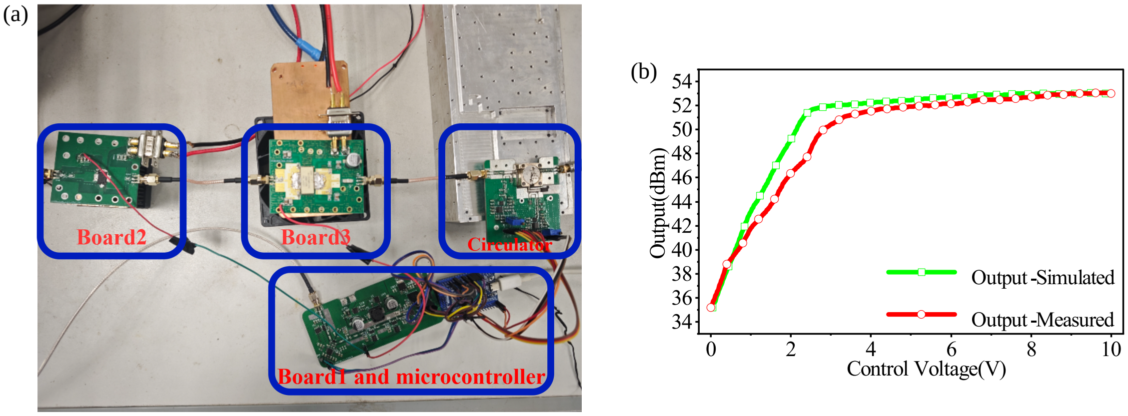


FIGURE 8. Digital attenuator circuit and attenuation characteristics. (a) Overall actual circuit diagram of the microwave source. (b) Attenuation Characteristics.

PID algorithm, which guides the output power to the set point with a measured settling time of approximately 1.8 s. Post-stabilization, the power delivery remains highly consistent, with measured fluctuations strictly confined within ±0.1 dB.

4. SYSTEM PERFORMANCE ANALYSIS AND MEASUREMENT

Figure 2(a) details the gain and output power distribution of each component under the maximum output-power condition. The frequency source output is -10 dBm. The gains for the subsequent stages are: 1st driver (12 dB), 2nd driver (12 dB), band-pass filter (-2 dB), digital attenuator (-35 to -5 dB), 3rd driver (11 dB), 4th PA (17 dB), and 5th PA (18 dB). Fig. 8 details the physical implementation and measured performance of the digital attenuator. As depicted in Fig. 8(a), the microwave source consists of four distinct modules: Board 1 (integrating the driver stage and microcontroller), Board 2 (the fourth-stage amplifier), Board 3 (the fifth-stage amplifier), and an isolation circulator module. Fig. 8(b) plots the measured attenuation against the control voltage, showing that the output power can be continuously tuned from approximately 53 dBm to 35 dBm over a voltage sweep of 0 V to 10 V. The excellent agreement between the simulated and measured results successfully validates the variable-gain stage design.

A circulator is connected at the output to ensure unidirectional transmission and facilitate power monitoring. Utilizing the non-reciprocal properties of ferrite, this three-port circulator transmits signals from Port 1 to Port 2 while isolating reflected signals.

A MACOM MA4P7455 digital attenuator chip is employed for output power control. Theoretical calculations, accounting for microstrip and coaxial line losses between components, predict an output power range of 35–53 dBm. The system monitors the output signal power via the circulator; the detected voltage is processed by an ADC circuit, and the MCU employs a PID algorithm to adjust the pre-stage digital attenuator in real-time, thereby achieving precise real-time power control. In addition, measurement uncertainty is introduced by the test setup. Across the 2–3 GHz band, the combined attenuation of all RF cables and interconnects is approximately 2 dB; unless otherwise stated, the reported power levels and efficiency are de-embedded by removing this systematic loss.

TABLE 2. Comparison with state-of-the-art works.

Reference	PAE (%)	Output Power (dBm)	Gain (dB)
[7]	44.4	38.6	18.2
[21]	> 60.2	41.3	11.3
[10]	52.5	45.4	19.0
[22]	44.8	38.7	17.2
This Work	**61.89**	**53.38**	**18.14**

Table 2 compares the proposed cascaded LDMOS microwave source with representative state-of-the-art works. Specifically, while [10] and [21] achieve PAEs above 50%, their output power is limited to the 10–30 W range (45.4 dBm and 41.3 dBm, respectively). In contrast, this work achieves a peak PAE of 61.89% at a significantly higher output power of 53.38 dBm (200 W class) with a practical gain of 18.14 dB. Relative to these prior studies, the proposed architecture provides an improved efficiency-power trade-off by combining deep class-AB operation with second-harmonic waveform control and closed-loop digital power regulation for industrial CW applications.

5. CONCLUSION

This work presents a digitally controlled 2.45 GHz solid-state microwave power source based on a cascaded LDMOS architecture. By adopting deep class-AB biasing and a near-short second-harmonic termination implemented with a lumped-element matching network, the final-stage PA achieves a saturated output power of 54.09 dBm, a gain of 18.14 dB, and a peak PAE of 61.89% under a 28 V supply. At the system level, the closed-loop digital attenuation scheme provides accurate output-power regulation from 35 to 53 dBm with good thermal stability under continuous-wave operation. Future work will include long-duration reliability characterization under representative thermal and load-mismatch conditions, expanded linearity evaluation and mitigation, and load-pull/impedance-trajectory measurements to further validate the second-harmonic optimization and quantify sensitivity to impedance variation and component tolerances.

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