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Compact Reflection-Type Phase Shifter Using an Impedance-Transforming Transdirectional Coupler Based on Double-Shielded Coupled Lines

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ABSTRACT: This paper presents a novel tunable reflection-type phase shifter (RTPS) employing an impedance-transforming transdirectional (IT-TRD) coupler terminated by varactor-based reflective loads. The coupler is based on double-shielded coupled lines (DSCLs) and is implemented as a distributed surface-mount component, providing inherent impedance transformation for increasing the relative phase shift for given varactors. Fabricated using standard PCB technology, the prototype features intrinsic DC isolation between the RF path and control circuits, requiring only a single control voltage. Measured results show that the RTPS operates over a wide frequency band from 2.2 to 2.8 GHz (24%), achieving a tunable phase shift of up to 180° with an insertion loss of 1.3±0.7 dB and a return loss better than 11 dB. The proposed design is characterized by compact physical dimensions of $0.1 \times 0.21\lambda$ at the center frequency.

1. INTRODUCTION

Phase shifters are essential building blocks in beamforming and signal routing networks of modern microwave systems. They are typically categorized into five architectures: loaded-line, switched-line, reflection-type, high-low pass, and vector-sum. A conventional reflection-type phase shifter (RTPS) utilizes a quadrature hybrid terminated by a pair of reflective loads (Fig. 1). These hybrids are typically implemented as branch-line (Fig. 1(a)) or coupled-line couplers, which fall into three types: co-directional (COD), contra-directional (CTD) (Fig. 1(b)), and trans-directional (TRD) (Fig. 1(c)). Notably, the TRD coupler offers distinct advantages for an RTPS implementation, providing intrinsic DC isolation between the radio frequency (RF) path and control circuits, enhanced design flexibility due to the ability to integrate impedance transformation, and more compact layouts compared to traditional solutions.

Conventional branch-line coupler-based RTPS designs face several limitations, including bulky dimensions and the requirement for external DC-blocking capacitors [1, 2]. While coupled-line CTD couplers [3] offer a more compact size, they fail to address the DC isolation issue.

Recent RTPS designs using symmetric coupled-line TRD couplers [4–8] provide intrinsic DC isolation, yet remain suboptimal: those in [4–6] provide a relative phase shift below 180°, while designs in [7, 8] achieve over 360° at the cost of high insertion loss and increased size. Consequently, there is a critical need for an RTPS that combines intrinsic DC isolation with a relative phase shift of at least 180°, low insertion loss, and a compact design. To address these issues, this paper presents an RTPS employing an impedance-transforming double-shielded coupled-line transdirectional (IT DSCL-TRD) coupler, which was introduced in [9] and subsequently developed in [10, 11].

This is the first implementation of such a coupler in a tunable phase shifter design. This solution simultaneously reduces losses and extends the phase-tuning range while maintaining a compact size, even when using standard printed circuit board (PCB) technology.

2. REFLECTION TYPE PHASE SHIFTER MODELING

The modeling of the proposed analog RTPS, utilizing a impedance-transforming DSCL-TRD coupler terminated by two varactor-based reflective loads (Fig. 2), begins with the analysis of the coupler presented in Fig. 2(b).

2.1. Impedance-Transforming DSCL-TRD Coupler

The IT TRD coupler is based on the DSCLs and has a configuration shown in Fig. 3, which illustrates its schematic diagram and geometry. As depicted in Figs. 2(b) and 3, the upper stripline 1 is placed on the reference stripline 2, which acts as an intermediate imperfect shield.

In quasi-static analysis, the primary parameters of the DSCLs are a pair of matrices: capacitances **C** and inductances **L** per unit length [9, 11].

$$\mathbf{C} = \begin{bmatrix} C_{11} & -C_{12} \\ -C_{12} & C_{22} \end{bmatrix} = \begin{bmatrix} C_{12} & -C_{12} \\ -C_{12} & C_{02} + C_{12} \end{bmatrix}_{C_{01}=0} \quad \text{(F/m)} \quad (1)$$

$$\mathbf{L} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} = \begin{bmatrix} L_{01} + L_{12} & L_{12} \\ L_{12} & L_{12} \end{bmatrix}_{L_{02}=0} \quad \text{(H/m)} \quad (2)$$

where C_{11}, C_{22} are self-capacitances of the first and second lines; C_{01}, C_{02}, C_{12} are self-partial and mutual capacities, re-

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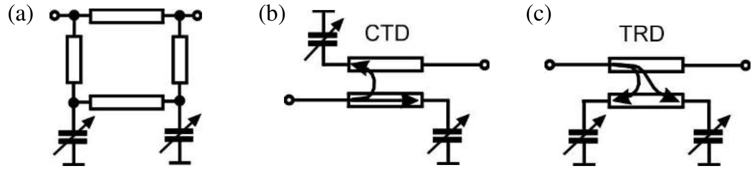

FIGURE 1. Schematics of analog RTPSs employing various 3-dB 90°: (a) branch-line, (b) CTD coupled-line, and (c) TRD coupled-line couplers.

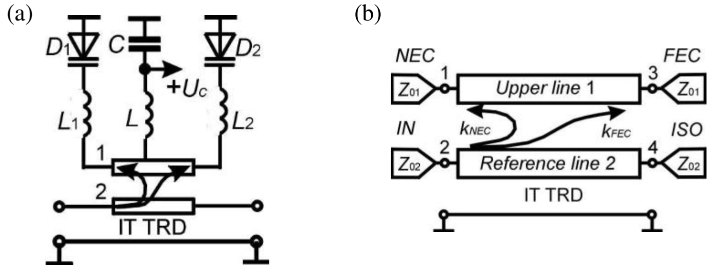

FIGURE 2. (a) Schematic of the proposed analog RTPS implemented with two varactors and (b) the IT DSCL-TRD coupler.

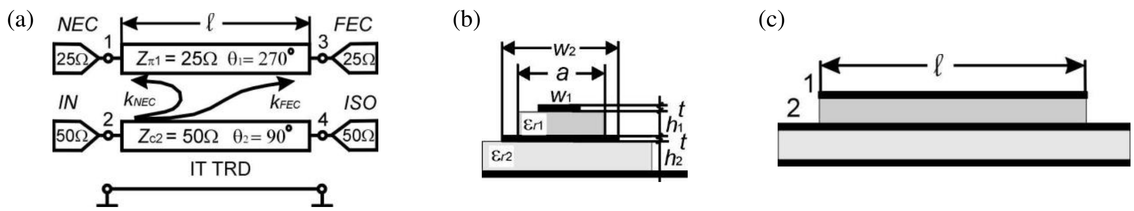

FIGURE 3. IT DSCL-TRD coupler: (a) schematic diagram with specified impedance and electrical length values; (b) cross-sectional and (c) side views showing the geometry.

spectively; L_{11}, L_{22} are self-inductances of the first and second lines; L_{01}, L_{02}, L_{12} are self-partial and mutual inductances, respectively. Perfect double shielding effect in DSCLs occurs when $C_{01} = 0$, $L_{02} = 0$, $C_{11} = C_{12}$, and $L_{22} = L_{12}$.

The secondary parameters are as follows: ε_{rc} and $\varepsilon_{r\pi}$ are the modal effective permittivities of the DSCLs during in-phase (c-mode) and out-of-phase (π-mode) excitations, respectively; R_c and R_π are normalized modal voltages characterizing the voltage ratios on the lines, which in the case of perfect double shielding take the values $R_c = 1$ and $R_\pi = 0$; $Z_{\pi 1}$ and Z_{c2} are the π-mode and c-mode impedances of the first and second lines, respectively, which equal $25\,\Omega$ and $50\,\Omega$ for the perfect double-shielding case, assuming the nominal near-end (NEC) and far-end (FEC) couplings of $NEC = FEC = 3$ dB [9].

As shown in [9–11], the TRD and impedance-transforming properties in the DSCL coupler appear when the difference in modal electrical lengths is 180°, and the ratio is

$$\frac{\theta_1}{\theta_2} = \frac{270^\circ}{90^\circ} = \frac{\sqrt{\varepsilon_{r\pi}}}{\sqrt{\varepsilon_{rc}}} = 3 \tag{3}$$

where θ_1, θ_2 are the electrical lengths of the upper (first) and reference (second) lines, respectively, as shown in Fig. 3(a). Consequently, an impedance-transforming DSCL-TRD coupler can be initially designed using two uncoupled lines with electrical lengths of 270° and 90°, respectively [10].

2.2. Varactor-Based Reflective Load

Varactor-based reflective load and its equivalent circuit are shown in Fig. 4. The modeled load consists of an external inductor L_1 and silicon varactor-diode D_1 (Infineon BB833), the equivalent circuit of which contains the series inductance $L_s = 1.8$ nH, resistance $R_s = 1.8\,\Omega$, and variable capacitance $C_v = (0.8, 1.0, 1.3, 1.8, 2.6, 4, 10)$ pF. Based on $C_{\min}(U_c = 20\,\text{V}) = 0.8$ pF and $C_{\max}(U_c = 0\,\text{V}) = 10$ pF, the harmonic mean capacitance is $C_0 = 2C_{\min}C_{\max}/(C_{\min} + C_{\max}) = 1.48$ pF. For a center frequency of $f_0 = 2.5$ GHz, the total series inductance ($L_0 = L_1 + L_s$) is determined as $L_0 = 1/(\omega_0^2 C_0) = 2.74$ nH. Hence, the external inductance L_1 is calculated as $L_1 = L_0 - L_s = 0.94$ nH.

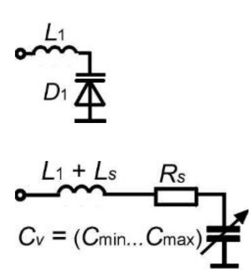

FIGURE 4. Varactor-based reflective load and its equivalent circuit.

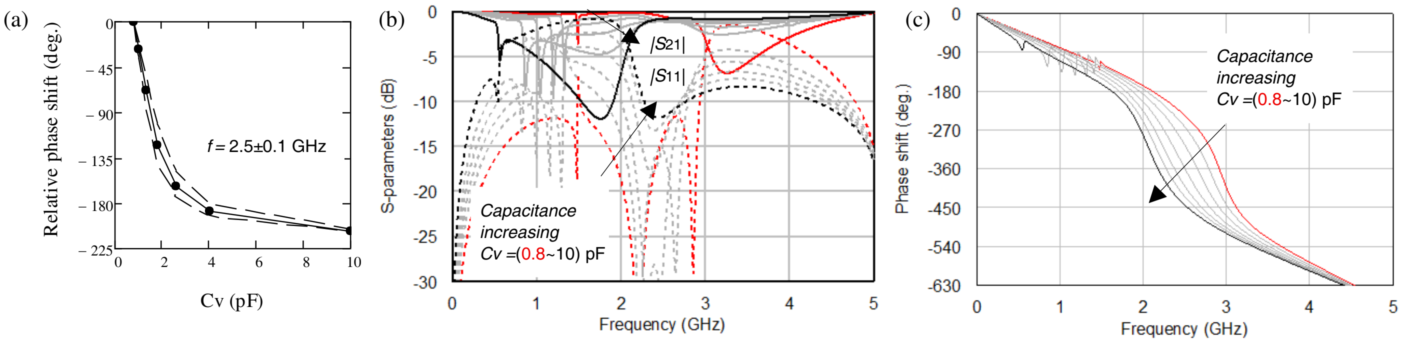

FIGURE 5. Simulation results of the proposed analog RTPS implemented with an IT DSCL-TRD coupler and two reflective loads: (a) relative phase shift at 2.5 GHz versus varactor-capacitance (BB833); (b) magnitude of S_{11} and S_{21}; and (c) phase shift versus frequency for the following varactor capacitances: (0.8, 1.0, 1.3, 1.8, 2.6, 4, 10) pF.

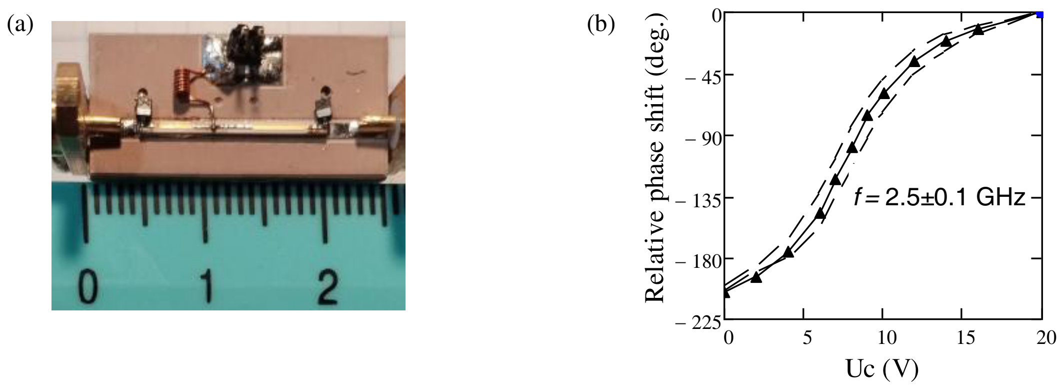

FIGURE 6. (a) Photograph of the proposed analog RTPS; and (b) measured relative phase shift at the center frequency as a function of the control voltage across the varactor diodes.

2.3. RTPS Simulation

Taking into account the capacitance tuning ratio $K_c = C_{\max}/C_{\min} = 10/0.8 = 12.5$, the harmonic mean capacitance $C_0 = 1.48\,\text{pF}$, and the first-line π-mode impedance $Z_{\pi1} = 25\,\Omega$, the maximum phase shift range at the specified frequency $f_0 = 2.5\,\text{GHz}$ can be calculated as follows

$$\Delta\varphi_{\max} = \frac{720^\circ}{\pi}\tan^{-1}\left(\frac{K_c-1}{K_c+1}\cdot\frac{1}{2\pi f_0 C_0 Z_{\pi1}}\right) = 223^\circ \quad (4)$$

which implies that a lower impedance of the varactor-terminated port $Z_{\pi1}$ results in a larger relative phase shift.

To simulate the performance of the proposed RTPS, the primary parameters of the IT DSCL-TRD coupler are first calculated based on the physical design specifications detailed in the next Section 3. Specifically, using the conformal mapping technique implemented in the authors' Lines Modelling Toolbox CAD, the primary parameters of the DSCLs are found to be $(L_{11}, L_{22}, L_{12}) = (0.701, 0.342, 0.256)$ µH/m and $(C_{11}, C_{22}, C_{12}) = (698, 850, 692)$ pF/m. The corresponding secondary modal parameters are $(Z_{\pi1}, Z_{c2}) = (22.6, 54.6)\ \Omega$ and $(R_c, R_\pi, \varepsilon_{rc}, \varepsilon_{r\pi}) = (0.97, -0.22, 4.82, 33.4)$; due to the imperfect shielding ($R_\pi \neq 0$), a full set of six parameters is required, as the simple four-parameter model is insufficient. Fig. 5 illustrates the simulated S-parameters of the proposed analog RTPS. The modeled device operates across a frequency band of 2.28–2.76 GHz, maintaining a return loss (RL) better than 10 dB and an insertion loss (IL) of 0.8 ± 0.6 dB. Fig. 5(a) shows the relative phase shift at 2.5 ± 0.1 GHz as a function of the varactor (BB833) capacitance over the range of 0.8 to 10 pF. At this center frequency, a maximum simulated relative phase shift of 208° is achieved.

3. EXPERIMENTAL RESULTS AND DISCUSSION

To experimentally verify the proposed analog RTPS prototype, a quadrature 3-dB IT DSCL-TRD coupler was first implemented. It features a double impedance ratio ($Z_{c2}/Z_{\pi1} \approx 50/25\,\Omega$) and a triple electrical length ratio ($\theta_1/\theta_2 \approx 270/90^\circ$), in accordance with the theoretical analysis presented above and in [9, 11]. The coupler was fabricated on a 1-mm-thick FLAN-7.2 dielectric substrate ($\varepsilon_{r2} = 7.2$, Moldavizolit, Tiraspol) as PCB with dimensions of $12 \times 25\,\text{mm}^2$. A ceramic bar overlay (MTC-60, $\varepsilon_{r1} = 60$, Magneton Plant, Russia) with a rectangular cross-section ($0.5 \times 0.9\,\text{mm}^2$) and broadside-coupled strips (15 mm) was mounted on the reference stripline 2 (see Fig. 3). The final physical parameters of the coupler design are as follows: $(w_1, w_2, h_1, h_2, h, t, \ell) = (0.3, 1.5, 0.5, 1, 0.02, 15)$ mm; $(\varepsilon_{r1}, \varepsilon_{r2}) = (60, 7.2)$.

A photograph of the fabricated RTPS and its measured relative phase shift versus control voltage at 2.5 ± 0.1 GHz are

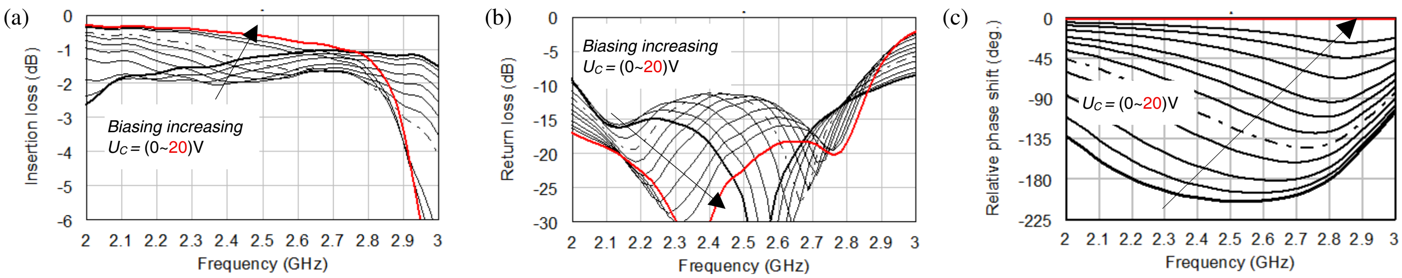

FIGURE 7. Measured RTPS performance: (a) S_{21}, (b) S_{11}, and (c) relative phase shift for the bias: (0, 2, 4, 6, 7, 8, 9, 10, 12, 14, 16, 20) V.

TABLE 1. State-of-the-art of the analog RTPS using 3-dB 90° TRD couplers.

[Ref]	Frequency (GHz)	FBW (%)	IL (dB)	RL_{min} (dB)	Relative phase shift (°)	Type of coupler	Number of varactors/ Material	Varactor range (pF)	Control voltage (V)	Intrinsic DC isolation	Circuit size		
											(mm×mm)	$(\lambda \times \lambda)^*$	(λ^2)
[3]	2.2±0.45	36	2.35±0.85	10	375	CTD	4/GaAs	0.28–2.8	2–20	No	17×20	0.13×0.14	0.018
[2]	2.0±0.1	10	0.54±0.09	12	201	IT BLC	2/GaAs	0.45–2.72	0–20	No	38×60	0.25×0.4	0.100
[4]	4.5±0.8	40	1.0±0.5	10	42	VIP TRD	2/GaAs	0.4–1.7	0–20	Yes	9.5×23	0.14×0.35	0.049
[5]	10.5±1.0	19	2.1±0.9	12	125	VIP TRD	2/GaAs	0.24–0.7	0–40	Yes	12×12	0.42×0.42	0.176
[6]	2.15±0.35	32	0.35±0.32	10	121	TRD	2/GaAs	0.45–2.72	0–20	Yes	14×40	0.1×0.29	0.029
[7]	5.8	<5	4.8±3.1	10	380	VIPC TRD	4/Si	0.31–1.24	0–30	Yes	26×30	0.45×0.77	0.347
[8]	2.0±0.2	20	3.0±1.3	10	425	TRD	4/Si	0.35–3.2	0–20	Yes	15.2×50.7	0.17×0.56	0.095
This work	**2.5±0.3**	**24**	**1.3±0.7**	**11**	**180**	**IT DSCL-TRD**	**2/Si**	**0.8–10**	**0–20**	**Yes**	**12×25**	**0.1×0.21**	**0.021**

*λ: free-space wavelength at the center frequency; CTD: contra-directional coupler; IT BLC: impedance-transforming branch-line coupler; VIP TRD: vertically installed planar transdirectional coupler; VIPC TRD: vertically-installed planar-capacitive transdirectional coupler; IT DSCL-TRD: impedance-transforming transdirectional coupler based on double shielded coupled lines.

shown in Fig. 6. Within this 200-MHz bandwidth and a 201° phase range, phase variations for different control voltages remain below ±15°. The RTPS was measured using a Planar S5048 VNA, showing a good agreement between simulations and measurements (Fig. 7).

Over the 2.2–2.8 GHz (24%) band, the device provides a 0–180° phase shift with an IL of 1.3 ± 0.7 dB and RL > 11 dB across all phase states.

Table 1 compares the proposed RTPS using an IT DSCL-TRD coupler with state-of-the-art designs. The results demonstrate that the proposed solution achieves a favorable balance among insertion loss, tuning range, circuit size, and fabrication complexity. The proposed RTPS occupies a physical area of only 12×25 mm^2, which translates to an electrical size of $0.021\lambda^2$. This is significantly more compact than most varactor-based designs, such as [7] and [8], and although design [3] shows slightly smaller dimensions, it lacks intrinsic DC isolation. Unlike designs [3, 7, 8], which require four varactors to achieve wide phase shifts, the proposed design achieves a 180° relative phase shift using only two Si varactors within a simplified topology. The measured IL of 1.3 ± 0.7 dB is competitive, particularly compared to [3, 8], although lower IL can be achieved by using more expensive GaAs varactors, as in [6]. The proposed RTPS provides intrinsic DC isolation, eliminating the need for external DC-blocking capacitors required in [2, 3].

4. CONCLUSION

A compact, tunable RTPS based on an IT DSCL-TRD coupler terminated by Si varactor-based reflective loads has been presented. Utilizing DSCLs for the TRD coupler enables inherent impedance transformation and high integration in a surface-mount format. Fabricated via standard PCB technology, the prototype achieved a 180° phase shift over a 24% bandwidth (2.2–2.8 GHz). With an IL of 1.3 ± 0.7 dB and RL > 11 dB, the design maintains high performance within a compact size of $0.021\lambda^2$. Its simplified single-voltage control and intrinsic DC isolation make this RTPS an excellent candidate for modern phased-array systems and RF front-ends.

ACKNOWLEDGEMENT

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APPENDIX A.

The phase of the RTPS is controlled by varying the impedance of the reflective load $X_L = (X_{\min} \ldots X_{\max})$, i.e., by varying the capacitance of voltage-controlled varactors with capacitance tuning ratio $K_c = C_{\max}/C_{\min}$. The resulting phase variation of the RTPS is equal to the phase variation of the reflection coefficient [1], and its absolute value is given by

$$\Delta\varphi_{\max} = 2\left[\tan^{-1}\left(\frac{X_{\max}}{Z_0}\right) - \tan^{-1}\left(\frac{X_{\min}}{Z_0}\right)\right]$$
$$= 4\tan^{-1}\left(\frac{X_{\max}}{Z_0}\right)$$

where $X_{\max} = \omega_0 L_0 - \frac{1}{\omega_0 C_{\max}}, \quad X_{\min} = \omega_0 L_0 - \frac{1}{\omega_0 C_{\min}}$. The series inductance is defined as $L_0 = 1/(\omega_0^2 C_0)$, where the harmonic mean capacitance is given by

$$C_0 = 2C_{\max}C_{\min}/(C_{\min} + C_{\max}).$$

Substituting C_0 into the expression for $X_{\max}$ yields

$$X_{\max} = \frac{1}{\omega_0 C_0}\left(1 - \frac{C_0}{C_{\max}}\right) = \frac{1}{\omega_0 C_0}\left(\frac{C_{\max} - C_{\min}}{C_{\max} + C_{\min}}\right)$$
$$= \frac{1}{\omega_0 C_0}\left(\frac{K_c - 1}{K_c + 1}\right)$$

which enables the maximum phase shift range at the specified frequency to be rewritten as

$$\Delta\varphi_{\max} = 4\tan^{-1}\left(\frac{X_{\max}}{Z_0}\right) = 4\tan^{-1}\left(\frac{K_c - 1}{K_c + 1}\cdot\frac{1}{\omega_0 C_0 Z_0}\right)$$

This equation is equivalent to (4) in the main text.

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