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TGV-Based Calibration Standards for D-Band Terahertz Measurements

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ABSTRACT: Owing to glass's excellent electrical properties and stability, Through-Glass Via (TGV) technology is regarded as a key technology for next-generation three-dimensional integration. Research on TGV-based transmission structures and Substrate-Integrated-Waveguide (SIW) structures has been relatively extensive. However, the investigated frequency range remains limited, rarely exceeding 100 GHz, and studies focusing on the intrinsic characteristics of the vias are still lacking. To address this issue, this study designs a set of TGV calibration standards operating in the D-band to extract the S-parameters and electrical parameters of the vias and to analyze their performance, thereby providing useful insights for the subsequent design of TGV devices in the terahertz band.

1. INTRODUCTION

In recent years, three-dimensional integrated packaging technology has attracted significant attention, and glass and glass-ceramics have gradually entered the spotlight [1–3]. Correspondingly, Through-Glass Via (TGV) technology has also seen significant advancements. Various TGV fabrication methods have been developed, including mechanical drilling, laser drilling, and hybrid technologies that combine wet etching with laser drilling [4], all of which benefit from the excellent electrical properties of glass. The emergence of TGV aims to address several challenges associated with traditional Through-Silicon-Via (TSV) technology [5], such as high signal loss in silicon substrates leading to degraded high-frequency or high-speed signal transmission performance, as well as high manufacturing costs and complex processes inherent to silicon-based technologies [6–8]. Currently, numerous components, packages, and interposer technologies have been successfully developed using glass substrates [9–11]. Fig. 1 shows the TGV's fundamental structure.

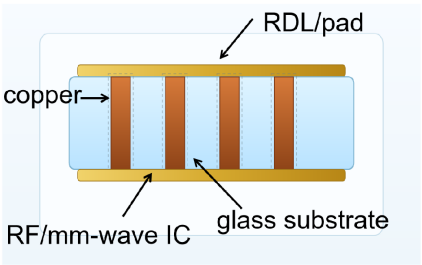

FIGURE 1. Cross-sectional schematic of the TGV structure.

Figure 2 shows CPW-CPW (coplanar waveguide) and GCPW-GCPW (ground coplanar waveguide) structures, as well as the equivalent circuit model, which constitutes the fundamental design architectures for TGV devices. For the CPW-CPW designs developed in this study, the corresponding calibration and de-embedding standards were designed to extract the via's parameters.

The second section discusses principles of the D-band calibration. The third section focuses on the design and algorithmic validation of the de-embedding standards. The fourth section presents conclusions.

2. DESIGN APPROACH FOR D-BAND CALIBRATION

The expressions for physical quantities in Fig. 2(b) are as follows [12].

The TGV's resistance and inductance formulas are given as follows:

$$R_{dc} = \frac{\rho h}{\pi r^2} \tag{1}$$

$$R_{ac} = \frac{\rho h}{2\pi r\delta} \cdot k \tag{2}$$

$$R_{TGV} = \sqrt{R_{ac}^2 + R_{dc}^2} \tag{3}$$

$$L_{TGV} = \frac{\mu_0 h}{2\pi} \ln\left(\frac{p-r}{r}\right) \tag{4}$$

where h and r denote the vias' height and radius, respectively; p represents the spacing between signal TGV and ground TGV; k represents the proximity effect; and δ is the skin depth.

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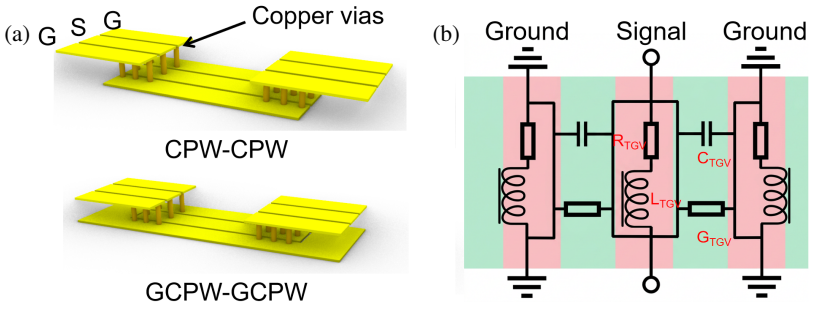

FIGURE 2. (a) CPW-CPW structure and GCPW-GCPW structure. (b) Equivalent circuit model.

The expressions for capacitance and conductance are given as follows:

$$C_{TGV} = \frac{\pi \varepsilon_0 \varepsilon_{glass} h}{\ln\left(\frac{p}{r}\right)} \tag{5}$$

$$G_{TGV} = 2\pi f C_{TGV} \tan\delta \tag{6}$$

where $\tan\delta$ is the dielectric loss tangent.

The TGV calibration devices we designed operate in the frequency range of 110 GHz to 170 GHz to extract loss characteristics of through-vias in CPW-CPW structures. In on-wafer electrical testing, short-open-load-through (SOLT) and through-reflect-line (TRL) calibration are the most commonly used calibration methods. However, while SOLT calibration performs well in low-frequency ranges, its high precision requirements for parameters lead to poor calibration performance at higher frequencies (above 100 GHz). In contrast, TRL calibration demonstrates superior performance in this frequency band; thus, TRL calibration is adopted for the initial calibration process. For the subsequent extraction of TGV via parameters and loss analysis, the L-2L method and Open-Short method referenced in the literature are employed [13].

In TRL calibration, the Thru, Line, and Reflect standards are used to establish a through-transmission reference, provide an additional propagation phase shift, and supply reflection information, respectively. The Thru standard is typically a short through transmission line used to determine the transmission relationship between the two ports and to define the calibrated reference planes. The Line standard has the same transmission-line structure and characteristic impedance as the Thru standard, but with an additional length. The electrical-length difference between the Line and Thru standards introduces the required phase shift, which is then used to solve for the propagation constant and the transmission-related systematic errors. The Reflect standard is usually implemented as an open or short structure, providing a strong reflection signal to help determine port reflection-related error terms. By combining these three standards, the systematic errors introduced by the measurement system, probes, and interconnect structures can be effectively removed, and the measurement reference planes can be shifted to the ports of the device under test. Design dimensions of the CPW-CPW structure were 108 µm for the signal line and 15 µm for the gap, ensuring 50-ohm impedance matching. The pitch of our probe is 100 µm, so the ground line design must ensure that the probe tip can make proper contact with the calibration standard.

For TRL calibration, its core principle relies on the length difference between two transmission lines for computation. Constrained by the phase requirements, the phase difference between the two transmission lines must be within 20°–160° to allow for TRL calibration [14, 15]. For broadband calibration, multiple transmission lines may be required. Generally, if the ratio of the terminal frequency to the starting frequency exceeds eight, multiple transmission lines are required. Given our frequency range of 110–170 GHz, theoretically, two transmission lines are sufficient. However, to improve the calibration accuracy, we designed four transmission lines of varying lengths.

For the D-band, the center frequency is 140 GHz. With a substrate relative permittivity of 4.29 and an effective dielectric constant of approximately 2.65, the optimal length difference between the Thru and Line standards can be calculated. Considering the L-2L calibration method used in the subsequent analysis, four transmission lines with lengths of 400 µm, 715 µm, 800 µm, and 958 µm were ultimately designed in this work. The shortest transmission line was used as the Thru standard, while the remaining lines were defined as L1-L3 in order of increasing length.

3. DESIGN AND PARAMETER EXTRACTION OF TGV DE-EMBEDDING STRUCTURES

3.1. De-Embedding Calibration Standards Design

The paper [13] mentions two methods for TGV de-embedding calibration: the L-2L method and the Open-Short method. Compared to the TRL calibration discussed earlier, these methods further shift the reference plane, as shown in Fig. 3.

The following section explains two de-embedding methods:

(1) L-2L Method

By converting the measured S-parameter matrix into an $ABCD$ parameter matrix, the following relationship was established:

$$ChainL = TGV * Trace * TGV \tag{7}$$

$$Chain2L = TGV * Trace * Trace * TGV \tag{8}$$

where *Trace* represents the $ABCD$ matrix of a transmission line with a length of L, and $Trace * Trace$ represents the

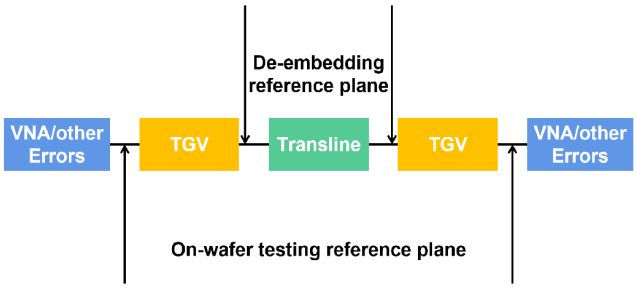

FIGURE 3. Comparison of reference planes between de-embedding testing and on-wafer testing.

$ABCD$ matrix of a transmission line with a length of $2L$. Based on the above two equations, we can derive:

$$TGV = \left(\sqrt{ChainL^{-1} \times Chain2L \times ChainL^{-1}}\right)^{-1} \quad (9)$$

(2) Open-Short Method

For this method, the Y-matrix representation is used.

$$Matrix1_Y = Thru_Y - Open_Y \quad (10)$$

$$Matrix2_Y = Short_Y - Open_Y \quad (11)$$

Next, the two obtained Y-parameter matrices are converted into Z-parameter matrices, and the Z-parameter matrix of the bottom transmission line is derived.

$$Trace_Z = Matrix1_Z - Matrix2_Z \quad (12)$$

The Z-parameter matrix of the transmission line can be converted from the $ABCD$ matrix. Based on this, we can derive the following:

$$TGV = \sqrt{Thru * Trace} * Trace^{-1} \quad (13)$$

The above describes the principles of the two de-embedding methods used in this study. The device design structures are shown in Fig. 4.

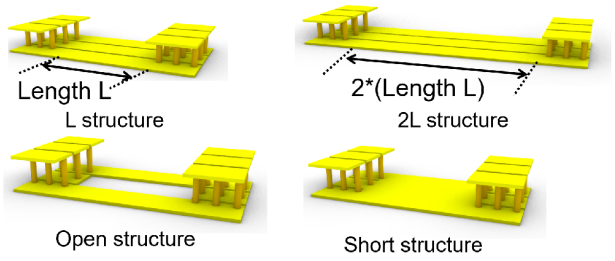

FIGURE 4. De-embedding structures.

3.2. Fabrication

The proposed D-band transmission calibration standards were fabricated on a 200-µm-thick BF33 glass wafer using a tailored through-glass-via (TGV) process. The BF33 glass used in this work has a relative permittivity (ε_r) of 4.29 and a dielectric loss tangent ($\tan\delta$) of 0.01 at D-band frequencies, as provided by the manufacturer and verified by our own material characterization. The fabrication sequence, as shown in Fig. 5, comprised the following key steps:

a. Wafer Pretreatment: The glass wafer was thoroughly cleaned in a piranha solution (H_2SO_4:H_2O_2 = 3:1) to remove organic contaminants and to hydroxylate the surface, promoting adhesion for subsequent layers.

b. Laser Drilling: Laser ablation was first employed to locally modify material properties in the via region. Through-glass vias (TGV) with a target diameter of 20 µm were patterned using an ultraviolet laser drilling system. According to process reliability requirements, minimum center-to-center spacing between adjacent vias was set at 40 µm, because a smaller spacing would drastically elevate the risk of glass cracking. In this work, the vias were primarily used for the vertical interconnection of transmission lines; additionally, the mode matching and crosstalk of high-frequency signals between adjacent vias had to be taken into consideration. For these reasons, the practical minimum spacing adopted in this study was 60 µm.

c. Wet Etching: A brief wet etching step in a diluted high-frequency (HF)-based solution was performed to smooth via sidewalls, remove laser-induced micro-cracks, and slightly widen the via diameter to the final dimension. It should be noted, however, that the diameter of the glass vias was not always precisely 20 µm, as it depended on the accurate control of the etching duration. In some cases, the via diameter was slightly enlarged, or over-etching occurred in a specific direction, leading to an elliptical shape and a reduction in circularity. This was considered a normal phenomenon in the fabrication process. Fig. 5 presents the measured data regarding the circularity and diameter of the fabricated vias.

d. Seed Layer Deposition (both sides): A conformal adhesion layer of Ti (60 nm) followed by a Cu seed layer (300 nm) was deposited on both sides of the wafer using magnetron sputtering, ensuring continuous coverage inside via holes. This bilateral deposition improved the uniformity of the seed layer along the entire via depth.

e. Cu Electroplating (both sides): After seed layer deposition, a copper electroplating process was carried out on both sides of the wafer to fill TGVs. By optimizing the electroplating duration and current density, void-free filling is achieved. To ensure sufficient filling of copper within vias, an over-plating technique was adopted, resulting in an excess copper layer covering the entire surface on both sides.

f. Chemical-Mechanical Polishing (CMP): Due to the over-plated copper, CMP was used to polish and remove the excess copper layer from both surfaces of the glass wafer. The overall mechanical strength of the glass wafer was considerably compromised after via drilling and metal filling; therefore, the mechanical pressure applied during the CMP process had to be precisely controlled, and removing excess metal was achieved primarily by chemical polishing. Through careful control of the polishing parameters, only the copper posts inside the TGVs were retained to protrude approximately 1 µm above the glass surface, while the rest of the copper on the wafer surfaces was completely removed. In other words, the final height of copper posts — i.e., the metal filling inside the vias — protruded approximately 1 µm above the glass surface. This design was intended to accommodate the

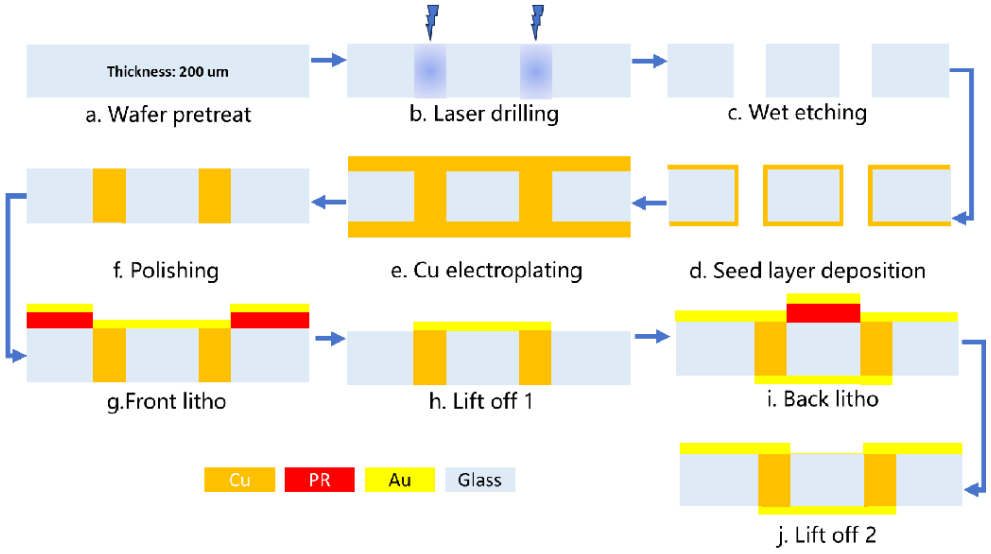

FIGURE 5. Process flow: A sequence of steps for fabricating glass vias and metallizing the through-vias, as well as the transmission lines on the glass surface.

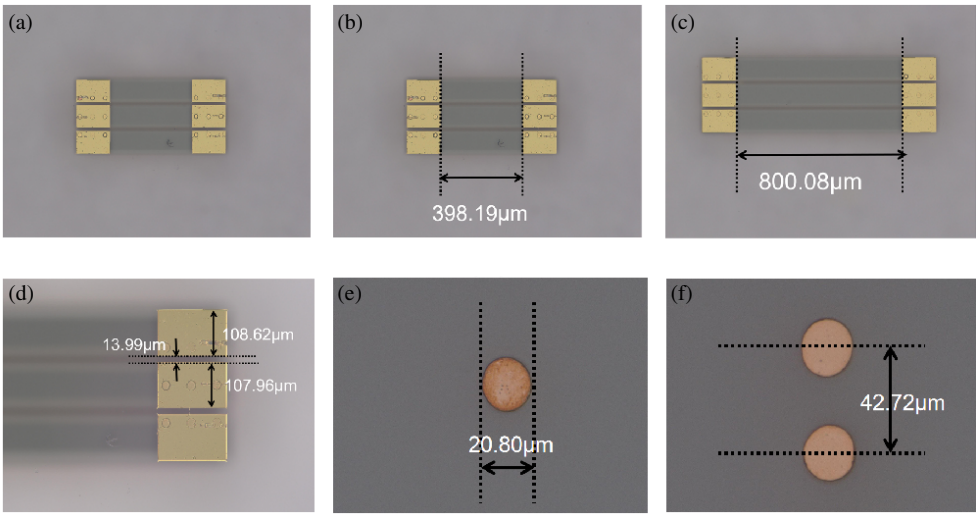

FIGURE 6. (a) CPWs' de-embedding L structure, (b) dimension drawing of CPW de-embedding L structure, (c) dimension drawing of CPW de-embedding 2L structure, (d) dimension drawing of pad of L-structure, (e) dimension drawing of via diameter, and (f) dimension drawing of adjacent via pitch.

mismatch in thermal expansion coefficients between metal and glass, thereby preventing an open circuit between the in-via metal and planar metal transmission lines caused by the recession of the in-via metal below the glass surface due to temperature variations.

g. & h. Front-Side Patterning (Lithography & Lift-off): A positive photoresist was patterned on the front side to define CPW traces. Subsequently, a bilayer of Ti/Au (60 nm/400 nm) was deposited via e-beam evaporation, followed by a lift-off process to form the final front-side metallization.

i. & j. Back-Side Patterning (Lithography & Lift-off): The wafer was then flipped over, and a similar photolithography and lift-off process was applied to the back surface to fabricate CPW transmission line structures there. This connected the transmission lines on the top surface, the glass vias, and the transmission lines on the bottom surface as an integrated vertical interconnection structure incorporating two sets of TGVs.

The completed devices were subsequently characterized in terms of their dimensions, as shown in Fig. 6. The fabricated devices matched the targeted design dimensions, indicating good fabrication quality.

3.3. Simulation

Electromagnetic simulations were performed for the proposed structures to evaluate their practical performance in the D-band and to verify the feasibility of the design approach. In the simulation model, the BF33 glass substrate was assigned a relative permittivity of 4.29 and a loss tangent of 0.01, consistent with the actual material properties. The electrical parameters of gold and copper were adopted from the material library. Both

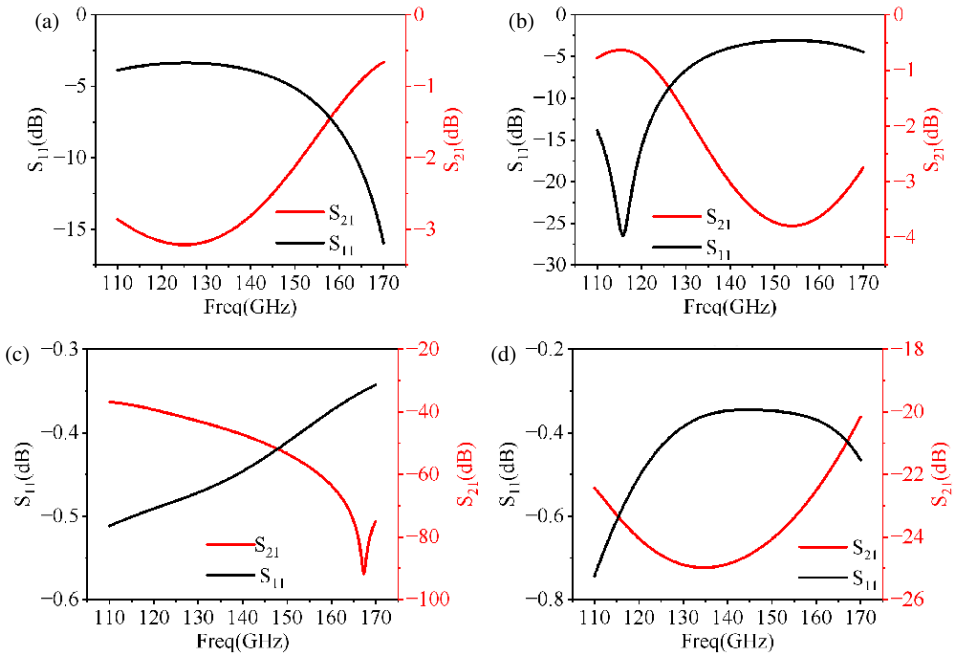

FIGURE 7. Device simulation results. (a) L structure, (b) 2L structure, (c) short structure, and (d) open structure.

materials possess a relative permittivity of 1 and a dielectric loss tangent of 0. The bulk conductivities of the two materials are 5.8×10^7 S/m and 4.1×10^7 S/m. Regarding the port settings, we adopted a lumped port, with the integration line directed from the signal line to the ground line. The surrounding air region was extended outward by one quarter of the center wavelength. The corresponding simulated results are shown in Fig. 7. For the transmission-line devices (L/2L structure), the insertion loss of both structures remains below 5 dB across the entire D-band, indicating relatively low power dissipation. More importantly, the insertion loss is further reduced to approximately 2.5 dB in certain frequency ranges, suggesting improved impedance matching and lower loss in these bands, and hence higher transmission efficiency. These results also indicate that the overall behavior of the designed transmission-line structures is consistent with expectations. Meanwhile, the simulations of the reflect structures (Open/Short structure) exhibit responses in good agreement with the design targets. The open- and short-terminated cases follow expected trends and provide stable reference reflection states, which is beneficial for subsequent calibration and parameter extraction.

It is worth noting that, for conventional TRL calibration, the S_{21} of the Thru standard is expected to approach 0 dB. However, according to the data in Fig. 7, S_{21} does not reach this value. This is because, in the D-band, the vias introduce significant loss; therefore, the measured S_{21} largely reflects the vias' influence. This is precisely why de-embedding methods are required to extract the via parameters.

In summary, the proposed devices achieved satisfactory performance in the D-band: transmission structures exhibited low loss; reflective structures behaved as expected; and no abnormal features were observed in the overall frequency response. Therefore, this set of structures can serve as baseline test vehicles for subsequent via-related calibration and support further parameter extraction, facilitating the development of accurate high-frequency models.

3.4. Results

We organized electromagnetic simulation data of the aforementioned structures and, based on these results, extracted the via scattering parameters using the L-2L method. The results are shown in Fig. 8. Overall, the via S_{21} remains higher than -1 dB across the entire D-band, indicating a low insertion loss within the target frequency range. In other words, the signal experiences limited attenuation when passing through the via, demonstrating a good transmission capability. This also indirectly confirms the rationality of the proposed device design and provides a reliable basis for subsequent via interconnect applications. Subsequently, extracted S-parameters were converted into corresponding RLGC electrical parameters, and their frequency-dependent behavior is shown in Fig. 9. Here, R and G represent the contributions of conductor loss and di-

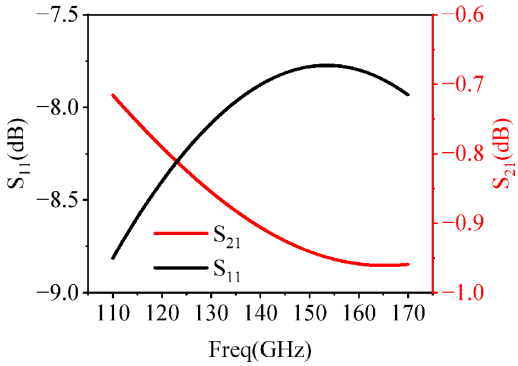

FIGURE 8. Extracted vias S-parameters.

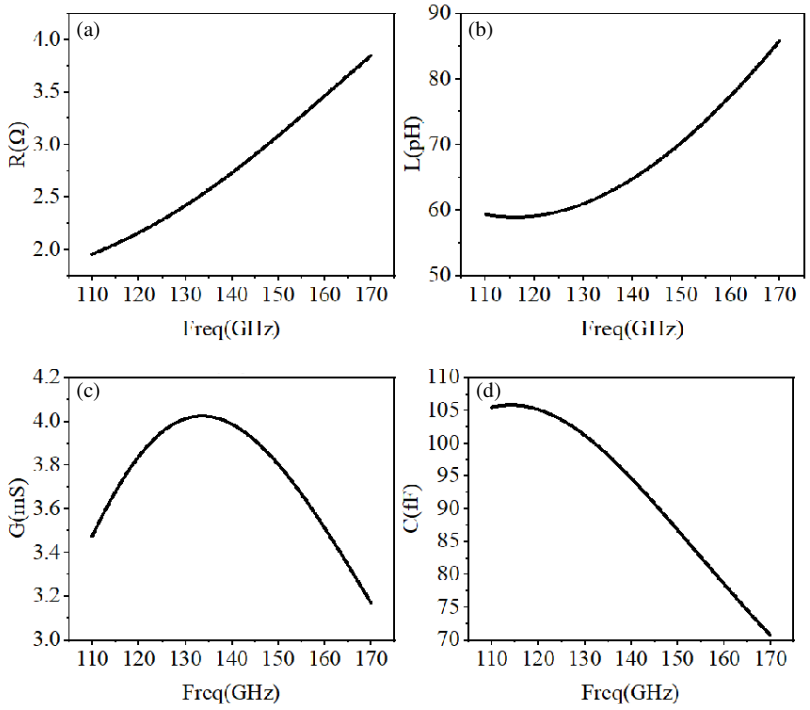

FIGURE 9. RLGC parameters of the vias.

TABLE 1. Data comparison table.

Freq. (GHz)	R (ohm)	L (pH)	G (mS)	C (pF)	S_{21} Extraction (dB)	S_{21} Calculation (dB)
110	1.95	59.33	3.47	0.11	−0.71	−0.72
120	2.16	59.10	3.84	0.11	−0.79	−0.79
130	2.42	60.98	4.01	0.10	−0.85	−0.86
140	2.73	64.75	3.99	0.09	−0.9	−0.91
150	3.08	70.33	3.80	0.08	−0.94	−0.94
160	3.47	77.47	3.51	0.08	−0.95	−0.96
170	3.85	85.84	3.16	0.07	−0.96	−0.96

TABLE 2. Some recent research progress.

Ref.	Via Type	Freq.	Comment	Parameter extraction
[16]	TSV	300 kHz–20 GHz	S-parameters	S_{21} 0.88 dB
[17]	TSV	1–40 GHz	Capacitance	Capacitance 1 GHz 140 fF 40 GHz 20 fF
[13]	TSV	100 kHz–30 GHz	S-parameters Capacitance	S_{21} 0.4 dB 30 GHz 30 fF
This work	TGV	110–170 GHz	S-parameters Capacitance	S_{21} 2.5 dB 170 GHz 70 fF

electric loss, respectively, and L and C are closely related to the parasitic inductance and capacitance introduced by the via and its surrounding structures. Frequency distributions of the RLGC parameters enable a more intuitive assessment of how losses and parasitic effects evolve with frequency, providing a basis for developing high-frequency models suitable for circuit simulation and further structural optimization and design refinement. Finally, using Eqs. (1)–(6), the extracted parameters were substituted into the simplified equivalent circuit to obtain the corresponding S_{21} values, which were then compared

with the extracted S_{21} results. As shown in Table 1, the two sets of results are in close agreement, indicating the validity of parameter extraction.

To demonstrate the advantages of the proposed device, Table 2 compares the performance and parameter extraction results of similar interconnect structures.

4. CONCLUSION AND FUTURE WORK

This study proposes D-band transmission structures for calibration and de-embedding. Using structural matching and dimension optimization within the target frequency band, the corresponding devices were designed and subsequently evaluated via simulation. The simulation results indicate good transmission performance, which is consistent with expectations. In future work, we will optimize fabrication process and experimentally test devices to obtain measured data, thereby making proposed structures more convincing.

Overall, the study and device designs presented in this paper support the development of high-frequency TGV technology. Future work will focus on designing more TGV devices and optimizing fabrication processes to improve device performance, while extending the proposed approach to higher-frequency bands.

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