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Analysis and Design of a Soft-Switched DDC Cell Converter with Enhanced Power Quality

Mirza J. Baig* and Rishi K. Singh

Department of Electrical Engineering, Maulana Azad National Institute of Technology, Bhopal, India

ABSTRACT: This article presents an improved power quality (IPQ) soft-switched diode-driven capacitor (DDC) cell converter for high-gain DC-DC conversion applications. The modified sixth-order DDC cell converter offers several advantages over conventional designs, including a common ground configuration, reduced pulsating source current, non-inverted output voltage, and a high voltage gain of $(1 + D)/(1 - D)$. A single-capacitor auxiliary circuit is employed to facilitate soft-switching operation by reducing switching stress and minimizing switching losses. The proposed converter achieves zero-voltage switching (ZVS) and zero-current switching (ZCS) conditions without significantly increasing circuit complexity or auxiliary component count. Comprehensive steady-state and small-signal analyses are carried out and validated through MATLAB/Simulink simulations and a 600 W experimental prototype. Experimental results demonstrate improved efficiency, reduced voltage stress, and enhanced input-side power quality with input current THD limited to 3% under rated operating conditions. Owing to its simple structure, reduced switching losses, and high voltage gain capability, the proposed converter is suitable for high-performance DC-DC power conversion applications.

1. INTRODUCTION

High-gain DC-DC converters are widely used in modern power electronic applications, such as renewable energy systems, battery energy storage, electric vehicles, and regulated DC power supplies. Conventional boost converters are commonly employed for voltage step-up applications because of their simple structure and ease of control. However, achieving high voltage gain using conventional boost converters requires operation at extremely high duty ratios, which increases conduction losses, voltage stress, switching losses, and electromagnetic interference (EMI) [1, 2].

To overcome these limitations, several high-gain converter topologies employing switched capacitors, coupled inductors, voltage multiplier cells, and soft-switching techniques have been reported in the literature [3–6]. Among these methods, soft-switching techniques are particularly attractive because they reduce switching losses and voltage stress while enabling high-frequency operation with improved efficiency. Zero-Voltage Switching (ZVS) is achieved when a semiconductor device is turned ON under zero or near-zero voltage conditions, whereas Zero-Current Switching (ZCS) is achieved when the device is turned OFF under zero or near-zero current conditions [6]. Nevertheless, many existing soft-switched converters require multiple auxiliary switches, inductors, resonant tanks, or complex control circuits, which increase converter complexity and component count [3–5].

The diode-driven capacitor (DDC) cell-based fifth-order boost converter reported in [9] offers several attractive features, such as high voltage gain, low input current ripple, common ground configuration, and non-inverted output voltage. The topology is derived from the Single-Ended Primary Inductor Converter (SEPIC) and utilizes a DDC cell to enhance voltage gain while preserving improved input current characteristics. However, the converter reported in [9] operates under hard-switching conditions, resulting in switching losses and increased device stress at higher switching frequencies.

To address these limitations, this paper presents a soft-switched DDC cell converter based on the topology reported in [9]. An auxiliary capacitor (C_1), connected in parallel with the main switch, is incorporated to facilitate soft-switching operation by reducing voltage-current overlap during switching transitions. The auxiliary capacitor assists in achieving ZVS and ZCS conditions without significantly increasing circuit complexity or auxiliary component count. Although C_1 participates in switching transition intervals, its average current over one switching cycle is zero under continuous conduction mode (CCM); therefore, the steady-state voltage conversion ratio remains unchanged.

The major contributions of this work are summarized as follows:

- Development of a soft-switched DDC cell converter derived from the topology presented in [9] by connecting an auxiliary capacitor C_1 in parallel with switch S_1
- Reduction of switching losses and switching stress using a single auxiliary capacitor.
- Achievement of ZVS and ZCS operation with minimal auxiliary circuitry.
- Improved input-side power quality with low source current THD.

* Corresponding author: Mirza Jawad Baig (213113005@stu.manit.ac.in).

- Validation of converter operation through steady-state analysis, small-signal modelling, MATLAB/Simulink simulations, and experimental verification using a 600 W prototype.

The remainder of this paper is organized as follows. Section 2 presents the operating principle and steady-state analysis of the proposed converter and also discusses small-signal modelling and controller design. Experimental validation and performance analysis are presented in Section 3, followed by conclusions in Section 4.

2. MODES OF OPERATION OF SOFT-SWITCHED DDC CELL CONVERTER AND ITS ANALYSIS

The whole system design is shown in Fig. 1, where the AC to DC supply conversion is accomplished by a bridge rectifier as shown in Fig. 2 and then by filters L_f and C_f. A soft-switched boost converter is the next component in the circuit. To get the required output, closed-loop operation is used to regulate the primary switch S_1. A 6th-order soft-switched DDC cell boost converter [9] is represented by the circuit's latter half, excluding the control section. With the inclusion of the DDC-cell, the SEPIC's buck-boost voltage gain function becomes boost while maintaining its low ripple content characteristic. Fig. 3(a) illustrates a 6th-order soft switched DDC cell boost converter, and Fig. 4 depicts its ideal waveforms. The suggested circuit decreases voltage stress across the switch, maintains the ability of the SEPIC to have minimal supply current ripple, has a common ground, and has an output voltage that is not reversed. Fig. 7 depicts the control circuit for the modified DDC cell converter, where the proportional-integral (PI) controller is used to maintain a constant output voltage.

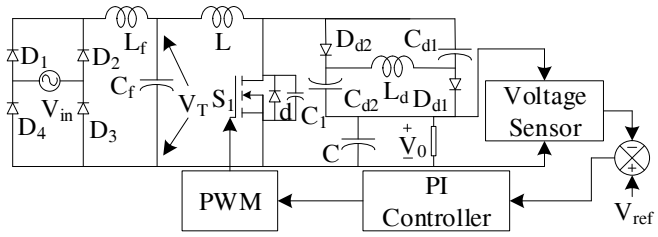

FIGURE 1. Schematic of system.

2.1. Analysis of Diode Bridge Rectifier

Figure 2 shows the diode bridge rectifier used at the input stage. The values of the filter inductor L_f and filter capacitor C_f are calculated as follows.

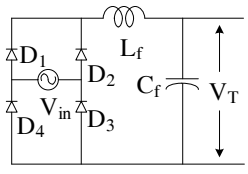

FIGURE 2. Diode bridge rectifier.

Input voltage is given as follows

$$V_{in} = V_m \sin \omega t$$
$$V_{in} = 230\sqrt{2} \sin \omega t \quad (1)$$

Filter capacitor (C_f) is calculated as [10]

$$C_{f\,\max} = \frac{I_{p\,k}}{\omega\, V_{pk}} \tan\theta = \left(\frac{P_{OUT}\sqrt{2}/V_{IN}}{\omega\, V_{IN}\sqrt{2}}\right) \tan\left(\cos^{-1} DPF\right) \quad (2)$$

C_f=580 nF

where θ is the change in the angular relationship between the maximum input voltage and the maximum current of the diode bridge rectifier, and the line frequency is computed as $\omega = 2\pi f$. The formula used to determine the maximum filter capacitance $C_{fmax's}$ is given in [10]. DPF is the displacement power factor.

Filter inductor (L_f) is calculated as [10]

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f}$$
$$L_f = 2\,\text{mH} \quad (3)$$

The output of the diode bridge rectifier can be calculated as

$$V_T = \frac{2V_m}{\pi}$$
$$V_T = 198.4\,\text{V} \quad (4)$$

2.2. Steady State and Time Domain Analysis of DDC Cell Converter

Figure 3(a) depicts the presented converter [9]. Figs. 3(b) & (c) illustrate how it operates. By adding a diode-driven capacitor (DDC) cell that displays a high voltage gain, the typical SEPIC [8] is basically the basis for the sixth-order boost converter that is being described. Here, the DDC cell's insertion converts the SEPIC's buck-boost voltage gain function into a boost mode while maintaining the low ripple content characteristic [9]. The converter that is being presented contains six energy-storing components, which add to the system's sixth order. These components include four capacitors and two inductors. An additional capacitor (C_1) is connected in parallel to the switch and improves power quality and soft switching. Although C_1 participates in switching transition intervals, its average current over one switching cycle is zero under continuous conduction mode (CCM); therefore, the steady-state voltage conversion ratio remains unchanged. Two operating modes are available for the Soft-Switched 6th-order (DDC) Cell Converter (equivalent circuit shown in Fig. 3(a)): Mode I (equivalent circuit shown in Fig. 3(b)) and Mode II (equivalent circuit in Fig. 3(c)). For the steady state study of the DDC-driven soft switch 5th-order converter, the following hypotheses were made.

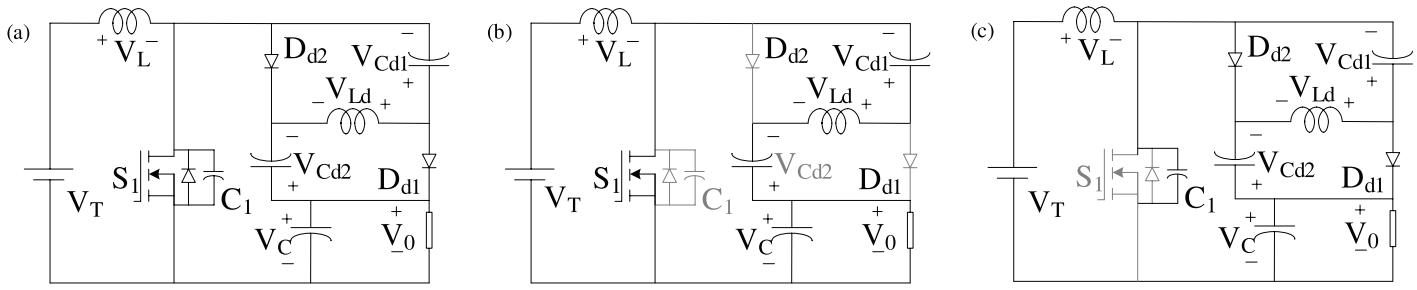

FIGURE 3. (a) Modified DDC cell converter, (b) equivalent circuit of mode-I, and (c) equivalent circuit of mode-II.

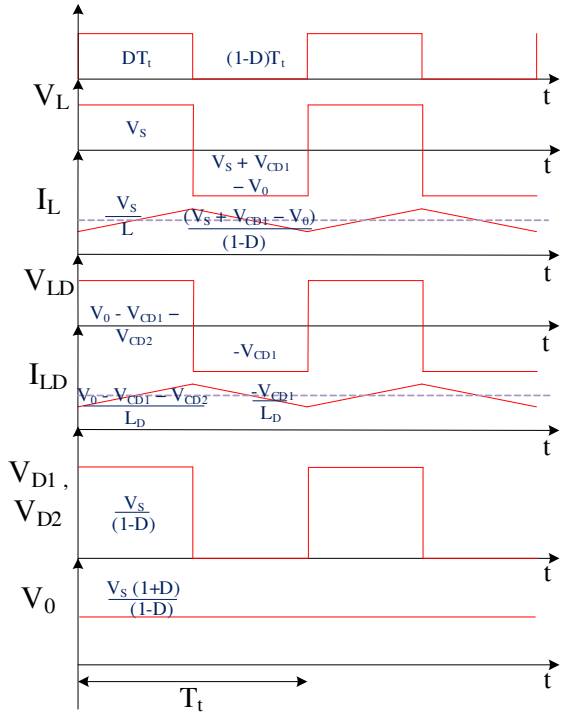

FIGURE 4. Ideal waveform for DDC cell converter.

1. In comparison to the switching time period, the circuit time constant is very high.
2. Every switching device, controlled and uncontrolled, is ideal.
3. The voltages of the capacitors are regarded as almost constant.
4. The passive components (R, L, and C) exhibit linear temporal invariance.
5. The inductor operates in the manner of continuous current.

This converter works in two operating modes.

Mode I ($0 < t < t_{on}, 0 < t < DT_t$)

Switch S_1 is ON, and DDC cell diode D_{d1} and D_{d2} are OFF. Its respective equations are as follows.

The voltage (V_L) across inductor L is given by

$$V_L = V_T \tag{5}$$

$$L\frac{dI_L}{dt_{ON}} = V_T \tag{6}$$

The voltage (V_{Ld}) across inductor L_d is given by

$$V_{Ld} = (V_0 - V_{Cd1} - V_{Cd2}) \tag{7}$$

$$L_d\frac{dI_L}{dt_{ON}} = (V_0 - V_{Cd1} - V_{Cd2}) \tag{8}$$

Mode II ($t_{on} < t < T_t, DT_t < t < T_t$).

Switch S_1 is OFF, and DDC cell diode D_{d1} and D_{d2} are ON. Its respective equations are as follows.

The voltage (V_L) across inductor L is given by

$$V_L = V_T + V_{Cd1} - V_0 \tag{9}$$

$$L\frac{dI_L}{dt_{OFF}} = V_T + V_{Cd1} - V_0 \tag{10}$$

$$V_L = V_T - V_{C1} \tag{11}$$

The voltage (V_{Ld}) across inductor L_d is given by

$$V_{Ld} = -V_{Cd1} \tag{12}$$

$$L_d\frac{dI_{Ld}}{dt_{OFF}} = -V_{Cd1} \tag{13}$$

For stable operation charging of inductor (L) = discharging of inductor (L)

$$L\frac{dI_L}{dt_{ON}} = -L\frac{dI_L}{dt_{OFF}} \tag{14}$$

$$(V_T)(DT_t) + (V_T + V_{Cd1} - V_0)(1-D)T_t = 0 \tag{15}$$

$$V_{Cd1} = V_0 - \left[V_t/(1-D)\right] \tag{16}$$

The voltage across capacitor C_{d1} is given by Eq. (16).

For stable operation charging of inductor (L_d) = discharging of inductor (L_d)

$$L\frac{dI_{Ld}}{dt_{ON}} = -L\frac{dI_{Ld}}{dt_{OFF}} \tag{17}$$

$$(V_0 - V_{Cd1} - V_{Cd2})(DT_t) + (-V_{Cd1})(1-D)T_t = 0 \tag{18}$$

Simplifying Eq. (17) yields the capacitor (V_{Cd1}, V_{Cd2}) voltage dependency on the duty ratio as the two intermediate capacitors in the mode-2 equivalent circuit are in parallel and charge to the same voltages, i.e, $V_{cd1} = V_{cd2}$.

$$V_{Cd1} = V_{Cd2} = \frac{(DV_0)}{(1+D)} \tag{19}$$

Simplifying Eqs. (19) & (16) gives following voltage gain

$$\frac{V_0}{V_T} = \frac{(1+D)}{(1-D)} \tag{20}$$

Now by Eqs. (19) & (20), V_{Cd1} and V_{Cd2} can be expressed in terms of input voltage

$$V_{Cd1} = V_{Cd2} = \frac{(DV_T)}{(1-D)} \tag{21}$$

The inductor L draws current from the input voltage (V_T) while operating in mode 1, and its ripple current is obtained as

$$\Delta I_L = \left(V_T D T_t / L\right) \tag{22}$$

Likewise, inductor L_d in mode-1 is impressed with $V_0 - V_{Cd1} - V_{Cd2}$ level, which is also equal to V_T, so current ripple in L_d can be obtained as

$$\Delta I_{Ld} = \left(V_T D T_t / L_d\right) \tag{23}$$

The input current (I_T), which is equal to inductor current (I_L), can be obtained, with the assumption of negligible losses ($V_T I_T = V_0 I_0$). The source current is obtained as

$$I_T = I_L = \left[(1+D)\, I_0 / (1-D)\right] \tag{24}$$

While the inductor L_D carries current identical to the capacitors for DT_t time and maintains its average current equal to load current as shown in Eq. (24), the capacitors (C_{d1} and C_{d2}) carry ripple current with zero average value.

$$I_0 = I_{Ld} = \left(V_0 / R\right) \tag{25}$$

The maximum (I_{Lmax}, I_{Ldmax}) and minimum (I_{Lmin}, I_{Ldmin}) currents through the inductors (L & L_d) are obtained by using Eqs. (22) & (23) as

$$I_{L\max} = I_L + \frac{\Delta I_L}{2} \tag{26}$$

$$I_{L\max} = I_L + \left(V_T D T_t / 2L\right) \tag{27}$$

$$I_{L\min} = I_L - \left(V_T D T_t / 2L\right) \tag{28}$$

Similarly,

$$I_{Ld\max} = I_L + \left(V_T D T_t / 2L_d\right) \tag{29}$$

$$I_{Ld\min} = I_L - \left(V_T D T_t / 2L_d\right) \tag{30}$$

The DDC converter's two modes may be seen to get the capacitor current expressions for each mode. These expressions are then used to obtain the ripple voltage expressions across capacitors C_{d1}, C_{d2}, and C_{dc}, which are provided by

$$\Delta V_{Cd1} = \left(I_0 D T_T / C_{d1}\right) = \Delta V_{Cd2} \tag{31}$$

$$\Delta V_{Cdc} = \left(2 I_0 D T_T / C_{dc}\right) \tag{32}$$

2.3. DDC Cell Converter Element and Choice of Parameters

MATLAB has been used to simulate the suggested model for 600 watts, and its respective experimental setup has been made. Switching frequency F_T is 50 KHz. The converter is designed to boost the voltage from 198.4 V to 300 V. Duty ratio can be calculated from Eq. (19), where $V_T = 198.4$ V and $V_0 = 300$ V. Duty ratio (D) = 0.203. The design equation listed in Table 1 with its ripple threshold [6] Δ_L, $\Delta_{Ld} < 30\%$ and $\Delta_{cd1} = \Delta_{cd2}$, $\Delta_{dc} < 5\%$) are used to calculate the value of energy storing elements (C_{d1}, C_{d2}, C_{dc}, L, and L_d) at ideal conditions $P_0 = 600$ w, $V_0 = 300$ V, $P_0 V_0 = I_0$, $I_0 = 2$ A, and $R_0 = 150\,\Omega$. from Eq. (25), $I_0 = I_{Ld} = 2$ A. From Eq. (24), source current I_T = inductor current I_L is computed as 3.03 A, by allowable ripple threshold $\Delta_L = 0.909$ A and $\Delta_{Ld} = 0.6$ A. The voltage across C_{d1} and C_{d2} can be calculated from Eq. (21) and $V_{cd1} = V_{cd2} = 50.623$ V and by allowable ripple threshold $\Delta_{cd1} = \Delta_{cd2} = 2.54$ V. The voltage across V_{dc} is equal to output voltage V_0, $V_{dc} = V_0 = 300$ V by ripple threshold $\Delta_{dc} = 15$ V. For soft switching to occur, the resonant frequency f_r must be greater than switching frequency $f_r = \frac{1}{2\pi\sqrt{LC_1}} \geq 50000, C_1 < 5.06$ nF.

TABLE 1. Parameter estimation.

Estimation of value of energy storing elements	
$L > (V_T \times D)/(\Delta I_L \times F_T)$	$C_{d1} > (I_0 \times D)/(\Delta V_{Cd1} \times F_T)$
$L_d > (V_T \times D)/(\Delta I_{Ld} \times F_T)$	$C_{d2} > (I_0 \times D)/(\Delta V_{Cd2} \times F_T)$
$\frac{1}{2\pi\sqrt{LC_1}} \geq 50000$	$C_{dc} > (2I_0 \times D)/(\Delta V_{dc} \times F_T)$

From the design equation listed in Table 1, $L > (V_T D)/\Delta_L F_t)$, $L > (198.4 * 0.203)/(0.456 * 50000) = 1004\,\mu$H. $L_d > (V_T D)/\Delta_{Ld} F_t)$, $L_d > (198.4 * 0.203)/(0.6 * 50000) = 1342.5\,\mu$H, $C_{d1} = C_{d2} > (I_0 D)/\Delta_{cd1} F_t)$. $C_{d1} = C_{d2} > (2 * 0.203)/(2.54 * 50000) = 3.19\,\mu$F. $Cdc > (2_0 D)/\Delta_{dc} F_t)$, $Cdc > (2 * 2 * 0.203)/(15 * 50000) = 1.08\,\mu$F. The values of energy storing elements used in are specified in Table 2 as follows $L = 2$ mH, $L_d = 1.35$ mH, $C_{d1} = C_{d2} = 4\,\mu$F, $C_{dc} = 3\,\mu$F, and $C_1 = 3$ nF.

TABLE 2. Parameter values.

Estimation of value of energy storing elements	
$L = 2$ mH	$C_{d1} = 4\,\mu$F
$L_d = 1.35$ mH	$C_{d2} = 4\,\mu$F
$C_1 = 3$ nF	$C_{dc} = 3\,\mu$F

2.4. Voltage Stress Across Switches

The voltage stress across switch S_1 is calculated from Fig. 3(b), and the voltage stress across the diode D_{d1} and D_{d2} are calculated from Fig. 3(a).

The voltage stress across switch S_1 is V_0-V_{cd1}, and the voltage stress across the diodes D_{d1} and D_{d2} are V_{Cd1}-V_{Ld}.

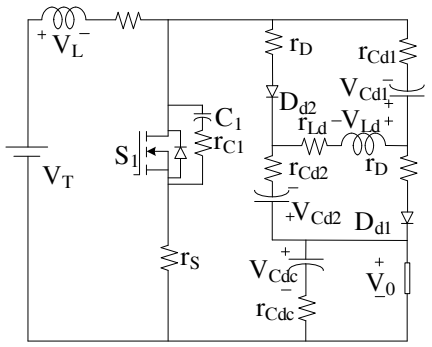

FIGURE 5. Modified DDC converter with its respective parasitic elements.

2.5. Small Signal Model Analysis and Closed Loop Operation

The equivalent circuit with its respective parasitic resistances is shown in Fig. 5. Using basic circuit rules, the equivalent circuit shown in Fig. 5 is converted into a set of first-order differential equations to explain the dynamic behavior of the converter. These differential equations are now expressed in the standard state space model as follows, in order to expand the linear system theory.

$$x = \begin{bmatrix} i_L & i_{Ld} & V_{C1} & V_{Cd1} & V_{Cd2} & V_{Cdc} \end{bmatrix}^T \quad (33)$$

$$u = V_T \quad (34)$$

$$y = V_0 = V_{Cdc}$$

Mode I ($0 < t < t_{on}, 0 < t < DT_t$)

Switch S_1 is ON, and DDC cell diode D_{d1} and D_{d2} are OFF. Its respective equations are as follows

$$V_L = L\frac{di_L}{dt} = V_T - r_L i_L - (r_S + r_{C1})\, i_L \quad (35)$$

$$V_{Ld} = L\frac{di_{Ld}}{dt} = V_0 - V_{Cd1} - V_{Cd2} - (r_{Cd1} + r_{Cd2} + r_{Ld})\, i_{Ld} \quad (36)$$

$$i_{C1} = C_1\frac{dV_{C1}}{dt} = i_L - \frac{V_{C1}}{r_{C1}} \quad (37)$$

$$i_{Cd1} = C_{d1}\frac{dV_{Cd1}}{dt} = -i_{Ld} \quad (38)$$

$$i_{Cd2} = C_{d2}\frac{dV_{Cd2}}{dt} = \frac{V_{Cd2} - V_0}{r_{Cd2}} \quad (39)$$

Mode II ($t_{on} < t < T_t, (1-D)Tt < t < T_t$)

Switch S_1 is OFF, and DDC cell diode D_{d1} and D_{d2} are ON. Its respective equations are as follows

$$V_L = L\frac{dI_L}{dt_{OFF}} = V_T + V_{Cd1} - V_0 - 2r_D i_L - r_L i_L \quad (40)$$

$$V_{Ld} = L_d\frac{dI_{Ld}}{dt_{OFF}} = -V_{Cd1} - (r_{Cd1} + r_{Ld})\, i_{Ld} \quad (41)$$

$$i_{C1} = C_1\frac{dV_{C1}}{dt} = -i_L - \frac{V_{C1}}{r_{C1}} \quad (42)$$

$$i_{Cd1} = C_1\frac{dV_{C1}}{dt} = i_L - i_{Ld} \quad (43)$$

$$i_{Cd2} = C_1\frac{dV_{C2}}{dt} = i_L - \frac{V_{Cd2} - V_0}{r_{Cd2}} \quad (44)$$

Average state space model using duty ratio d

$$\dot{x} = d\,(A_1 x + B_1 u) + (1-d)(A_2 x + B_2 u) \quad (45)$$

$$\dot{x} = Ax + Bu \quad (46)$$

where,

$$A = dA_1 + (1-d)A_2 \quad (47)$$

$$B = dB_1 + (1-d)B_2 \quad (48)$$

$$A = \begin{bmatrix} \frac{-r_{C1}}{L} & 0 & \frac{-1}{L} & -\frac{1-d}{L} & -\frac{1-d}{L} & 0 \\ 0 & \frac{-r_{Ld}}{L_d} & 0 & \frac{1-d}{L_d} & \frac{-d}{L_d} & -\frac{1-d}{L_d} \\ \frac{2d-1}{C_1} & 0 & \frac{-1}{r_{C1}C_1} & 0 & 0 & 0 \\ \frac{1-d}{C_{d1}} & -\frac{1-d}{C_{d1}} & 0 & 0 & 0 & 0 \\ \frac{1-d}{C_{d2}} & \frac{-d}{C_{d2}} & 0 & 0 & -\frac{1}{r_{Cd1}C_{d2}} & \frac{1}{r_{Cd1}C_{d2}} \\ 0 & \frac{1-d}{C_{dc}} & 0 & 0 & \frac{1}{r_{Cd2}C_{dc}} & -\left(\frac{1}{r_{Cd2}C_{dc}} + \frac{1}{r_0 C_{dc}}\right) \end{bmatrix} \quad (49)$$

$$B = \begin{bmatrix} \frac{1}{L} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad (50)$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (51)$$

The transfer function can be obtained as

$$G_{DDC}(S) = B\,[SI - A]^{-1}\, C \quad (52)$$

$$G_{DDC}(S) = \frac{\left[\alpha_2 s^2 + \alpha_1 s^1 + \alpha_0 s^0\right]}{\left[s^6 + \beta_5 s^5 + \beta_4 s^4 + \beta_3 s^3 + \beta_2 s^2 + \beta_1 s^1 + \beta_0 s^0\right]} \quad (53)$$

where,

$$\alpha_2 = 2.87\,(10)^{13},\ \alpha_1 = 4.11\,(10)^{17},\ \alpha_0 = 1.74\,(10)^{21}$$

$$\beta_5 = 1.92\,(10)^{4},\ \beta_4 = 3.78\,(10)^{8},\ \beta_3 = 4.62\,(10)^{12}$$

$$\beta_2 = 3.55\,(10)^{16},\ \beta_1 = 1.48\,(10)^{20},\ \beta_0 = 2.93\,(10)^{23}$$

The open-loop pole-zero (P-Z) map of the DDC cell-driven converter is shown in Fig. 6. The fact that all 6 poles of the DDC cell-driven converter (shown by crosses) are on the left

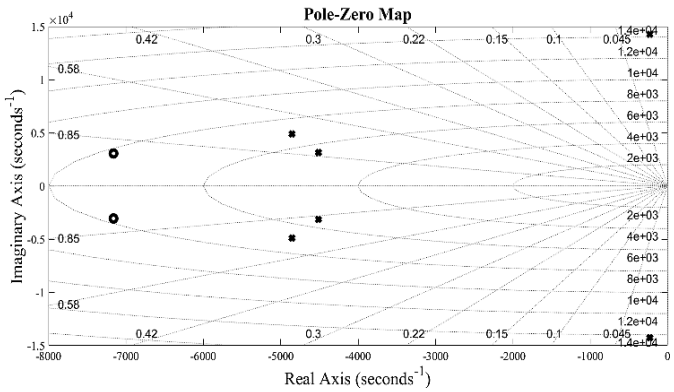

FIGURE 6. Pole zero plot for DDC cell boost converter.

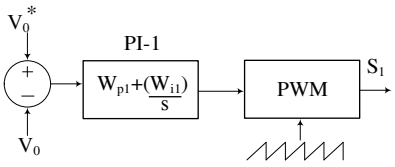

FIGURE 7. Control circuit for 6th order soft switched DDC cell boost converter.

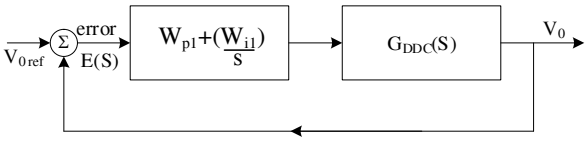

FIGURE 8. Pole zero plot for DDC cell boost converter.

side of the y axis validates the Routh-Hurwitz stability criterion. Using the PI controller seen in Fig. 7, the tuned PI controllers are used in a cascaded voltage control loop. The DDC cell converter transfer function is provided by Eq. (53), which represents an open-loop stable system.

The open-loop transfer function of the complete system employing control is shown in Fig. 8, and the open-loop transfer function of the complete system is calculated as

$$TF_{DDC}(S) = \left(W_{P1} + \frac{W_{i1}}{s}\right) \times G_{DDC}(S) \tag{54}$$

$$TF_{DDC}(S) = \frac{\left[\chi_3 s^3 + \chi_2 s^2 + \chi_1 s^1 + \chi_0 s^0\right]}{\left[s^7 + \delta_6 s^6 + \delta_5 s^5 + \delta_4 s^4 + \delta_3 s^3 + \delta_2 s^2 + \delta_1 s^1\right]} \tag{55}$$

where $\chi_3 = 7.365\,(10)^{11}$, $\chi_2 = 1.622\,(10)^{16}$, $\chi_1 = 4.41\,(10)^{20}$, $\chi_0 = 3.798\,(10)^{23}$, $\delta_6 = 7.64\,(10)^{4}$, $\delta_5 = 1.92\,(10)^{9}$, $\delta_4 = 2.73\,(10)^{13}$, $\delta_3 = 2.187\,(10)^{17}$, $\delta_2 = 9.602\,(10)^{20}$, $\delta_1 = 2.291\,(10)^{24}$.

The bode-plot corresponding to the DDC cell converter is shown in Fig. 9. The stability of the DDC cell converter and control system is demonstrated by the gain and phase margins obtained from the Bode diagram, and the closed-loop system achieves a gain margin of 78.9 dB and is a closed loop as well as an open-loop stable system.

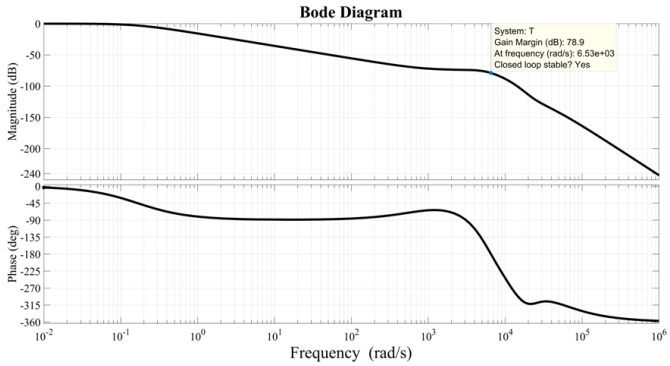

FIGURE 9. Bode plot of closed loop soft switched DDC cell boost converter.

2.6. Efficiency Analysis

This section discusses the detailed efficiency analysis of a modified DDC cell converter with parasitic resistance, thus formulating the actual voltage gain and power loss across different components.

Applying volt-Sec balance on Inductor L

$$(V_L)(DT_t) + (V_L)(1-D)T_t = 0 \tag{56}$$

From Eqs. (35) & (40)

$$\begin{aligned}&(V_T - r_L i_L - (r_S + r_{C1})\, i_L)\,(d)\\ &+ (V_T - r_L i_L - (r_S + r_{C1})\, i_L)\,(1-d) = 0\end{aligned} \tag{57}$$

$$V_{Cd1} = \frac{(1-d)\, V_0 i_L R_1 - V_T}{1-d} \tag{58}$$

where,

$$R_1 = d\,(r_L + r_S + r_{C1}) + (1-d)\,(2r_D + r_L) \tag{59}$$

Applying volt-Sec balance on inductor L_d,

$$(V_L)(DT_t) + (V_L)(1-D)T_t = 0 \tag{60}$$

From Eqs. (36) & (41)

$$\begin{aligned}&(V_0 - V_{Cd1} - V_{Cd2} - (r_{Cd1} + r_{Cd2} + r_{Ld})\, i_{Ld})\,(DT_t)\\ &+ (-V_{Cd1} - (r_{Cd1} + r_{Ld})\, i_{Ld})\,(1-D)\,T_t = 0\end{aligned} \tag{61}$$

$$V_{Cd1} = \frac{dV_0 + i_{Ld} R_2}{1+d} \tag{62}$$

where,

$$R_2 = d\,(r_{Cd1} + r_{Cd2} + r_{Ld}) + (1-d)\,(2r_{Cd1} + r_{Ld}) \tag{63}$$

The actual gain of the converter is calculated from Eqs. (58) & (62)

$$G = \left(\frac{1+d}{1-d}\right) - \left(\frac{(1+d)\, i_L R_1 + (1-d)\, i_{Ld} R_2}{(1-d)\, V_T}\right) \tag{64}$$

Figure 10 shows the variation of voltage gain with duty ratio under different load conditions.

To further assess practical performance, a power-loss study of the 600 W prototype is conducted. The modified DDC cell converters' power loss and its estimation are shown in Table 3.

TABLE 3. Total power loss and estimation.

Classification	Estimation	Value (W)	Percentage
MOSFET Conduction loss	$\sum I_{s,rms}^2 r_S$	3.6	19.40
Switching loss	$P_{sw,S1} + P_{Sw,D}$	1.08	5.83
Diode Conduction Loss	$\sum I_{D,rms}^2 r_D$	8	43.12
Inductor loss	$\sum I_{L,rms}^2 r_L$	1.9	10.24
Capacitor loss	$\sum I_{C,rms}^2 r_c$	2.1	11.32
Core losses + gate driver		0.5	2.69
miscellaneous		1.37	7.385

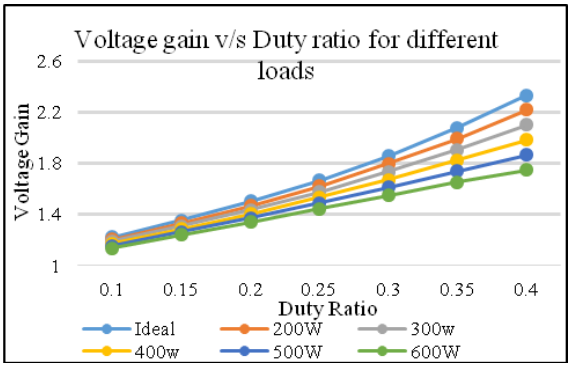

FIGURE 10. Voltage gain versus duty ratio for different load conditions.

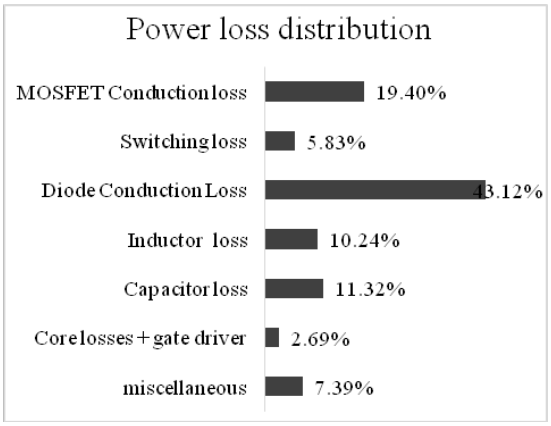

FIGURE 11. Power loss distribution for the presented converter.

At full load, the observed peak load efficiency of 97% is equal to a total power loss of

$$P_{loss} = \frac{P_{output}}{\eta} - Poutput = 18.55\,\text{W} \tag{65}$$

where P_{loss} is the summation of all losses from the parasitic component of the modified DDC cell converter.

Switching losses are estimated as there is a small overlap between voltage and current waveforms in the experimental setup, and conduction losses account for most of the total power dissipation.

MOSFET switching loss is calculated as

$$P_{Sw,S1} = \left(1/2\right)\left(V_{S1} I_{S1}\right)\left(t_r + t_f\right) f_t \tag{66}$$

where t_r is the rise time, and t_f is the fall time of voltage and current across switch

$$P_{Sw,S1} = \left(1/2\right)\left(52 \times 3.02\right)\left(80 \times 10^{-9}\right) 50000 = 0.36\,\text{W} \tag{67}$$

Diode switching loss is calculated as

$$P_{Sw,Dd1} = P_{Sw,Dd2} = Q_{rr} V_{Dd1} f_t \tag{68}$$

where Q_{rr} is the reverse recovery charge of diode

$$P_{Sw,Dd1} = P_{Sw,Dd2} = \left(70 \times 10^{-9}\right) 102 \times 50000 \tag{69}$$

$$P_{Sw,Dd1} = P_{Sw,Dd2} = 0.36 \tag{70}$$

Total switching loss across the diode is

$$P_{Sw,D} = 0.72w \tag{71}$$

Figure 11 illustrates that diode conduction loss, which accounts for approximately 45% of the total losses, is the primary source of power loss in the converter. Duty ratio for switch is minimum, which increases the conduction time of diode, and is the primary cause of loss. The conduction losses of the MOSFET are around 20%, since the converter's operational duty ratio is minimal. The losses across the capacitor and inductor are around 10% and 11%, respectively.

$$\eta = \frac{V_0}{V_T\left(\frac{1+d}{1-d} + P_{loss}\right)} \tag{72}$$

Figure 12 shows the efficiency of the DDC cell converter with varying load. Experimental efficiency at 600 W is 97% while theoretical efficiency is 98.1%.

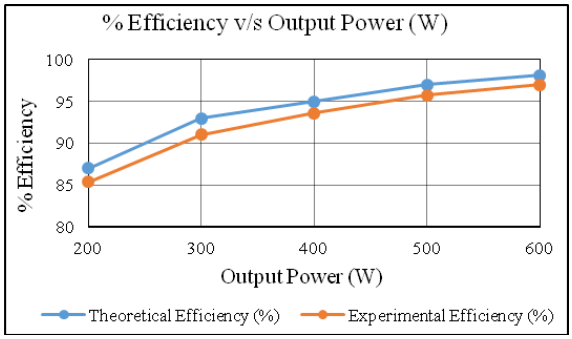

FIGURE 12. %efficiency v/s output power.

TABLE 4. Comparative evaluation of semiconductor stress, efficiency, and auxiliary components.

S. No.	Reference	Voltage stress		Efficiency	Power rating	Auxiliary circuit Component count				
		Switch	Diode			Q	L	C	d	T
1.	[5]	$\frac{V_0}{2}\big\|_{s_1,s_2}$	$V_0\|_{d_1}$, $V_0\|_{d_2}$, $V_{D0}\|_{d_3}$	96%	200 W	0	2	2	3	7
2.	[11]	$V_0\|_{s_1,s_2}$	$V_0 - V_T\|_{d_1,d_2}$	96%	3 KW	2	2	0	3	7
3.	[12]	$\frac{3V_T}{2}\Big\|_{s_1,s_2}$	$V_T\|_d$	97.5%	150 W	2	3	1	1	7
4.	[13]	$V_0\|_s$	$V_0\|_d$	94.7%	300 W	2	2	0	3	7
5.	[14]	$\frac{V_0 n_2}{n_1} - V_T\Big\|_{s_1,s_2}$	$V_0\|_{d_{01},d_{02}}$	96%	18 KW	2	1	2	2	7
6.	[15]	$V_0 - \frac{V_T}{2}\Big\|_{s_1}$	$V_0\|_d$	97%	1 KW	1	2	3	2	8
8.	[16]	$V_0 - V_T\|_{s_1}$	$V_0\|_d$	98%	300 W	1	2	3	2	8
9.	[17]	$\frac{(1+n_2)V_0}{1+2n_3-D(n_2+n_3-1)}\Big\|$	$\frac{(1+n_3)V_0}{1+2n_3-D(n_2+n_3-1)}\Big\|$	95.24	200 W	0	3	4	3	10
10.	[18]	$\frac{V_0}{2}\big\|_{s_1,s_2}$	$\frac{V_0}{2}\big\|_{d_1,d_2}$	97.3%	150 W	0	5	1	4	10
11.	[19]	$\frac{V_T}{1-D}\Big\|_{s_1}$, $\frac{(1+n)V_T-V_{LK}}{1-D}\Big\|_{s_2}$	$\frac{V_T}{1-D}\Big\|_{d_1}$, $\frac{(1+n)V_T-V_{LK}}{1-D}\Big\|_{d_2}$	96.7%	100 W	1	2	3	2	8
12.	[20]	$\frac{V_T}{1-D}\Big\|_{s_1}$	$\frac{V_T}{1-D}\Big\|_{d_1,d_2,d_3}$, $\frac{nV_T}{1-D}\Big\|_{d_4,d_5,d_6}$	95%	300 W	0	1	1	2	4
13.	DDC	$V_0 - V_{Cd1}\|_{s_1}$	$V_{Cd1} - V_{Ld}\|_{d_{d1},d_{d2}}$	97%	600 W	0	0	1	0	1

*d = Diode, D = duty ratio, Q = controlled Switch, L = inductor, C = capacitor, T = total auxiliary component.

2.7. DDC Cell Driven Soft Switched Converter Differential Factors

Table 4 presents a comprehensive comparison between the proposed DDC-cell converter and several recently reported high-gain DC-DC converter topologies. From the comparison, it can be observed that the proposed converter achieves a high conversion efficiency of 97% while operating at a power rating of 600 W. One of the most notable advantages of the proposed topology is its significantly reduced auxiliary component requirement. Unlike many existing converters that rely on multiple auxiliary inductors, capacitors, switches, and diodes to realize soft-switching operation, the proposed converter utilizes only a single auxiliary capacitor. As a result, the overall converter structure becomes much simpler and easier to implement. The reduced component count also minimizes gate driving complexity, control circuitry requirements, converter volume, and overall system cost.

Another important advantage of the presented converter is the reduced voltage stress across the semiconductor devices. The voltage stress across the main switch is limited to V_0-V_{cd1}, whereas the voltage stress across the diodes is restricted to V_{Cd1}-V_{Ld}. Due to this reduced stress profile, lower voltage-rated semiconductor devices can be employed, which directly contributes to lower conduction losses, reduced switching losses, and improved overall efficiency. In comparison, several converters reported in [11, 14, 17, 19] experience relatively higher switch or diode voltage stress and often require additional passive or active clamping networks to protect the devices. Furthermore, some topologies achieve soft switching at the expense of increased circuit complexity and higher auxiliary component count, which may reduce reliability and increase implementation difficulty.

Although certain converters, such as the topology presented in [16], demonstrate slightly higher peak efficiency, they operate at substantially lower power levels and require a greater number of auxiliary components. Similarly, other converters achieve acceptable efficiency but suffer from either high component count, increased device stress, or limited power capability. In contrast, the proposed DDC-cell converter offers a well-balanced trade-off among efficiency, voltage stress reduction, circuit simplicity, and power handling capability. The combination of high efficiency, reduced semiconductor stress, minimal auxiliary circuitry, and medium-to-high power operation makes the proposed converter highly suitable for practical renewable energy systems, battery charging applications, electric vehicle power interfaces, and other high-gain DC-DC conversion applications requiring efficient and reliable operation.

3. VALIDATIONS AND RESULTS

This section evaluates the effectiveness of the modified DDC cell converter using MATLAB/Simulink results and experimental setup results.

Steady state simulation results are shown in Fig. 13 and Fig. 14. Switch's current and voltage are shown in Figs. 13(a) and (b), respectively. ZCS for the switch S_1 is achieved as the current across the switch is made zero and after that the voltage across the switch starts to rise. ZVS is also achieved by the switch as the voltage across the switch is zero before the current across it starts to increase. The theoretical voltage stress and current stress on switch S_1 are 52 V and 3.25 A, Similarly, Figs. 13(c) and (d) show the current and voltage across the Diode D_{d1}, respectively; D_{d1} also achieves ZVS and ZCS; and its theoretical voltage stress is 102 V.

Figures 14(a) and (b) show the current and voltage across the diode D_{d2} respectively; D_{d2} also achieves ZVS and ZCS; and its theoretical voltage stress is 102 V. Figs. 14 (c) and (d) show the output voltage and current, respectively, a ndV_0 is held constant at 300 V, delivering 2 A current to 150 Ω resistive load.

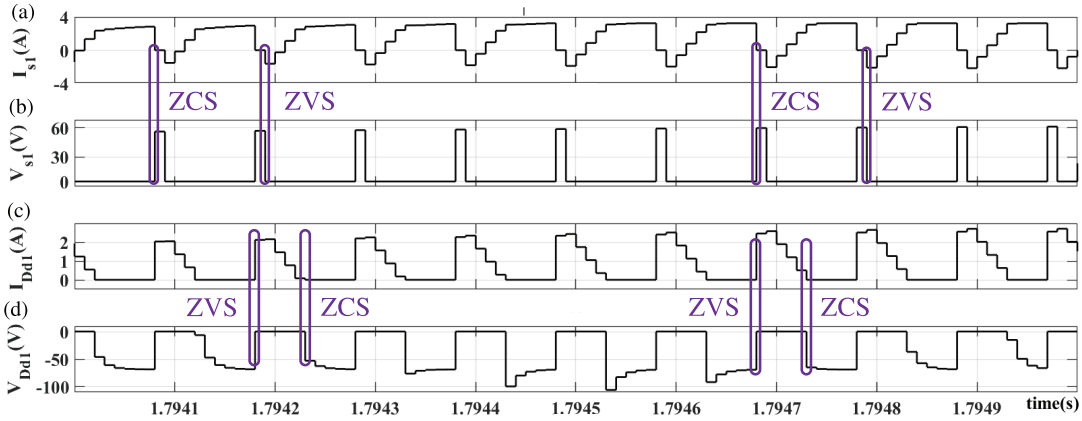

FIGURE 13. (a) Current through S_1 (I_{S1}), (b) voltage across S_1 (V_{S1}), (c) current through D_{d1} (I_{Dd1}), and (d) voltage across D_{d2} (V_{Dd2}).

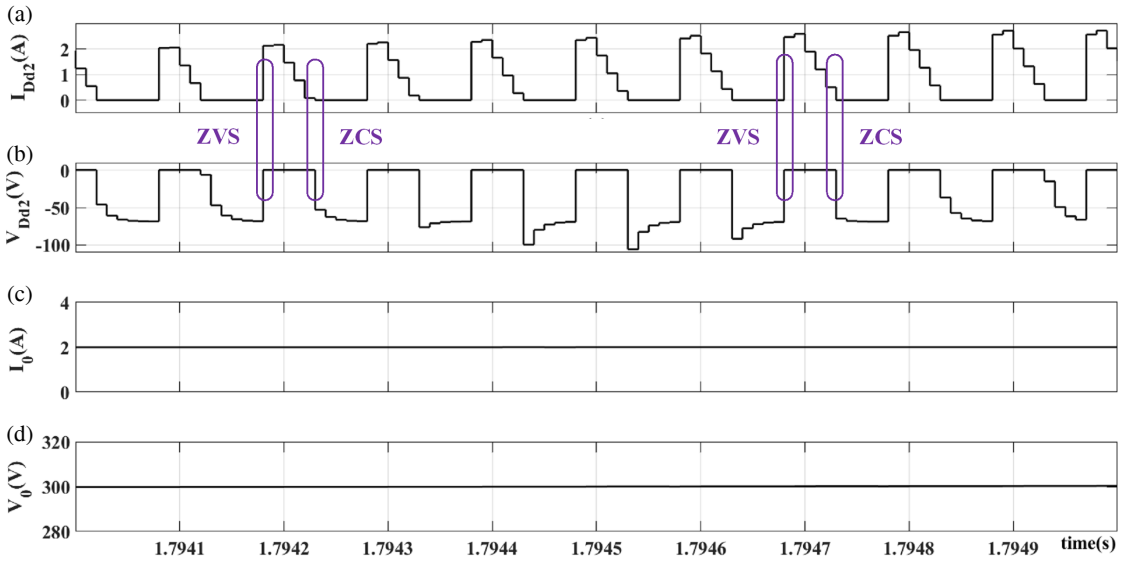

FIGURE 14. (a) Current through $Dd2$ (I_{Dd2}), (b) voltage across $Dd2$ (V_{Dd2}), (c) output voltage (V_0), and (d) output current (I_0).

Figure 20 shows the hardware implementation of the DDC cell converter. The DBR is used to convert AC voltage into DC voltage, which is then supplied to the MOSFET module. A 50 kHz switching signal is generated using dSPACE DS1104 to drive switch S_1.

Experimental steady state results are shown in Fig. 15 and Fig. 16. I_{S1}, V_{S1}, I_{Dd1}, and V_{Dd1} results are shown in Fig. 15, respectively, and their soft switching operation is also shown.

During Mode-I, before the main switch S_1 is turned ON, the auxiliary capacitor C_1 discharges through the body diode of the MOSFET. This discharge path reduces the voltage across the main switch nearly to zero before the gate pulse is applied. Consequently, the switch turns ON under near-zero-voltage conditions, thereby significantly reducing turn-on switching losses.

During Mode-II, when the main switch is turned OFF, the auxiliary capacitor C_1 begins charging and gradually diverts the current away from the switch. As a result, the current through the switch decreases close to zero before complete turn-off occurs, thereby minimizing the overlap between voltage and current during switching transition. This controlled charging and discharging action of C_1 reduces switching losses, suppresses current spikes, and alleviates reverse recovery stress in the auxiliary diodes, leading to improved efficiency and smoother switching transitions.

I_{Dd2}, V_{Dd2}, and V_o results are shown in Fig. 16, while soft switching operation of diode D_{d2} is also shown. The voltage stress (experimental setup) across the switch and diode are 64 V and 102 V, respectively. The output voltage is held constant at 300 V, validating the theoretical expectation. Due to negligible overlap of voltage and current waveforms, switching losses across the diode and switch are evaluated in Table 3.

The modified DDC cell converter also improves the power quality on the input side, and its respective power quality analyzer result is shown in Fig. 17. The input stage of the DDC cell converter is derived from the SEPIC converter topology. The input inductor L helps improve the input current profile and power quality, thereby reducing THD.

By Power Quality Analyzer, the total harmonic distortion is 3.00%, which satisfies the IEEE-519 standard. The input side voltage profile and current profile are shown in Fig. 18. The

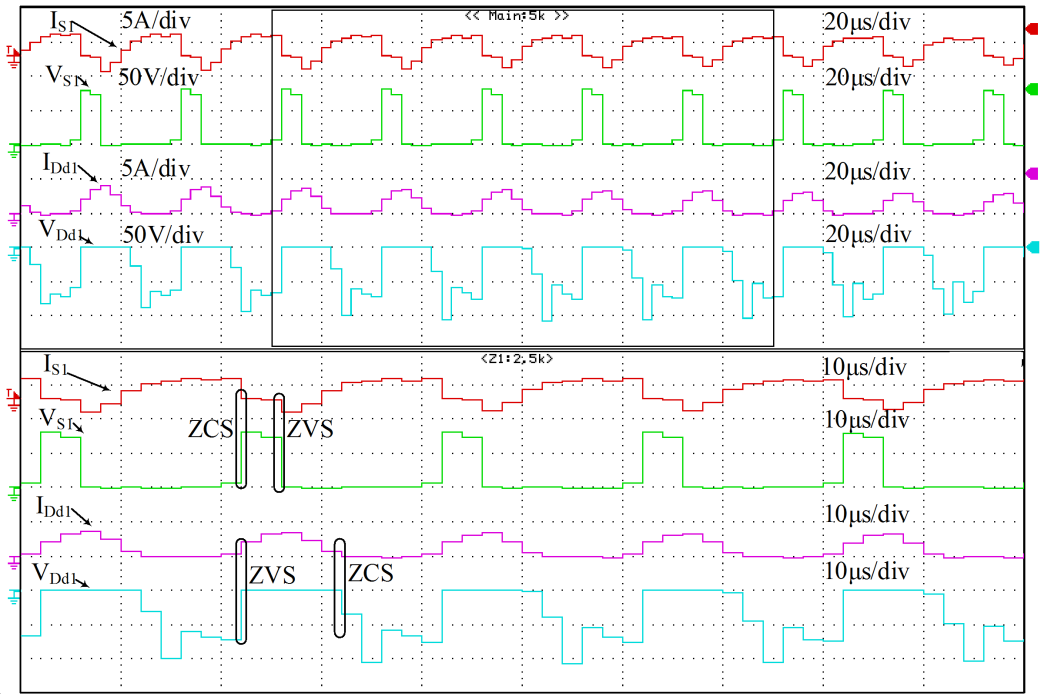

FIGURE 15. Experimental setup results I_{S1}, V_{S1}, I_{Dd1}, V_{Dd1}.

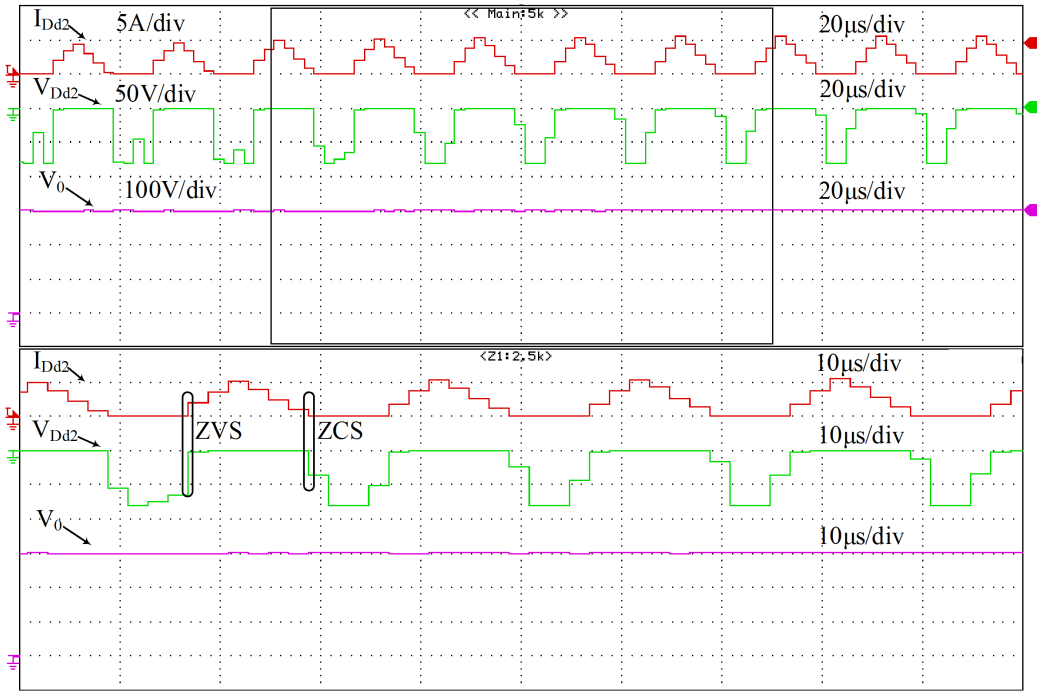

FIGURE 16. Experimental setup results I_{Dd2}, V_{Dd2}, and V_0.

input current (I_{in}) is shown in Fig. 18(b), which is sinusoidal as (V_{in}) shown in Fig. 18(a).

Experimental waveforms indicate that the input current remains nearly sinusoidal with THD limited to approximately 3%. However, a phase displacement between input voltage and current is observed due to the reactive behavior of the input filtering and converter dynamics, resulting in an input power factor of approximately 0.8.

To further assess the performance of the presented converter, dynamic results with variation of load voltage are shown in Fig. 19, in which the converter is subjected to the variation of load current. Load current is changed from 2 A to 1 A, and V_0 reaches a peak voltage of 306 V and settles down to 300 V in 200 ms. Further load current is changed from 1 A to 2 A, and V_0 reaches a reduction to 295 V and settles down to 300 V in 180 ms. V_0 settles down to 300 V in both cases.

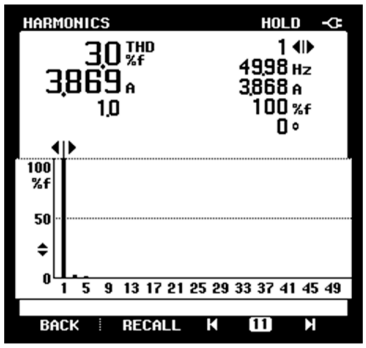

FIGURE 17. FFT analysis of power quality improved soft-switched DDC cell converter.

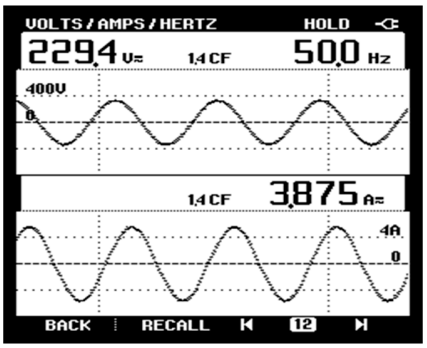

FIGURE 18. (a) Input Voltage V_{in} and (b) input current I_{in}.

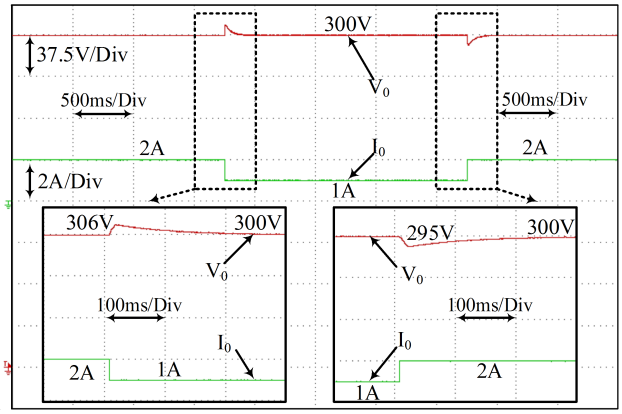

FIGURE 19. Dynamic result for the variation of load current.

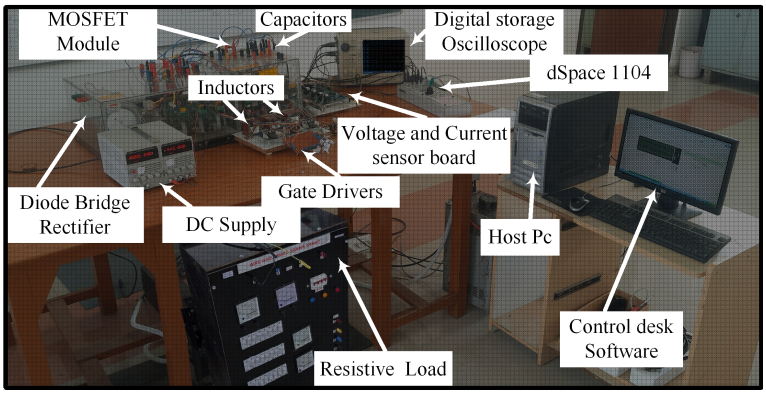

FIGURE 20. Experimental setup for DDC cell converter.

TABLE 5. Steady state performance at different loads.

Load Power (W)	Output Voltage (V)	Output Current (A)	Efficiency (%)	Input Current THD (%)	Power Factor
200	300	0.67	85.4	3.8	0.74
300	300	1	91	3.5	0.76
400	300	1.33	93.6	3.2	0.78
500	300	1.67	95.7	3.1	0.79
600	300	2	97	3	0.8

Steady state performance for different loads is shown in Table 5.

4. CONCLUSION

This article presents a modified DDC converter for high-gain DC-DC conversion applications. The proposed converter achieves a high voltage gain of $(1 + D)/(1 - D)$ while maintaining a common-ground configuration, reduced pulsating source current, and non-inverted output voltage. A single auxiliary capacitor is employed to facilitate soft-switching operation with reduced switching stress and minimized switching losses without significantly increasing converter complexity.

Detailed steady-state analysis, small-signal modelling, and dynamic analysis under load variation are carried out to validate the converter performance. Experimental verification using a 600 W prototype demonstrates a peak efficiency of 97% with reduced semiconductor voltage stress. Experimental waveforms confirm soft-switching operation with only a small overlap between switch voltage and current during switching transitions, resulting in reduced switching losses and smoother commutation characteristics. In addition, the converter achieves improved input-side power quality with input current THD limited to 3%, satisfying the IEEE-519 harmonic standard requirements. The experimentally observed input power factor is nearly 0.8 under rated operating conditions due to the phase displacement between the source voltage and current.

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