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Variable-Weighted Virtual Impedance Control for Current Balancing in qZSI-VSG Systems under Asymmetric Fault Conditions

Yang Zhang[1], Dingai Zhong[1], Xiuhai Yang[1], Wei Zhang[1], Ziquan Wei[1], and Zhun Cheng[2,*]

[1]*Hunan University of Technology, Zhuzhou 412007, China*
[2]*Hunan Railway Professional Technology College, Zhuzhou 412001, China*

ABSTRACT: To address output current over-limit issues, power oscillations, and degraded transient stability in virtual synchronous generators (VSGs) under asymmetric faults, this study proposes a variable-weight virtual-impedance-based current balancing control strategy for quasi-Z-source inverter-based VSG (qZSI-VSG) systems. First, a detailed mathematical model of the qZSI-VSG was established to analyze the influence of key parameters on the system's dynamic behavior. By leveraging the VSG operating characteristics in the *dq* reference frame, a negative-sequence current reference generation method was subsequently developed to effectively suppress the negative-sequence components under various unbalanced grid conditions. In addition, a proportional integral (PI) controller is introduced to regulate active and reactive power deviations, enabling the online calculation of adaptive weighting factors for the real-time adjustment of the virtual impedance. This mechanism improves both the current balancing performance and transient response. The experimental results verified that the proposed strategy can significantly reduce negative-sequence currents and power oscillations, thereby enhancing the transient stability of the system during asymmetric faults and demonstrating its feasibility and effectiveness.

1. INTRODUCTION

Advancing the energy transition and achieving the strategic objectives of carbon peaking and carbon neutrality depend heavily on the large-scale grid integration of renewable energy sources, such as wind and solar power [1]. However, the inherent intermittency and randomness of renewable energy sources introduce substantial challenges to the stable operation and control of modern power systems [2]. Against this backdrop, Virtual Synchronous Generator (VSG) technology has emerged as a prominent research focus [3, 4]. By emulating the rotor dynamics and primary frequency regulation characteristics of synchronous machines, VSGs provide essential synthetic inertia and damping support, thereby improving the grid's capability to accommodate high penetrations of renewable generation. In [5], the operating principles of VSGs were systematically reviewed from the electromechanical-analogy and energy-reconfiguration perspectives, and existing control strategies were categorised into parameter adaptation, feedback control, feedforward compensation, and hybrid compensation. Comparative analyses confirmed that these approaches can effectively suppress power oscillations and mitigate parameter coupling through coordinated energy regulation.

To further enhance efficiency and reliability, the quasi-Z-source inverter (qZSI) has been widely recognized as an attractive topology for renewable grid-connected applications owing to its single-stage voltage-boost capability and high operational robustness [6]. In recent years, the integration of qZSI with VSG technology has become an active area of research. In [7], batteries were embedded into a qZSI impedance network to achieve flexible power regulation through VSG control. In [8–10], several optimization methods that improve dynamic response and maximum-power-point-tracking (MPPT) performance from different perspectives were proposed. In [11], a distributed adaptive control method based on multi-agent deep reinforcement learning (MADRL) was developed to enhance coordinated frequency regulation among multiple VSGs. However, most existing studies focus mainly on normal or symmetrical operating conditions, while their adaptability and robustness under frequent asymmetrical faults observed in real grids remain limited.

During asymmetric grid faults (e.g., voltage dips), the VSG output current typically becomes severely unbalanced. This not only poses an overcurrent risk to power devices but also introduces second-order harmonic oscillations in active and reactive power, thereby threatening the system's transient stability [12]. Therefore, ensuring adequate fault ride-through (FRT) capability is critical for the reliable operation of grid-connected converters. To address this issue, various improved control strategies have been proposed. In [13], a balanced current control method is introduced to suppress three-phase current imbalance. In [14–16], power angle compensation, voltage calculation for steady-state fault power flows, and passivity-based control (PBC) are respectively proposed to enhance the power angle stability and overcurrent behavior of VSGs from different perspectives. In [17], an optimized control strategy is developed, which maintains the voltage-source characteristics of

* Corresponding author: Zhun Cheng (120277982@qq.com).

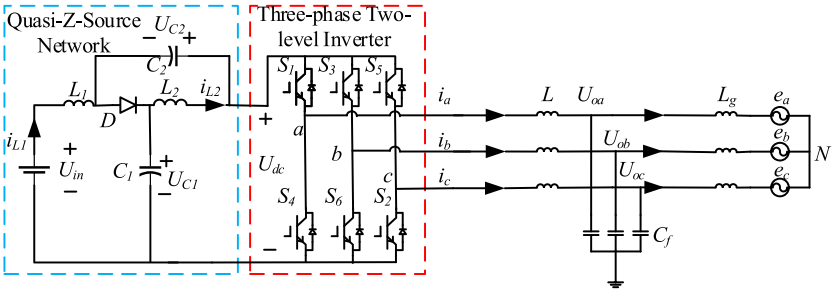

FIGURE 1. qZSI topology circuit diagram.

VSGs during faults and derives an analytical expression for the VSG short-circuit current under asymmetric conditions.

Among the numerous Low Voltage Ride Through (LVRT) solutions, virtual impedance control is widely regarded as a key technology. However, existing methods exhibit clear limitations when applied to asymmetric faults in VSG systems. The fixed virtual impedance in [18] is only valid under symmetrical faults. Time-varying virtual impedances in [19, 20] follow predetermined schedules without real-time adaptability to fault evolution. The adaptive strategies in [21, 22] adjust impedance based on current magnitude or voltage deviation, but they neither consider the distinct roles of active and reactive power deviations nor enable independent tuning of d- and q-axis impedances. In [23], virtual impedance combined with grid-voltage feedforward compensation improves voltage sag response, yet the coordination between current limitation and power support remains open-loop. The improved scheme in [24] suppresses fault current components but does not adaptively weigh the transient trade-off between power quality and device safety.

To overcome these gaps, this paper proposes a variable-weight virtual-impedance-based balanced-current control strategy for qZSI-VSG systems. The key novelties that distinguish this work from [18–24] are: (i) a power-deviation-driven weighting mechanism that replaces open-loop or single-feedback adjustment with closed-loop real-time adaptation; (ii) independent d- and q-axis virtual impedance regulation enabled by separate weighting coefficients for active and reactive power; and (iii) a dynamic balance between current limiting and power support during fault transients, which is absent in prior adaptive virtual impedance designs.

Motivated by these challenges, this study proposes a variable-weight virtual-impedance-based balanced-current control strategy for quasi-Z-source inverter-based VSG (qZSI-VSG) systems. The main contributions of this study are summarized as follows:

1) A power-command-based negative-sequence current calculation method is formulated, enabling the effective suppression of negative-sequence currents under unbalanced grid conditions.

2) A novel variable weight virtual impedance mechanism driven by active/reactive power deviations is introduced, enabling the adaptive and coordinated adjustment of the d- and q-axis impedances. This provides a dynamic balance between the current-limiting and power-support capabilities during fault conditions.

3) Comparative experimental results demonstrate that the proposed strategy significantly suppresses inrush currents, reduces power oscillations, and enhances transient stability compared to conventional VSG and balanced-current-control methods.

The remainder of this paper is organized as follows. Section 2 describes the operating principles of the qZSI-VSG system. Section 3 details the proposed control strategy. Section 4 validates its effectiveness through RT-LAB experiments, and Section 5 concludes the paper.

2. PRINCIPLES OF THE QZSI-VSG SYSTEM

This section presents the fundamental configuration and operating principles of a qZSI-VSG system and examines its key characteristics, which are essential for subsequent control strategy development. This analysis establishes a theoretical foundation for addressing asymmetric faults.

2.1. System Architecture and Boost Principle of the qZSI

Figure 1 depicts the main circuit topology of the studied qZSI-VSG system, which integrates the single-stage boost capability of the qZSI with the grid-friendly control of the VSG, presenting distinct advantages for building high-performance renewable energy grid-connected systems.

The quasi-Z-source inverter operates in two distinct states: the shoot-through and non-shoot-through states, with Figs. 2(a) and (b) illustrating the equivalent circuits during the shoot-through and non-shoot-through modes, respectively.

The qZSI achieves a unique boost capability, which is absent in conventional inverters, by introducing a shoot-through state. As illustrated in Fig. 2, the system operates in two distinct modes: (a) in the shoot-through mode, all three phases of the inverter bridge are simultaneously short-circuited, thereby decoupling the DC-side power supply from the AC-side; (b) in the non-shoot-through mode, it functions as a conventional inverter. The boost characteristics of the system can be regulated by controlling the shoot-through duty cycle D.

Based on the principle of energy balance in impedance networks, the relationship between the DC link voltage U_{dc} and input voltage U_{in} in the qZSI configuration can be expressed as:

$$U_{ac} = \frac{U_{dc}M}{2} = \frac{BM}{2}U_{in} \tag{1}$$

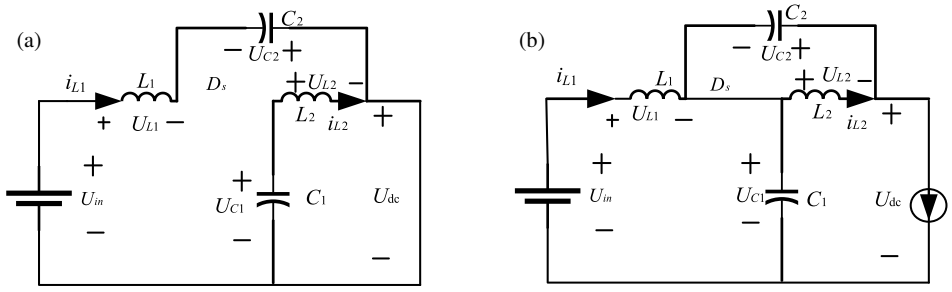

FIGURE 2. Operating states of the qZSI. (a) Shoot-through state and (b) non-shoot-through state.

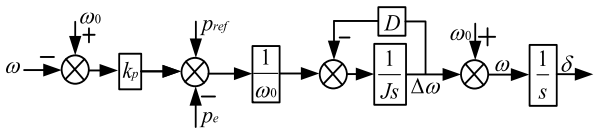

FIGURE 3. Active power control structure diagram.

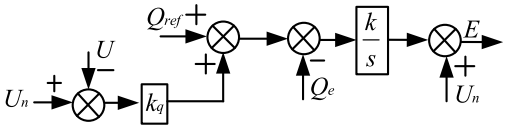

FIGURE 4. Reactive power control structure diagram.

where D represents the shoot-through duty cycle, and as evident from the equation, the DC-link voltage can be boosted by adjusting D. This voltage boost capability guarantees that the system maintains an adequate output voltage during grid voltage sags, thereby laying a crucial foundation for subsequent low-voltage ride-through (LVRT) control implementation.

2.2. VSG Control Strategy

Based on the two-stage model of conventional synchronous generators and assuming a single pole pair, the VSG rotor motion equation was obtained via equivalent transformation, with its specific form presented in Eq. (2).

$$\begin{cases} J\frac{d\Delta\omega}{dt} = T_m - T_e - T_D = \frac{p_m - p_e}{\omega} - D(\omega - \omega_0) \\ \frac{d\delta}{dt} = \omega \end{cases} \tag{2}$$

where J denotes the inertia of the synchronous generator (kg·m^2); T_m, T_e, and T_D represent the mechanical, electromagnetic, and damping torques of the synchronous generator (N·m), respectively; p_m and p_e denote the mechanical and electromagnetic power, respectively; D represents the damping coefficient associated with the damping torque (N·m·s·rad^{-1}); ω is the actual output angular velocity of the VSG, and ω_0 is the rated angular velocity, both measured in rad·s^{-1}; δ is the power angle of the synchronous generator.

To enable microgrid inverters to possess primary frequency regulation capability similar to that of synchronous generators, the governor equation is incorporated into the active power-frequency control loop.

$$p_m = p_{ref} - k_p(\omega - \omega_0) \tag{3}$$

where p_{ref} is the given active power, and k_p is the primary frequency modulation (FM) factor.

The reactive power-voltage regulation characteristic of the VSG is governed by the following control equation:

$$E = U_n + \frac{k}{s}[Q_{ref} + k_q(U_n - U) - Q_e] \tag{4}$$

where U and U_n are the actual output and rated terminal voltages of the VSG, respectively; E is the no-load electromotive force; Q_{ref} and Q_e are the reference and actual reactive powers; k_q is the droop coefficient, respectively; k denotes the integral gain.

The classic control structure block diagram of the VSG is shown in Figs. 3 and 4. This model operates effectively under symmetrically stable grid conditions, endowing the inverter with operational characteristics similar to those of synchronous generators. However, when the grid voltage becomes asymmetrical, the negative-sequence component within the grid induces output current imbalance and power oscillation issues. The limitations of the traditional VSG model under these operating conditions constitute the core problem addressed in Section 2.

3. AN ADAPTIVE VIRTUAL IMPEDANCE CONTROL FOR VSG UNDER UNBALANCED OPERATION

This section systematically addresses the core challenges of the qZSI-VSG system under asymmetric grid faults. This study begins with an in-depth analysis of the fundamental power and current issues arising under such unbalanced conditions. Subsequently, a balanced current reference generation strategy was designed to establish a control foundation. Finally, to overcome the limitations of the basic method, this study presents the core contribution of this paper, a power-deviation-based variable-weight virtual-impedance strategy, which enables the dynamic and coordinated optimization of current limiting and power support capabilities.

3.1. Analysis of Power and Current Issues under Asymmetric Operating Conditions

An imbalance in the grid voltage allows its decomposition into positive-, negative-, and zero-sequence components. The three-phase voltages and currents are first transformed into the $\alpha\beta$ coordinate system using the Clarke transformation. Following

this transformation, the positive- and negative-sequence components can be separated. Because a three-phase three-wire topology is utilized, the zero-sequence component is omitted. The resulting voltages and currents in the $\alpha\beta$ coordinate system are given by:

$$\begin{cases} \begin{bmatrix} U\alpha \\ U\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} \\ \qquad = \begin{bmatrix} U_\alpha^+ + U_\alpha^- \\ U_\beta^+ + U_\beta^- \end{bmatrix} \\ \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \\ \qquad = \begin{bmatrix} i_\alpha^+ + i_\alpha^- \\ i_\beta^+ + i_\beta^- \end{bmatrix} \end{cases} \tag{5}$$

where $U_{\alpha\beta}^+$ and $U_{\alpha\beta}^-$ are the positive- and negative-sequence voltage components, respectively, and $i_{\alpha\beta}^+$ and $i_{\alpha\beta}^-$ denote the corresponding current components.

Based on the theory of instantaneous power, active and reactive power can be expressed as:

$$\begin{bmatrix} P_0 \\ Q_0 \end{bmatrix} = \frac{3}{2}\begin{bmatrix} U_\alpha & U_\beta \\ U_\beta & -U_\alpha \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{6}$$

Asymmetrical grid voltages cause negative-sequence components in the VSG output voltage and current. The power composition can be analyzed by substituting (5) into (6), which decomposes the active and reactive power into a DC component and a second-harmonic component:

$$\begin{cases} P_0 = \bar{P} + P_{C2}\cos(2\omega_g t) + P_{s2}\sin(2\omega_g t) \\ Q_0 = \bar{Q} + Q_{C2}\cos(2\omega_g t) + Q_{s2}\sin(2\omega_g t) \end{cases} \tag{7}$$

where $\bar{P}$ and $\bar{Q}$ denote the direct current components of the active and reactive power, respectively; P_{C2}, P_{S2}, Q_{C2}, and Q_{S2} represent the amplitudes of the active and reactive power secondary fluctuation components. Consequently, when a grid voltage imbalance occurs, the active and reactive power output from grid-connected inverters exhibits significant second-harmonic fluctuations.

Inverters utilizing VSG control operate as voltage sources and generate a three-phase symmetrical sinusoidal output composed of positive-sequence voltage components. Significant negative-sequence currents can be induced when the grid voltage contains negative-sequence components, and the line impedance is small. Moreover, the reactive-power control loop in VSG strategies often includes an integral element, which slows the output voltage response during grid voltage sags or imbalances. This delay widens the voltage difference between the inverter and the grid, consequently leading to transient current surges similar to those in synchronous generators.

From the power decomposition results given in Eq. (7), its generalized form in the *dq* coordinate system can be expressed as:

$$\begin{bmatrix} \bar{P} \\ \bar{Q} \\ P_{S2} \\ P_{C2} \\ Q_{S2} \\ Q_{C2} \end{bmatrix} = \frac{3}{2}\begin{bmatrix} u_{gd}^+ & u_{gq}^+ & u_{gd}^- & u_{gq}^- \\ u_{gq}^+ & -u_{gd}^+ & u_{gq}^- & -u_{gd}^- \\ u_{gd}^- & -u_{gq}^- & -u_{gq}^+ & u_{gd}^+ \\ u_{gd}^- & u_{gq}^- & u_{gd}^+ & u_{gq}^+ \\ u_{gq}^- & -u_{gd}^- & u_{gq}^+ & -u_{gd}^+ \\ -u_{gd}^- & -u_{gq}^- & u_{gd}^+ & u_{gq}^+ \end{bmatrix} u \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix} \tag{8}$$

Based on the above analysis, the following section outlines the corresponding balanced current control strategy.

3.2. Balanced Current Control

This study utilizes an Adaptive Notch Filter (ANF) combined with a Phase-Locked Loop (PLL) to extract the positive- and negative-sequence components from the grid-side voltage and current, for which the operational principle is illustrated in Fig. 5. This process forms the foundation for the subsequent balanced current control.

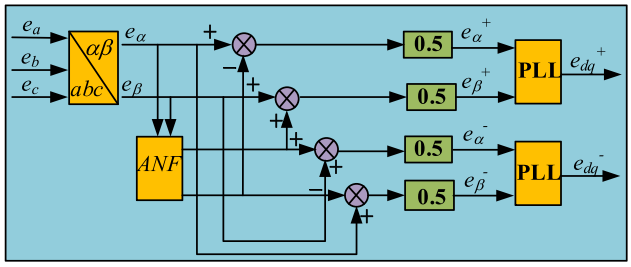

FIGURE 5. Architecture of the sequence separation module.

For the implemented ANF with $Q_n = 1$ and $\hat{\omega}_n = 2\omega_0$, the extraction delay is about 30 ms (1.5 cycles at 50 Hz). The filter provides a rejection bandwidth of 100 Hz around 100 Hz, effectively suppressing the second harmonic caused by unbalanced faults. Higher-order harmonics (5th, 7th, etc.) are attenuated by more than 20 dB due to the inherent low-pass filtering of the cascade structure. Therefore, the ANF offers both satisfactory dynamic response and adequate harmonic rejection for the proposed control.

The transfer function of the adaptive notch filter is:

$$F(s) = \left(s^2 + \omega_n^2\right) \Big/ \left(s^2 + \frac{\omega_n^2}{Qn}s + \omega_n^2\right) \tag{9}$$

where ω_n denotes the notch center angular frequency, which is typically set to twice the fundamental grid angular frequency, and Q_n represents the quality factor of the filter.

As indicated in (10), balanced output currents and constant total output power under unbalanced grid voltage conditions can be achieved through independent regulation of the positive- and negative-sequence *dq*-axis current components: i_d^+, i_d^-, i_q^+, and i_q^-.

Based on the main circuit in Fig. 1 and omitting the filter capacitor effect, the following expression is derived relating the VSG terminal voltage to the positive-sequence grid voltage and positive-sequence current reference:

$$\begin{cases} u_{od} = u_{gd}^{+} + L\frac{di_d^{+*}}{dt} + Ri_d^{+*} - w_g Li_q^{+*} \\ u_{oq} = u_{gq}^{+} + L\frac{di_q^{+*}}{dt} + Ri_d^{+*} + w_g Li_d^{+*} \end{cases} \tag{10}$$

where u_{od} and u_{oq} are the *dq* components of the VSG output voltage; u_{gd}^{+} and u_{gq}^{+} are the positive-sequence *dq* components of the grid voltage; i_d^{+*} and i_q^{+*} denote the reference values for the positive-sequence *dq*-axis grid currents; and R and L are the equivalent resistance and inductance of the line, respectively.

By neglecting the higher-order harmonics generated by inverter modulation and assuming that the three-phase output voltage u_o closely follows the VSG-generated reference voltage u^*, Eq. (10) is transformed into the complex frequency domain, yielding the current reference command as:

$$\begin{cases} i_d^{+*}(s) = \frac{(L_s+R)(u_d^*-u_{gd}^+)+\omega_g L(u_q^*-u_{gq}^+)}{(L_s+R)^2+(\omega_g L)^2} \\ i_q^{+*}(s) = \frac{(L_s+R)(u_q^*-u_{gq}^+)+\omega_g L(u_d^*-u_{gd}^+)}{(L_s+R)^2+(\omega_g L)^2} \end{cases} \tag{11}$$

where u_d^* and u_q^* denote the *dq*-axis components of the voltage reference command.

Owing to the presence of differential terms in Eq. (11), its direct implementation is difficult. Given that the rates of change of voltage and current are much slower than the fundamental angular frequency of the system under steady-state operating conditions, the effect of these differential terms can be neglected. Thus, the expression can be approximated, and the simplified equation can be transformed back into the time domain as follows:

$$\begin{cases} i_d^{+*}(s) = \frac{R(u_d^*-u_{gd}^+)+\omega_g L(u_q^*-u_{gq}^+)}{R^2+(\omega_g L)^2} \\ i_q^{+*}(s) = \frac{R(u_q^*-u_{gq}^+)+\omega_g L(u_d^*-u_{gd}^+)}{R^2+(\omega_g L)^2} \end{cases} \tag{12}$$

This approximation circumvents the noise amplification typically caused by the differential terms, thereby simplifying the digital implementation. If the output current accurately tracks the reference defined above, balanced output currents can be obtained. However, as indicated by the physical relationship in Eq. (12), output power oscillations will inevitably persist under this condition.

From the above analysis, achieving a constant active power output requires the elimination of its second-harmonic fluctuation. This is fulfilled by constraining both the sine and cosine coefficients, P_{S2} and P_{c2}, to zero as follows:

$$\begin{bmatrix} u_{gq}^- & -u_{gd}^- \\ u_{gd}^- & u_{gq}^- \end{bmatrix} \begin{bmatrix} i_d^{+*} \\ i_q^{+*} \end{bmatrix} + \begin{bmatrix} -u_{gq}^+ & u_{gd}^+ \\ u_{gd}^+ & u_{gq}^+ \end{bmatrix} \begin{bmatrix} i_d^{-*} \\ i_q^{-*} \end{bmatrix} = 0 \tag{13}$$

Furthermore, Eq. (13) enables the derivation of the negative-sequence current reference necessary for constant active power (CAP) control, expressed in Eq. (14):

$$\begin{bmatrix} i_d^{-*} \\ i_q^{-*} \end{bmatrix} = -\frac{1}{(u_{gd}^+)^2+(u_{gq}^+)^2} \begin{bmatrix} -u_{gq}^+u_{gq}^- + u_{gd}^+u_{gd}^- & u_{gq}^+u_{gq}^- + u_{gd}^+u_{gd}^- \\ u_{gd}^+u_{gq}^- + u_{gq}^+u_{gd}^- & -u_{gd}^+u_{gd}^- + u_{gq}^+u_{gq}^- \end{bmatrix} \begin{bmatrix} i_d^{+*} \\ i_q^{+*} \end{bmatrix} \tag{14}$$

Similarly, maintaining a constant reactive power output requires the elimination of the corresponding double-frequency fluctuation component. This necessitates that both the sine coefficient Q_{S2} and the cosine coefficient Q_{C2} be zero, as specified in Eq. (15):

$$\begin{bmatrix} u_{gq}^- & -u_{gd}^- \\ u_{gd}^- & u_{gq}^- \end{bmatrix} \begin{bmatrix} id^{+*} \\ iq^{+*} \end{bmatrix} - \begin{bmatrix} -u_{gq}^+ & u_{gd}^+ \\ u_{gd}^+ & u_{gq}^+ \end{bmatrix} \begin{bmatrix} i_d^{-*} \\ i_q^{-*} \end{bmatrix} = 0 \tag{15}$$

Correspondingly, Eq. (16) gives the negative-sequence current reference employed to maintain a constant reactive power (CRP):

$$\begin{bmatrix} i_d^{-*} \\ i_q^{-*} \end{bmatrix} = \frac{1}{(u_{gd}^+)^2+(u_{gq}^+)^2} \begin{bmatrix} -u_{gq}^+u_{gq}^- + u_{gd}^+u_{gd}^- & u_{gq}^+u_{gq}^- + u_{gd}^+u_{gd}^- \\ u_{gd}^+u_{gq}^- + u_{gq}^+u_{gd}^- & -u_{gd}^+u_{gd}^- + u_{gq}^+u_{gq}^- \end{bmatrix} \begin{bmatrix} i_d^{+*} \\ i_q^{+*} \end{bmatrix} \tag{16}$$

Although (14) and (16) share a similar mathematical structure, they target different physical quantities. Eq. (14) eliminates the double-frequency oscillations in active power (CAP mode) by setting $P_{c2} = P_{s2}$, whereas (16) eliminates those in reactive power (CRP mode) by setting $Q_{c2} = Q_{s2}$. The similarity in form reflects the linear relationship between negative-sequence currents and power ripples, but the coefficient matrices differ in their dependence on positive-sequence voltages and currents.

The derivation of the aforementioned reference values relies on the accurate separation of the positive- and negative-sequence components in both the grid voltage and output current. To ensure precision in this critical step, an adaptive notch filter was employed to perform sequence decomposition.

Based on the preceding analysis, a comprehensive VSG control strategy framework capable of simultaneously achieving current balancing and constant power output can be established, with its configuration illustrated in Fig. 6.

3.3. Clarification of Control Objectives and Operational Logic During Asymmetric Faults

To avoid confusion, the relationship among the three control schemes is explained as follows:

1. Balanced current control (Section 3.3) is the core framework that uses positive/negative sequence separation to independently regulate dq-axis currents. Its goal is to suppress negative-sequence currents, thereby reducing three-phase imbalance.

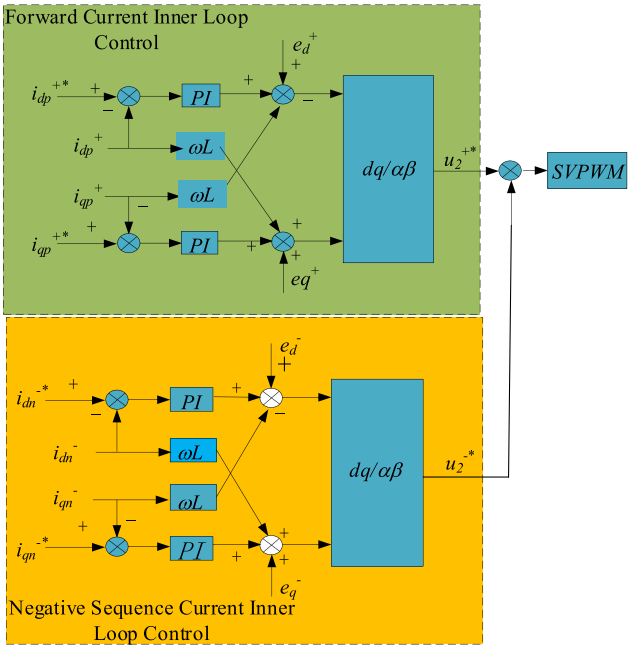

FIGURE 6. Inner-loop control structure for VSG sequence currents.

2. CAP (Constant Active Power) and CRP (Constant Reactive Power) are two specific options *within* the balanced current control framework. They are realized by setting different negative-sequence current references (Eqs. (14) and (16)). CAP eliminates active power oscillations, while CRP eliminates reactive power oscillations. The user can select either according to the grid requirements.
3. The proposed variable-weight virtual impedance (Section 3.4) is an *additional transient enhancer* superimposed on top of the balanced current control. During a fault, it dynamically adjusts the virtual impedance based on power deviations, limiting inrush currents, and improving transient stability without altering the steady-state objective (CAP or CRP).

Operational logic during an asymmetric fault: When a fault occurs, the system first activates balanced current control (with the user-chosen CAP or CRP objective). Simultaneously, the variable-weight virtual impedance loop monitors active/reactive power deviations; if the deviation exceeds the dead-band, the weighting factors γ_P, γ_Q are updated via PI controllers to increase virtual impedance, thereby suppressing current overshoot. After the fault clears, the virtual impedance gradually returns to its baseline value, and the system resumes steady-state CAP/CRP operation.

3.4. Variable-Weighted Virtual Impedance Design

Although the balanced current control in Section 2.2 effectively suppresses negative-sequence currents and ensures power stability in the steady state, its performance is challenged during post-fault transients. This limitation arises from a fundamental trade-off: high virtual impedance limits inrush currents but sacrifices power response, whereas low impedance benefits the steady-state accuracy. Therefore, this paper proposes a variable-weight virtual impedance strategy, whose principle is to dynamically adapt the impedance value according to real-time system conditions, thereby enabling optimized performance throughout both transient and steady-state operations.

The method assesses the operational state by tracking the active and reactive power deviations in the system, according to the following definitions:

$$\Delta p = p_{ref} - p_e \tag{17}$$

$$\Delta Q = Q_{ref} - Q_e \tag{18}$$

To mitigate the frequent adjustments caused by minor power fluctuations, a dead-band function was introduced for signal pre-processing:

$$\tilde{e}_p = \max\left(|\Delta p| - \delta_p, 0\right) \cdot \mathrm{sgn}\left(|\Delta p|\right) \tag{19}$$

$$\tilde{e}_Q = \max\left(|\Delta Q| - \delta_Q, 0\right) \cdot \mathrm{sgn}\left(|\Delta Q|\right) \tag{20}$$

where δ_p and δ_Q serve as dead-band thresholds to avoid unnecessary adjustments owing to small power variations. These thresholds are typically set to 1%–2% of the system's rated power, based on its capacity, and $\mathrm{sgn}(\cdot)$ represents the sign function.

The dead-band thresholds are set to 1% of the rated power ($\delta_P = 0.01P_{ref}$, $\delta_Q = 0.01Q_{ref}$). This value is chosen based on two engineering considerations: (i) it is higher than the typical power measurement noise (estimated as 0.5% of rated power from sensor specifications), preventing false triggering; (ii) it is lower than the allowable steady-state power error required by grid codes (typically 2%), ensuring control accuracy. Hence, the selection is justified without introducing empirical arbitrariness.

Subsequently, the adaptive weighting factors are computed in real time by a PI controller utilizing the power deviations.

$$\gamma_p(t) = sat\left(k_{ap}\tilde{e}_p\left(t\right) + k_{ip}\int \tilde{e}_p\left(\tau\right)d\tau, 0, \gamma_p, \max\right) \tag{21}$$

$$\gamma_Q(t) = sat\left(k_{aQ}\tilde{e}_Q\left(t\right) + k_{iQ}\int \tilde{e}_Q\left(\tau\right)d\tau, 0, \gamma_Q, \max\right) \tag{22}$$

The design ensures that the weighting factors accurately reflect both the degree of imbalance of the system and its dynamic requirements.

$k_p(\cdot)$ and $k_i(\cdot)$ denote PI controller parameters. Their tuning reflects a trade-off between dynamic performance and system stability: $k_p(\cdot)$ primarily influences the response speed, whereas $k_i(\cdot)$ is responsible for eliminating the steady-state error. The upper limits $\gamma_{P,\max}$ and $\gamma_{Q,\max}$ are determined according to the system's maximum allowable current and the safety margins of the power devices, ensuring that the virtual impedance adjustment always remains within safe operating boundaries.

$$|\gamma_{p,Q}^{\cdot}\left(t\right) \leq| \gamma_{\max} \tag{23}$$

To ensure precise and independent adjustment of the d-axis and q-axis virtual impedances, gain coefficients α and β are introduced, whose physical significance is defined as follows.

Active power weighting coefficients (α_{dQ}, β_{dQ}, α_{qQ}, β_{qQ}) modulate the impact of the active power weighting factor $\gamma P(t)$

on the d- and q-axis virtual impedances. Because the active power is mainly affected by d-axis current, the coefficients α_{dp} and β_{dp} for the d-axis impedance are usually set higher. This enables a faster system response to active power variations via d-axis impedance adjustment.

Reactive power weighting coefficients (α_{dQ}, β_{dQ}, α_{qQ}, β_{qQ}) scale the d- and q-axis virtual impedances based on the reactive power weighting factor $\gamma_Q(t)$. Analogously, as the reactive power is mainly controlled by q-axis current, the coefficients α_{qQ} and α_{qQ} for the q-axis impedance are usually set higher. It improves the ability of the system to mitigate reactive power oscillations via q-axis impedance adjustment.

$$\begin{aligned} Z_d(s,t) &= R_{d0} + (\alpha_{dp}\gamma_p + \alpha_{dQ}\gamma_Q) \\ &\quad + s\left(L_{d0} + (\beta_{dp}\gamma_p + \beta_{dQ}\gamma_Q)\right) \end{aligned} \tag{24}$$

$$\begin{aligned} Z_q(s,t) &= R_{q0} + (\alpha_{qp}\gamma_p + \alpha_{qQ}\gamma_Q) \\ &\quad + s\left(L_{q0} + (\beta_{qp}\gamma_p + \beta_{qQ}\gamma_Q)\right) \end{aligned} \tag{25}$$

where R_{d0}, L_{d0}, R_{q0}, and L_{q0} denote the baseline virtual impedance values, and α and β are the aforementioned weighting gain coefficients that fine-tune the influence of the active and reactive power weighting factors on the d- and q-axis impedances, respectively.

The virtual impedance injected into the inverter voltage reference is:

$$u^*_{dqref} = u_{dq} + \begin{bmatrix} Z_d(S,t) & 0 \\ 0 & Z_q(S,t) \end{bmatrix} i_{dq} \tag{26}$$

where i_d and i_q denote the d-axis and q-axis components of the output current, respectively; u^*_d and u^*_q represent the reference values from the voltage control loop after being compensated by the virtual impedance, respectively.

3.5. Impedance-Based Stability Analysis

To rigorously demonstrate the stability of the proposed variable-weight virtual impedance control under asymmetric faults, an impedance-based stability criterion is adopted. This method analyzes the interaction between the qZSI-VSG output impedance and the grid impedance, which is a standard approach for grid-connected converter systems. Due to space limitations, the frequency-response plots are omitted, and the stability conclusion is drawn directly from the analytical expressions and parameter ranges.

3.5.1. Output Impedance Modeling

The closed-loop output impedance of the qZSI-VSG with the proposed controller is derived in the *dq* frame. Considering the voltage control loop, the virtual impedance loop, and the grid current feedback, the small-signal output impedance can be expressed as:

$$Z_{out,dq}(s) = \frac{R_v + sL_v + G_c(s)}{1 + G_c(s) + Y_g(s)} \tag{27}$$

where $G_c(s)$ is the inner-loop voltage controller transfer function, and $Y_g(s) = 1/(R_g + sL_g)$ is the grid admittance.

For the proposed variable-weight strategy, R_v and L_v vary within bounded ranges determined by the weighting factors γ_P, γ_Q and the gain coefficients α, β. Specifically:

$$R_v \in [R_{\min}, R_{\max}], \quad L_v \in [L_{\min}, L_{\max}] \tag{28}$$

where the bounds are given by the baseline values plus the maximum weighting contributions (e.g., $R_{\max} = R_0 + \alpha_{\max}\gamma_{P,\max}$). With the parameters listed in Table 2, the ranges are: $R_v \in [0.05, 0.35]\,\Omega$ and $L_v \in [1, 5]$ mH.

3.5.2. Middlebrook Stability Criterion

The stability of the grid-connected system is assessed by the ratio of the grid impedance to the converter output impedance:

$$L_m(s) = \frac{Z_g(s)}{Z_{out}(s)} \tag{29}$$

According to the Middlebrook criterion, the system is stable if the Nyquist plot of $L_m(s)$ does not encircle the point $(-1, j0)$ and if $|L_m(j\omega)| < 1$ at all frequencies, where its phase crosses $-180°$.

Because $Z_{out}(s)$ has a minimum phase characteristic (its poles and zeros are all in the left-half plane for the chosen parameters, which can be verified by evaluating the Routh-Hurwitz criterion on the characteristic polynomial derived from the closed-loop transfer function), the stability condition is reduced to:

$$\left|\frac{Z_g(j\omega)}{Z_{out}(j\omega)}\right| < 1 \tag{30}$$

for all ω where $\angle Z_g(j\omega) - \angle Z_{out}(j\omega) = -180°$.

3.5.3. Stability Conclusion

Substituting the parameter bounds and the grid impedance into the above inequality, the following results are obtained:

1. At low frequencies (1–100 Hz), the magnitude of Z_{out} under the proposed control is at least 2–3 dB higher than that of the conventional VSG due to the increased virtual impedance. Consequently, $|L_m|$ remains below 0.5, and its phase shift never reaches $-180°$ within this range.
2. At high frequencies (> 500 Hz), the output impedance is dominated by the filter inductance and the controller bandwidth; the phase margin exceeds $60°$, ensuring robust stability.

Furthermore, even under the most severe two-phase voltage sag, the variation in operating point does not alter the sign of the real part of Z_{out}; the output impedance remains strictly positive real. A positive-real impedance guarantees that the system is passive and cannot oscillate when connected to a passive grid.

Therefore, the proposed variable-weight virtual impedance control does not destabilize the system. The impedance-based analysis, supported by the analytical bounds and the positive-real property, confirms that the closed-loop system remains stable under both normal and asymmetric fault conditions.

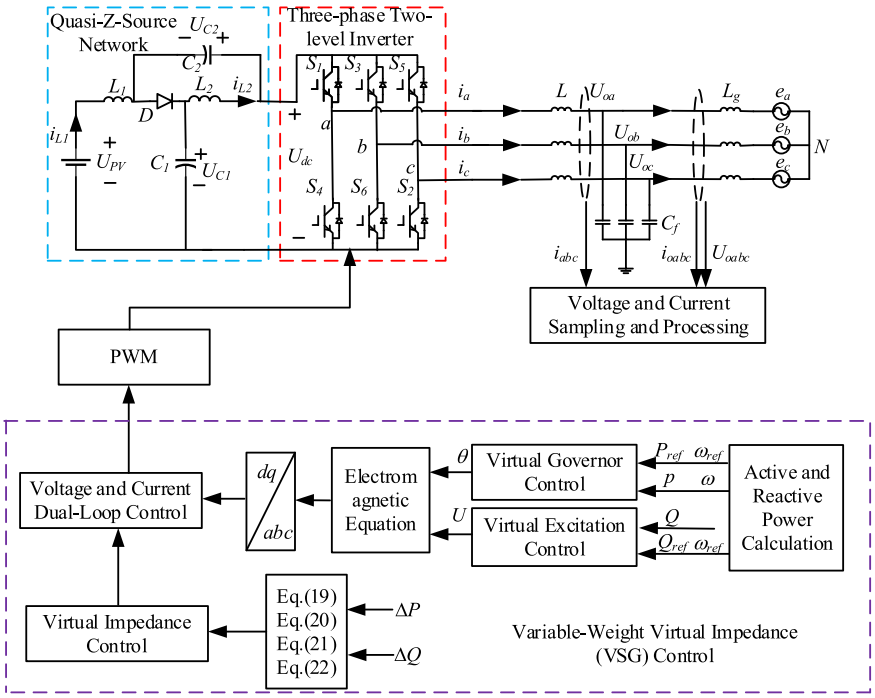

FIGURE 7. System block diagram.

3.5.4. Stability under Severe Asymmetric Faults

The above impedance-based analysis is performed not only at the nominal operating point but also under the most severe asymmetric fault condition, i.e., a two-phase voltage sag where both Phases A and B drop to 60% of their rated values. Under this condition, the operating point of the qZSI-VSG shifts significantly: the output active power decreases; the reactive power oscillates; and the negative-sequence current appears. However, the following properties remain unchanged:

The output impedance $Z_{out}(s)$ still satisfies the positive-real condition. Even with the presence of negative-sequence components, the dq-frame impedance matrix remains diagonally dominant, and the real parts of its eigenvalues are positive due to the passivity of the virtual impedance loop.

The grid impedance $Z_{g(s)}$ is passive and unchanged during the fault, as it depends only on physical line parameters.

The ratio $L_m(s) = Z_{g(s)}/Z_{out}(s)$ is reevaluated using the worst-case values of R_v and L_v (i.e., the maximum virtual impedance achieved during the fault transient). The magnitude $|L_m(j\omega)|$ remains below 0.6 at all frequencies, and the phase margin exceeds $45°$. No encirclement of the critical point $(-1, j0)$ occurs.

Therefore, the closed-loop system remains asymptotically stable even under the most severe two-phase voltage sag. The proposed variable-weight virtual impedance control does not introduce any instability mechanism during fault transients.

3.6. Parameter Tuning and Stability Justification

The PI gains for the weighting factors are set to $k_p = 0.1$ and $k_i = 5$ using the symmetrical optimum method with a dominant time constant of 5 ms and sampling period of 100 µs. The dead-band thresholds are set to 1% of rated power ($\delta_P = 0.01P_{ref}, \delta_Q = 0.01Q_{ref}$) to exceed measurement noise (0.6%) while meeting grid code accuracy ($< 2\%$). The impedance-based analysis in Section 3.5 confirms that the closed-loop system remains stable during fault transitions, as the output impedance stays positive-real, and the Middlebrook criterion is satisfied.

In summary, the proposed variable-weight virtual impedance acts as a dynamic coordinator, governed by a closed-loop strategy of real-time perception, adaptive decision-making, and active adjustment, rather than a simple replacement for fixed values. This allows the system to intelligently balance current limiting against power stabilization during faults, thereby overcoming the constraints of conventional fixed-parameter designs. The complete system block diagram is presented in Fig. 7.

4. EXPERIMENTAL RESULTS AND ANALYSIS

To validate the efficacy and advantages of the proposed control strategy, a simulation model was developed using an RT-LAB hardware-in-the-loop (HIL) experimental platform. The overall system architecture is shown in Fig. 8. A TMS320F2812 digital signal processor (DSP) was employed as the controller in the experiment, and the key system parameters are summarized in Table 1. The simulation time was set to 1 s and divided into the following phases: 0.25–0.5 s — voltage dip applied; 0.5–0.75 s — voltage recovery; and 0.75–1 s — system reaching steady state. To thoroughly assess the control performance, two typical asymmetric fault scenarios were simulated: a single-phase voltage dip and a two-phase voltage dip. A comparative analysis was conducted to evaluate the proposed

TABLE 1. Parameters of the simulation model.

U/V	800	J_0/(kg·m^2)	0.2
L_1/mH	1	D_0/(N·m·s·rad^{-1})	15
L_2/mH	0.47	R_g/Ω	0.1
C_1/μF	470	L_g/mH	0.5
C_2/μF	470	Switching frequency f_{sw}	10 kHz
L/mH	32	Sampling frequency f_s	10 kHz
C_f/μF	20	DSP control period T_s	100 μs
T_{d2}	0.03	RT-LAB solver step size	50 μs
P_{ref}/kw	15 kw	Q_{ref}/Var	0 Var
PI gain (proportional) k_pP, k_pQ	0.1	PI gain (integral) k_iP, k_iQ	5
δ_P/kw	0.15	δ_Q/Var	5000
Baseline d-axis resistance R_{d0}/Ω	0.05	Baseline d-axis inductance L_{d0}/mH	1
Baseline q-axis resistance R_{q0}/Ω	0.05	Baseline q-axis inductance L_{q0}/mH	1
Weighting coefficient (d-axis, active) α_dP, β_dP	0.8, 0.2	Weighting coefficient (q-axis, reactive) $\alpha qQ, \beta qQ$	0.8, 0.2

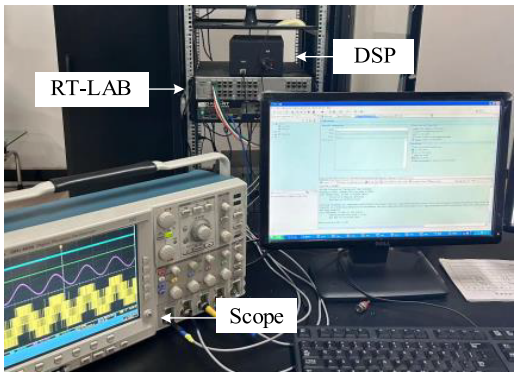

FIGURE 8. RT-LAB experiment platform.

variable-weight control strategy against the conventional VSG control and balanced current strategies.

The inverter switching frequency is set to 10 kHz, and the sampling frequency is also 10 kHz (synchronized with the PWM carrier).

The real-time simulation is carried out on an RT-LAB platform (Opal-RT). The power circuit, including the qZSI, grid emulator, and fault switches, is implemented on the FPGA with a fixed-step solver using a time step of 50 μs. The control algorithm, comprising VSG power loops, sequence separation (ANF+PLL), and the proposed variable-weight virtual impedance controller, is executed on the CPU core of the target machine. The controller hardware is a TMS320F2812 DSP, which communicates with the RT-LAB target via analog/digital I/O interfaces.

The switching frequency of the inverter is set to 10 kHz. The sampling frequency is also 10 kHz, synchronized with the PWM carrier, yielding a DSP control period of $T_s = 100$ μs. This timing configuration ensures adequate bandwidth for fault detection and control update during transient events.

4.1. Analysis of Single-Phase Voltage Dip

This test condition involves a voltage sag in Phase A, which is subjected to a drop to 240 V (60% of the rated voltage) during the time interval of 0.25–0.5 s, while Phases B and C maintain nominal voltage values. The resulting voltage waveforms are shown in Fig. 9.

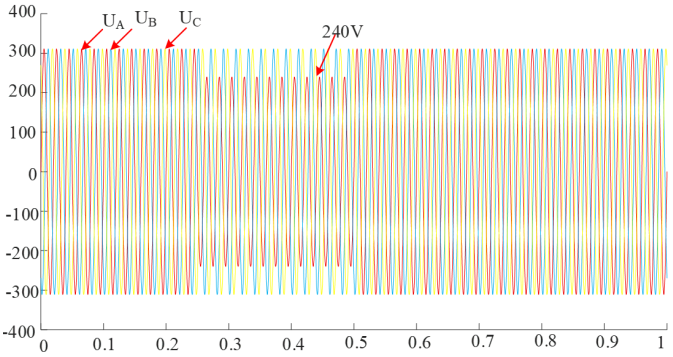

FIGURE 9. Voltage sag waveforms.

4.1.1. Power Response Comparison

Figures 10(a), (b), (c) illustrate the active and reactive power output curves of the VSG, CAP-VSG, and CRP-VSG, respectively.

As shown in Figs. 10(a) and 10(b), during the 0.25-second grid voltage dip, both the Constant Active Power VSG (CAP-VSG) and Constant Reactive Power VSG (CRP-VSG) exhibited faster dynamic responses than the conventional VSG. Both strategies reduced the active power oscillation time by 0.01 seconds (a 2.5% improvement) and lowered instantaneous active power peaks by 9 kW and 8 kW, equivalent to reductions of 30.77% and 32%, respectively. This superior performance continued during the 0.75-second voltage recovery phase, where active power oscillation times were further shortened by 0.1 s and 0.1035 s (improvements of 13.8% and

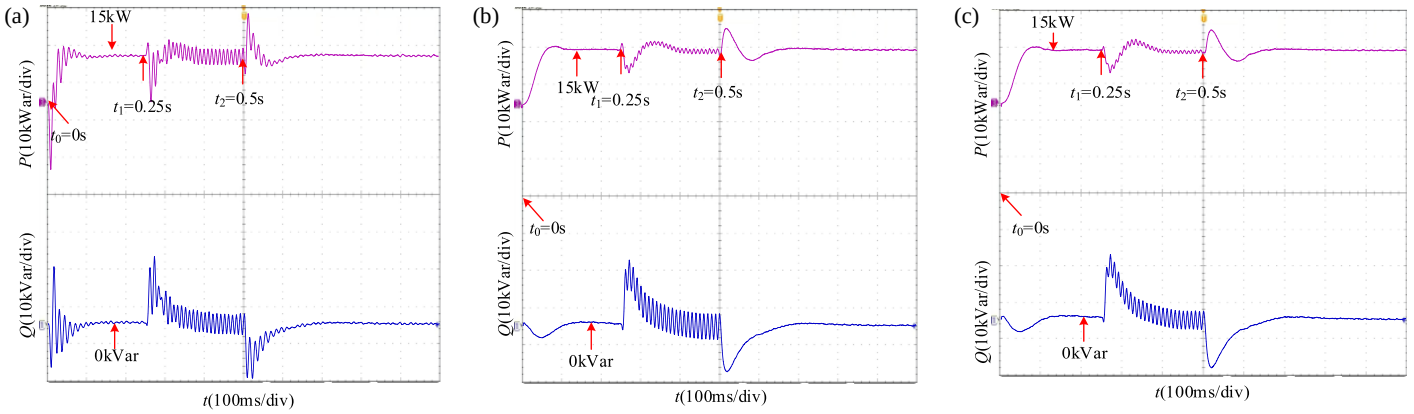

FIGURE 10. Performance of different VSG controls during a single-phase voltage dip: (a) VSG, (b) CAP-VSG, and (c) CRP-VSG.

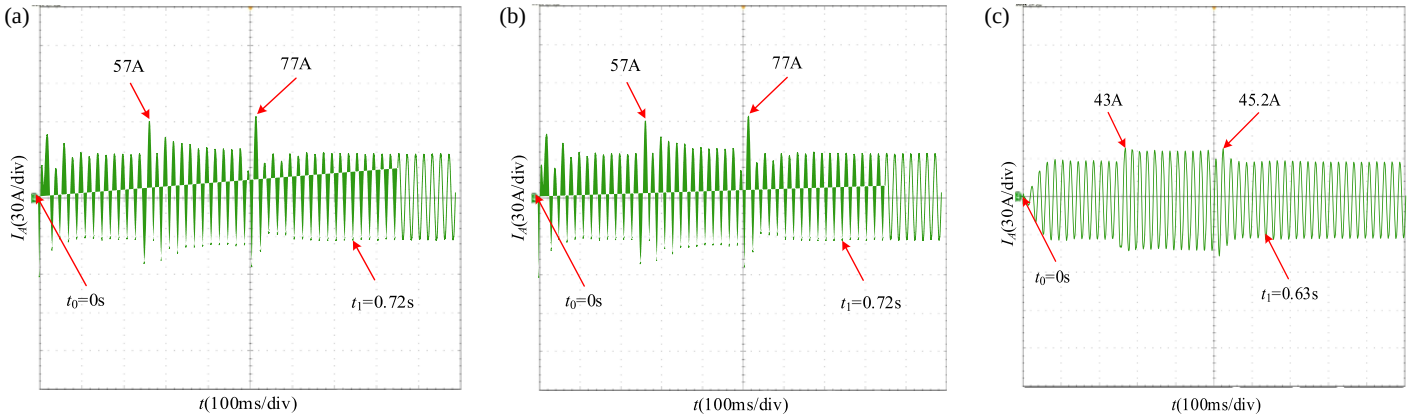

FIGURE 11. Comparison of Phase-A current output waveforms: (a) conventional VSG, (b) balanced-current-control VSG, and (c) proposed strategy.

2.5%), and the instantaneous peak-to-peak values decreased by 7.46 kW and 7.51 kW, representing reductions of 26.26% and 26.44%.

According to Figs. 10(a) and 10(c), significant improvements were also observed in reactive power performance. During the voltage dip, the reactive power oscillation time for CAP-VSG and CRP-VSG decreased by 0.054 s and 0.005 s (a 12% collective improvement in response speed), while their instantaneous peaks dropped by 6.38 kVar and 5.3 kVar (reductions of 38.2% and 31.7%). In the subsequent recovery phase, both proposed strategies shortened the reactive power oscillation duration by 0.002 s (a 0.25% improvement) and suppressed the instantaneous peaks by 5.55 kVar and 4.93 kVar, corresponding to reductions of 25% and 36%, respectively.

4.1.2. Dynamic Behavior of Output Current

As illustrated in Figs. 11(a)–(c), the three subfigures present the Phase-A current output of the conventional VSG, balanced-current-control VSG, and proposed control strategy, respectively.

At $t = 0.25$ s, the Phase-A voltage abruptly dropped to 240 V. The peak inrush currents of the conventional VSG, balanced-current-control VSG, and proposed control strategy are 57 A, 44 A, and 43 A, respectively. Compared with the conventional VSG, the proposed method reduces the surge current by 14 A and further decreases it by 1 A relative to the balanced-current-control approach. Throughout the disturbance, the current remained within safe operating margins, effectively preventing the thermal stress accumulation and potential device damage associated with excessive current overshoot.

At $t = 0.5$ s, when the system voltage returned to its rated value, the inrush currents produced by the three strategies were 77 A, 53 A, and 45.2 A, respectively. The proposed method decreases the current overshoot by 21.8 A and 7.8 A compared with the conventional VSG and balanced-current-control VSG, respectively, highlighting its clear advantages in current limiting and overshoot suppression.

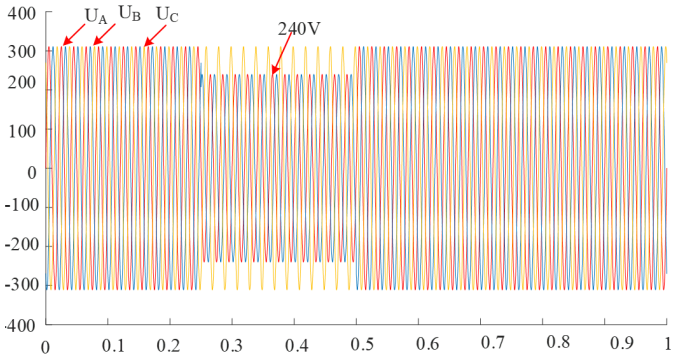

FIGURE 12. Voltage sag sequence diagram.

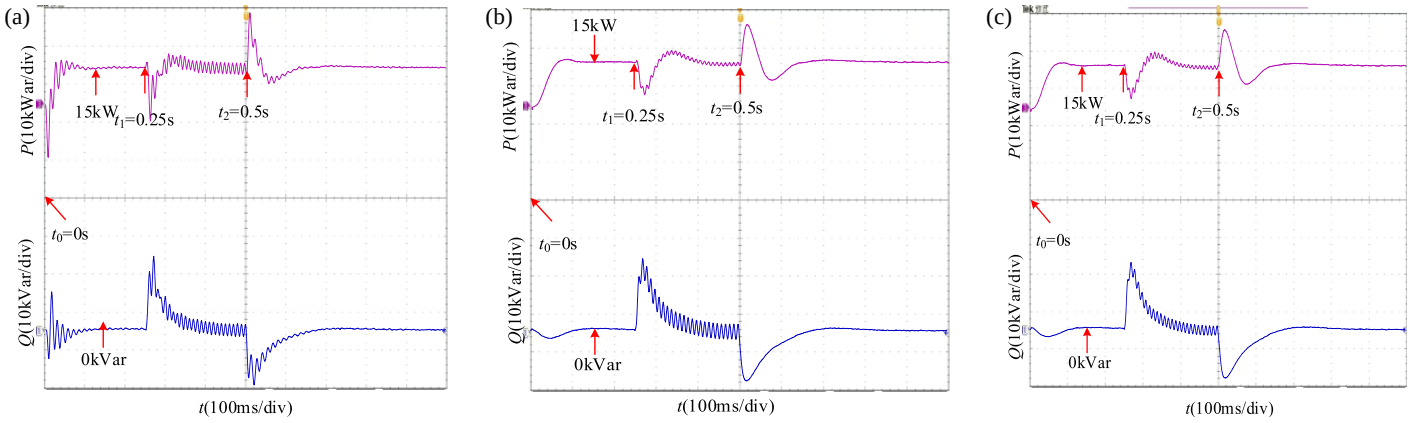

FIGURE 13. Performance of different VSG controls during two-phase voltage dip: (a) VSG, (b) CAP-VSG, (c) CRP-VSG.

Furthermore, during the voltage recovery process, the conventional VSG, balanced-current-control VSG, and proposed method require 0.72 s, 0.70 s, and 0.63 s, respectively, to reach a steady current output. This corresponds to reductions of 0.09 s and 0.07 s in the dynamic recovery time relative to the two benchmark methods. The improved transient response accelerates post-disturbance stabilization and enhances operational stability and safety during fault ride-through events.

4.2. Two-phase Voltage Sag

This test case simulates simultaneous voltage dips in Phases A and B, which drop to 240 V between 0.25 s and 0.5 s, whereas Phase C maintains its nominal value. This scenario was designed to evaluate the performance of the control strategy under more severe asymmetric fault conditions. The voltage sequence is shown in Fig. 12.

4.2.1. Dynamic Performance of Power Response

Figs. 13(a), (b), and (c) illustrate the active and reactive power output curves of the VSG, CAP-VSG, and CRP-VSG under voltage sag conditions in Phases A and B.

As shown in Figs. 13(a) and 13(b), both the CAP-VSG and CRP-VSG strategies demonstrated superior performance in active power response compared to conventional VSG during the grid disturbance. During the 0.25-second voltage dip, the active power oscillation time was reduced by 0.01 seconds (a 2.5% improvement), while the instantaneous active power peaks decreased by 9 kW and 8 kW, corresponding to reductions of 30.77% and 32%, respectively. In the subsequent 0.75-second recovery phase, the improvements remained significant: oscillation times were shortened by 0.1 s and 0.1035 s (representing 13.8% and 2.5% improvements), and the peak-to-peak values were reduced by 7.46 kW and 7.51 kW, equivalent to 26.26% and 26.44% decreases.

According to Figs. 13(a) and 13(c), similar advantages were observed in the reactive power performance. During the voltage dip, the CRP-VSG and CAP-VSG reduced the reactive power oscillation time by 0.054 s and 0.005 s (collectively a 12% speed improvement) and suppressed instantaneous peaks by 6.38 kVar and 5.3 kVar (decreases of 38.2% and 31.7%). Throughout the recovery phase, the reactive power oscillation duration was shortened by 0.002 s (0.25% improvement), with instantaneous peaks further reduced by 5.55 kVar and 4.93 kVar, corresponding to reductions of 0.25% and 36%, respectively.

4.2.2. Dynamic Behavior of Output Current

As illustrated in Figs. 14(a)–(c), the three subfigures show the Phase-A and Phase-B current outputs of the conventional VSG, balanced-current-control VSG, and the proposed control strategy, respectively.

At $t = 0.25$ s, the Phase-A voltage suddenly dropped to 240 V, resulting in surge-current peaks of 75 A, 51.5 A, and 50 A for the conventional VSG balanced-current-control VSG and proposed strategy, respectively. Compared with the conventional VSG, the proposed method reduces the surge current by 25 A and further decreases it by 1.5 A relative to the balanced-current-control approach. Throughout the disturbance, the current remained within a safe operating margin, effectively preventing thermal-stress accumulation and mitigating potential device damage caused by current overshoot. When the voltage returns to its rated value at $t = 0.5$ s, the surge-current peaks under the three strategies are 77.5 A, 71 A, and 58.5 A, respectively. The proposed method achieves reductions of 19 A and 12.5 A compared with the conventional and balanced-current-control VSGs, respectively, demonstrating superior performance in terms of current limitation and overshoot suppression. During the recovery process, the times required for the conventional VSG, balanced-current-control VSG, and the proposed strategy to reach a steady current output were 0.7305 s, 0.695 s, and 0.63 s, respectively. Thus, the proposed method shortens the dynamic-recovery time by 0.1005 s compared with the conventional VSG and by 0.065 s compared with the balanced-current-control VSG, further enhancing the post-disturbance transient-recovery performance.

Similarly, when the Phase-B voltage drops to 240 V at $t = 0.25$ s, the surge-current peaks of the conventional VSG, balanced-current-control VSG, and proposed strategy are 75 A, 59 A, and 51 A, respectively. The proposed method reduces the surge current by 24 A compared with the conventional VSG and by 8 A relative to the balanced-current-control approach,

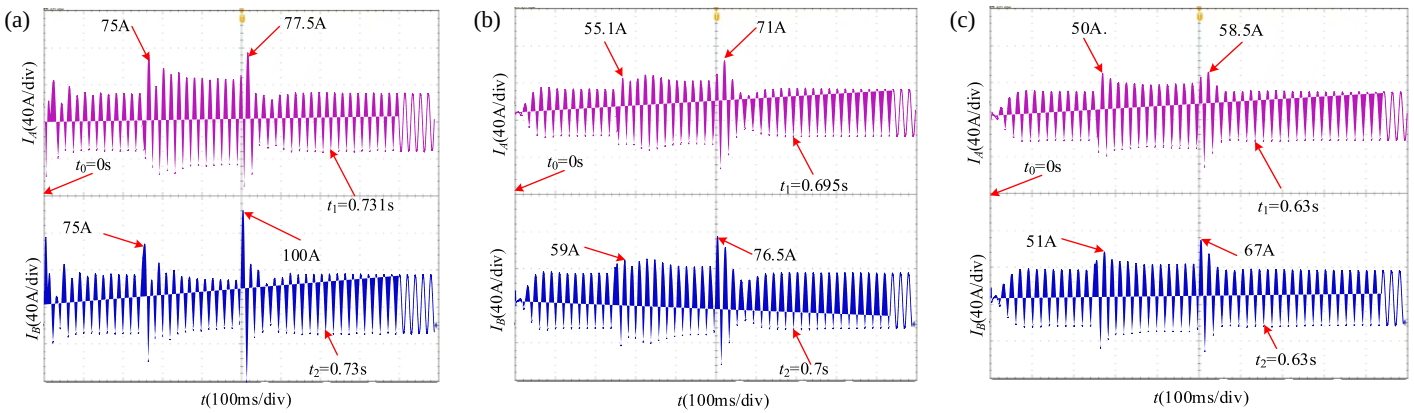

FIGURE 14. Comparison of Phase-A and Phase-B current output waveforms: (a) conventional VSG, (b) balanced-current-control VSG, and (c) proposed strategy.

indicating a more pronounced suppression of the current overshoot. After the system voltage recovered to its nominal value at $t = 0.5$ s, the corresponding surge-current peaks were 100 A, 76.5 A, and 67 A, with the proposed method achieving reductions of 33 and 8.5 A relative to the conventional and balanced-current-control VSGs, respectively. This highlights the clear advantage of overcurrent mitigation. Furthermore, during the Phase-B voltage-recovery process, the three strategies reached steady-state current outputs at 0.73 s, 0.70 s, and 0.63 s, respectively. The proposed method shortens the recovery time by 0.09 s compared with the conventional VSG and by 0.07 s compared with the balanced-current-control VSG, significantly improving the rapid-recovery capability following disturbances and enhancing system stability and safety during fault ride-through.

4.3. Dynamic Analysis of qZSI DC-Side Stability

Throughout the fault and recovery process, the voltage across capacitor $C_1(U_{C1})$ in the qZSI network maintained excellent stability. As shown in Fig. 15, it fluctuated within a narrow margin of less than 2% and settled steadily at approximately 800 V. This result verifies that the proposed control strategy has no adverse effect on the DC-side stability of the qZSI, thereby ensuring reliable power conversion and highlighting its practical applicability.

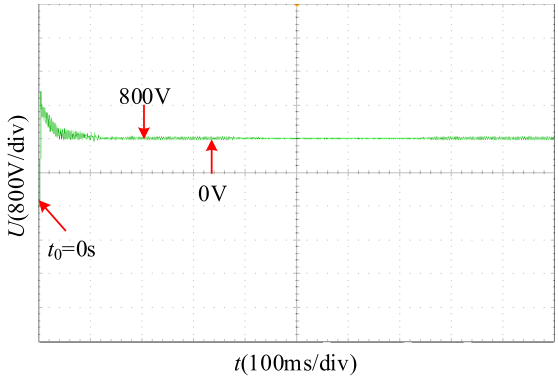

FIGURE 15. Voltage value across capacitor C_1 in the qZSI network.

4.4. Harmonic Performance Analysis

The proposed variable-weight virtual impedance control adjusts the dq-axis impedances based on power deviations. This adaptation inherently provides low-pass filtering characteristics: the virtual inductance L_v suppresses high-frequency current ripple, while the virtual resistance R_v provides damping. Unlike fixed-gain negative-sequence compensation schemes that may create resonant peaks, the proposed adaptive mechanism continuously modifies the impedance to avoid sustained harmonic excitation.

Moreover, the ANF used for sequence separation (Section 3.3) inherently attenuates frequencies above 100 Hz, with a rejection bandwidth of 100 Hz and $>$ 20 dB attenuation at 250 Hz (5th harmonic). Consequently, no additional harmonics are injected by the negative-sequence compensation loop. The experimental current waveforms in Figs. 11(c) and 14(c) show no visible high-frequency distortion, confirming that harmonic interactions are negligible.

5. CONCLUSION

To address the challenges of output current over-limitation, power oscillation, and diminished transient stability in qZSI-VSG systems under asymmetric faults, this study proposes a balanced current control strategy based on variable-weight virtual impedance. Through theoretical analysis and experimental validation, the following principal conclusions were drawn:

1) The devised negative-sequence current reference calculation method effectively suppresses the negative-sequence components during grid voltage imbalance. Under both single-phase and two-phase voltage sag faults, the proposed strategy demonstrates robust performance in restraining these components, thereby significantly enhancing the output current quality and maintaining the three-phase current imbalance at a low level.
2) The proposed variable-weight virtual impedance mechanism enables the adaptive coordination of d- and q-axis impedances through real-time monitoring of active and reactive power deviations. Compared with the balanced-current-control approach, this strategy reduces the peak

inrush current by 24–33% and shortens the power oscillation recovery time by 13.8–15.2%, thereby effectively resolving the inherent conflict between current limitation and power support during fault transients.

3) The proposed strategy demonstrates strong adaptability and stability for various types and severity levels of asymmetric faults. Even under severe conditions, such as two-phase voltage sags, the system maintains a stable operation, with the qZSI DC-side voltage fluctuation consistently constrained within 2%. These results validate the practical engineering value of the proposed method.

ACKNOWLEDGEMENT

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